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Efficient EM simulation of GCPW structures applied to a 200-GHz mHEMT power amplifier MMIC

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Abstract The behaviour of grounded coplanar waveguide (GCPW) structures in the upper millimeter-wave range is analyzed by using full-wave electromagnetic (EM) simulations. A methodological approach to develop reliable and time-efficient simulations is proposed by investigating the impact of different simplifications in the EM modelling and simulation conditions. After experimental validation with measurements on test structures, this approach has been used to model the most critical passive structures involved in the layout of a state-of-the-art 200 GHz power amplifier based on metamorphic high electron mobility transistors (mHEMTs). This millimeter-wave monolithic integrated circuit (MMIC) has demonstrated a measured output power of 8.7 dBm for an input power of 0 dBm at 200 GHz. The measured output power density and power added efficiency (PAE) are 46.3 mW/mm and 4.5%, respectively. The peak measured small-signal gain is 12.7 dB (obtained at 196 GHz). A good agreement has been obtained between measurements and simulation results.

Keywords millimeter-wave · MMIC (monolithic millimeter-wave integrated circuit) · mHEMT (metamorphic high electron mobility transistor) · power amplifier, GCPW (grounded coplanar waveguide) · electromagnetic simulation.

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1 Introduction

The atmospheric window located around 200 GHz has been identified as an important frequency range for applications like millimeter-wave imaging [1] or high-speed data communication. These applications raise the demand for power amplifiers, since the operating range of these systems is a direct function of the transmitted power. A millimeter-wave monolithic integrated circuit (MMIC) solution offers tremendous advantages in terms of compactness, repeatable performance and low-cost fabrication in large quantities [2].

Successful and efficient design of MMICs in the upper millimeter and submillimeter-wave ranges requires reliable models of all active and passive components. This is especially critical in the particular case of high electron mobility (HEMT)-based power amplifiers. Due to the low breakdown voltage provided by the available (GaAs metamorphic HEMT (mHEMT) [3] and InP HEMT [4]) technologies and the high losses of the passive networks, achieving low-loss on-chip power combining and matching is one of the main challenges. Therefore, a reliable simulation of all components becomes completely necessary to avoid additional losses.

3D full-wave simulation is widely considered as a very powerful tool for modelling of passive structures in millimeter-wave applications. However, this type of simulations implies considerable computational cost, often prohibited for design purposes. Additionally, the complexity of some physical structures (for example, multilayer dielectric and metallization stacks composed of ultra thin layers) make 3D modelling a cumbersome task. Commercial software packages are claimed to handle a wide range of problems. However, the specific properties of the problem to be solved determine which of the existing techniques is most advantageous and under which simulation conditions.

Previous work about electromagnetic (EM) simulation to predict the performance of some grounded coplanar-waveguide (GCPW) structures beyond 100 GHz can be found in [5], [6] and [7]. The novelty of the current work in comparison to previous contributions lies in that it presents an overall description of the main methodological aspects involved to achieve, not only accurate simulation of these structures, but also low computation time. The impact of different simplifications in the EM modelling and simulation conditions is analyzed. This investigation includes validation with experimental results from different test structures.

Furthermore, a state-of-the-art medium power amplifier is demonstrated. At an operating frequency of 200 GHz, this MMIC achieves a measured output power of 8.7 dBm for an input power of 0 dBm. The output power density and the power added efficiency (PAE) are 46.3 mW/mm and 4.5%, respectively. Following the proposed methodology, EM simulations for specific passive parts involved in the final amplifier layout have been carried out. The results of these EM simulations have been used in the overall simulation of the amplifier, obtaining a good agreement up to 260 GHz. Simulations of the complete amplifier were performed with Advanced Design System (ADS), by using S-parameter and Harmonic Balance analysis.

The paper is organized as follows. In Section 2, a brief description of the technology is provided. Section 3 explains the proposed methodology to perform efficient EM simulations of GCPW structures and also the experimental validation with test structures is presented. Power amplifier design and experimental evaluation are described in Section 4. Finally, some conclusions are drawn in Section 5.

2 Technology

The present work is based on the Fraunhofer IAF mHEMT technology. Transistors are grown via molecular beam epitaxy (MBE) on 4-inch GaAs wafers. Their channel is based on an $In_{0.52}Al_{0.48}As/In_{0.80}Ga_{0.20}As/In_{0.53}Ga_{0.47}As$ heterostructure on a metamorphic buffer with a linear $In_xAl_{0.48}Ga_{0.52-x}As$ ($x = 0 \rightarrow 0.52$) transition in composition. The 35-nm T-gates are defined by electron beam lithography and a Pt-Ti-Pt-Au layer sequence is used for the gate metallization.

The transistors are encapsulated in a low-k benzocyclobutene (BCB) layer ($\epsilon_r = 2.65$) to minimize the parasitic gate capacitance, and passivated with 250-nm-thick silicon nitride (SiN) for high reliability and robustness. This SiN layer also acts as the dielectric layer of the on-wafer metal-insulator-metal (MIM) capacitors and is grown by chemical vapor deposition (CVD).

In addition to the active devices and the MIM capacitors, NiCr thin-film resistors and two interconnection layers, that can be stacked to a 3 μm thick metal sheet, are available. The lower metal layer is electron beam evaporated and has a thickness of 0.3 μm, whereas the plated upper layer has a thickness of 2.7 μm and is available in airbridge technology. The transmission lines used in this work are realized using both metal layers and utilize a GCPW environment with 50 μm ground-to-ground (GG) spacing. After front-side processing, a full back-side process follows. This includes wafer thinning to a 50 μm thickness, through-substrate via-holes and backside metallization. The precision of the process allows via-holes below MIM capacitors without damaging the first metallization layer.

3 EM simulation of GCPW structures in the upper millimeter-wave range

The methodology for the EM modelling is based on full-wave analysis. This is carried out with CST Microwave Studio frequency-domain solver, based on the Finite Element Method (FEM).

The aim is to use a description of the structure as simplified as possible to perform a computationally efficient numerical analysis with a short modelling time, while being accurate enough for design purposes. Note that the final goal is circuit design. The considered GCPW structures are based on the layer structure shown in Fig. 1 (left). Some possible simplifications that will be

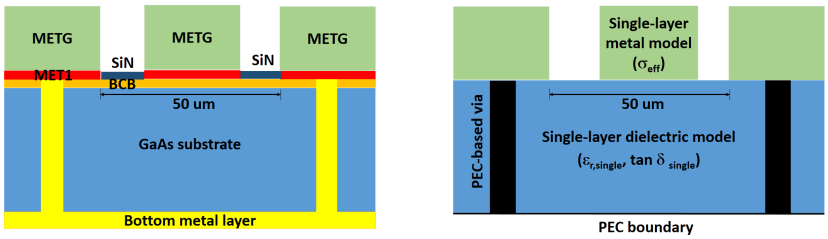

Fig. 1 Cross section of GCPW transmission line: real layer structure (left) and simplified model (right).

explored with the aim of achieving more efficient simulations are shown in Fig. 1 (right).

A simplified dielectric model is used which substitutes the two layers (GaAs and BCB) by an effective single layer. Its thickness is obtained by summing the thicknesses of the two individual dielectric layers. Unique values for the dielectric constant and the loss parameter $tan\delta_{single}$ must be determined for single-layer reduction. The thin BCB layer causes a change in the effective dielectric constant, so an homogeneous substrate model that replaces the combination of BCB and GaAs layers must be simulated with a lower value of the dielectric constant in comparison to the value of GaAs ($\epsilon_r = 12.9$). The values of the dielectric constant and $tan\delta_{single}$ for this effective single dielectric layer have been obtained by fitting the EM model of a transmission line to measurements. As it is shown later, this model has been further validated with another different test structure. The values ($\epsilon_{r,single} = 10.5$, $tan\delta_{single} = 0.006$) are defined at 200 GHz and a Debye first-order model [10] is used to simulate the frequency dispersion. According to this model, the permittivity function is of the form

$$\epsilon(\omega) = \epsilon(\infty) + \frac{\epsilon_s - \epsilon(\infty)}{1 + j\omega\tau},$$

where ϵ_s and $\epsilon(\infty)$ are the static and high-frequency permittivities of the medium, ω is the angular frequency and τ is the relaxation time.

Also a metal single-layer reduction could be applied instead of using the double-metal stack. The effective conductivity of the single metal layer can be estimated by $\sigma_{eff} = (\sigma_{MET1} * t_{MET1} + \sigma_{METG} * t_{METG})/t$, where σ_{MET1} and σ_{METG} are the individual conductivities of the two metallization layers, t_{MET1} and t_{METG} are the thicknesses of these metallizations and $t = t_{MET1} + t_{METG}$ is the total thickness.

Due to the skin effect, at millimeter-wave frequencies current flows in an extremely thin region near the surface of the conductors. In order to save computational effort, surface-based meshing (sheet conductor) is an interesting alternative to explore instead of volume-based meshing (that is, solving inside the metal).

A straight GCPW transmission line is considered. This structure has a 50 μm GG spacing and its length is 1500 μm. On-wafer S-parameter measurements were performed on this structure using an Agilent PNA-X network analyzer, two VDI 4.3 frequency extension modules and two Cascade i260 microwave probes. For a 2-port TRL calibration, a Cascade 138-356 calibration substrate was chosen. This calibration establishes the reference planes at the probe tips. The measurement curve in Fig. 2 shows some small resonances. In the upper millimeter-wave range, it is common that S-parameter measurements are affected by some artifacts, related to spurious wave modes that excite and propagate. These artifacts could even be present in the calibration measurement. However, in this case they seem to arise only in the measurement of specific test structures, so they are not considered to be an influence of the calibration.

Different EM simulations have been performed and compared with the measurements of the transmission line. In all the cases, CST de-embedding tool has been used to move the reference planes from the line structure edges (where the ports are placed) to the probe tip positions.

First, the impact of some simulation conditions has been analyzed. The transmission line has been simulated by using surface and volume meshing for the single effective conductor layer. Concerning the frequency-domain solver, also two options have been explored: simulation of discrete frequency points or interpolating S-parameter sweep to minimize the number of simulations.

Fig. 2 shows the comparison between measured and simulated results in the four considered cases. Simulations are based on a simplified EM model (named model 1), based on single-layer dielectric, single-layer metallization, a passivation layer, a perfect electrical conductor (PEC) boundary to simulate the bottom ground plane, and ideal via-hole elements based also on PEC.

The computation performance is presented in Table 1. The results have been obtained on a CPU based on 2 processors (Intel Xeon E5-2630 v3 at 2.4 GHz) and 128 GB of RAM. As it can be observed, volume meshing is computationally much more intensive and achieves a comparable accuracy. Note that, in the case of simulating discrete frequency points, the solver time is given in seconds per frequency sample. However, in the case of interpolating S-parameter sweep, increasing the number of points does not significantly increase the time required for a simulation and it is even possible to recalculate the broadband S-parameter curves with a higher number of frequency samples as a postprocessing step. Since this methodology is focused on efficient design, interpolating frequency sweep and surface meshing for the conductors will be used from now on. The type of meshing is a combination of tetrahedral volume meshing for the dielectric layers and triangular surface meshing for the conductor layers. The mesh density is established to be at least 10 cells per wavelength of maximum frequency.

Next, the impact of different simplifications in the EM model on simulation accuracy and computation time has been evaluated. The resuls are shown in Fig. 3 and Table 2. This table also includes a summarized description of the different EM models. The comparison between a single-layer and a double-

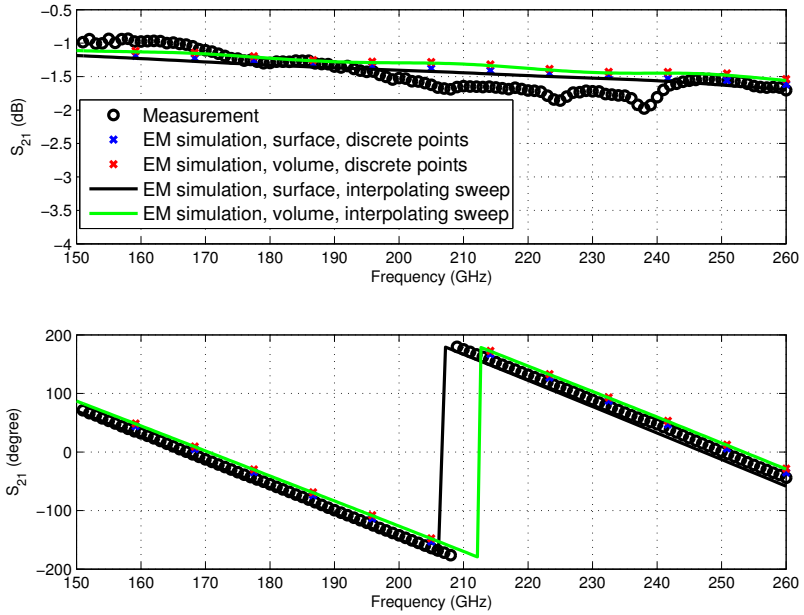

Fig. 2 Comparison between EM simulation (model 1) and measurements for a 1500 μm transmission line.

Table 1 Comparison of computation performance by using different simulation conditions, by using EM model 1.

Meshing type	Solver	Solver time
Volume	Discrete points	2357 s/frequency point
Volume	Interpolating sweep	4722 s
Surface	Discrete points	177 s/frequency point
Surface	Interpolating sweep	498 s

layer model to simulate the metal stack shows that the difference in accuracy is small, whereas there is an important reduction in computation time. The simulation of the passivation layer is also proven to have little impact on accuracy. This SiN layer (with a relative permittivity $\epsilon_r = 6.5$) slightly increases the effective dielectric constant in contrast to the simulations where the layer is not included (i.e. substituted by air $\epsilon_r = 1$). This explains a small phase advance observed in Fig. 3 between model 3 and model 1, whose only difference in the presence or absence of this passivation layer.

In models 1 and 3-4, the bottom surface of the substrate is defined as a PEC boundary and the via-holes are considered very simple PEC bricks. The impact of these simplifications on simulation accuracy and computation time is shown by comparison between models 2 and 3. The use on a nonzero-thickness bottom metallization and a more realistic via-hole model defined as intersection of shapes with finite conductivity produces a negligible difference in accuracy in the operating frequency range. Note that this range is far away

Table 2 Description of the different EM models and impact on computation time.

Model	Dielectric	Metal	SiN	Bottom ground	Via	Solver time
1	Single	Single	Yes	PEC	PEC	498 s
2	Single	Single	No	Non ideal	Non ideal	955 s
3	Single	Single	No	PEC	PEC	215 s
4	Single	Double	Yes	PEC	PEC	3992 s

from parasitic resonances, thanks to the use of a sufficient number of via-holes. Considering computation-time, the simulation with the simpler model (model 3) is more efficient (more than a factor of 3) and therefore can be used for fast circuit design if via-holes are located at a distance that ensures an operating bandwidth far away from unwanted resonances. In [8] the authors recommend to use a via-to-via pitch lower than quarter wavelength at the highest frequency to remove resonances in the GCPW. In this structure, via-to-via distance is $\lambda/6$ at the highest frequency of operation.

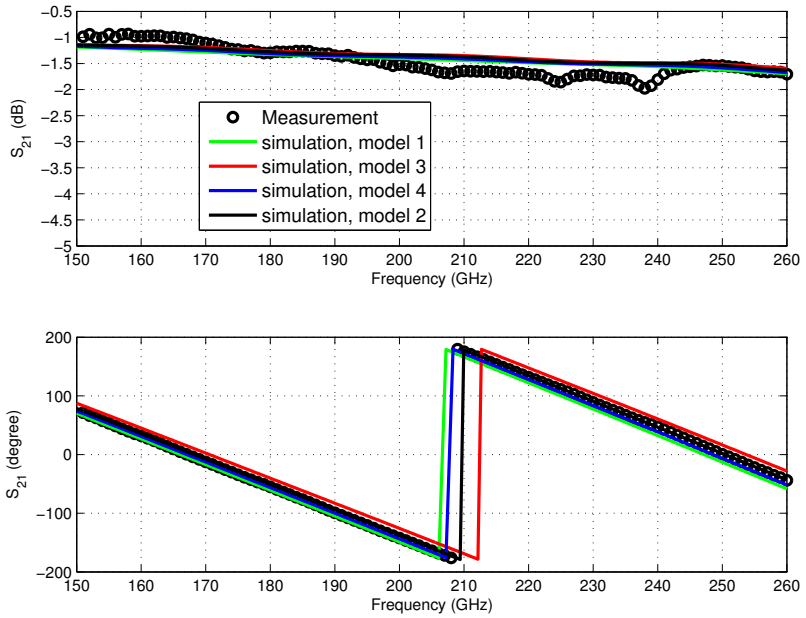

Fig. 3 Comparison between measurements of a 1500 μm transmission line and EM simulation under different 3D modelling approaches.

In order to make a more general experimental validation of the proposed methodology, another measured test structure, in this case including discontinuities, was considered. Fig. 4 shows the EM model of this structure and the comparison between measurements and EM simulation. An excellent agreement has been obtained, validating the simulation methodology based on model 3.

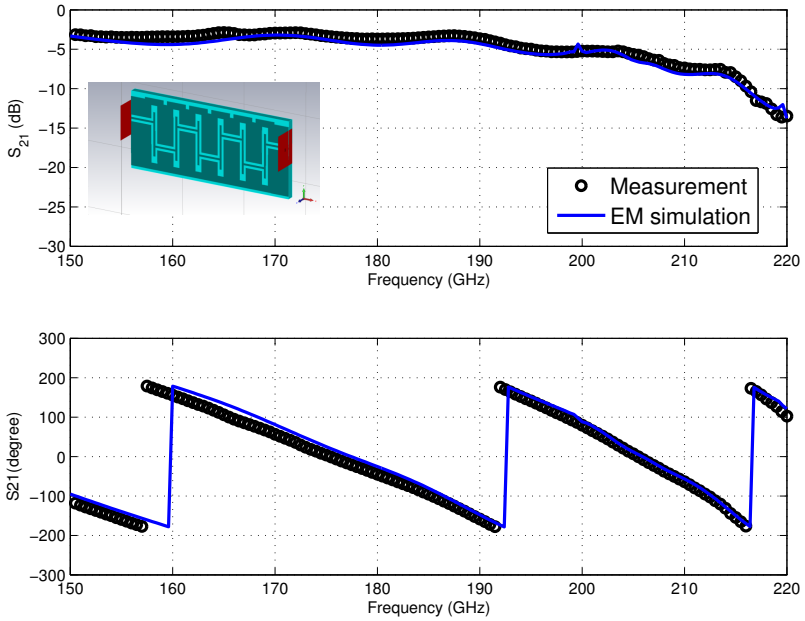

Fig. 4 Comparison between EM simulation (model 3) and measurements for a test structure.

4 A 200 GHz mHEMT power amplifier MMIC

A four stage MMIC amplifier was designed and fabricated using the mHEMT technology described in Section 2. The overall circuit topology and the chip photograph of the MMIC are shown in Figs. 5 and 6, respectively. The die size is 3×1 mm^2.

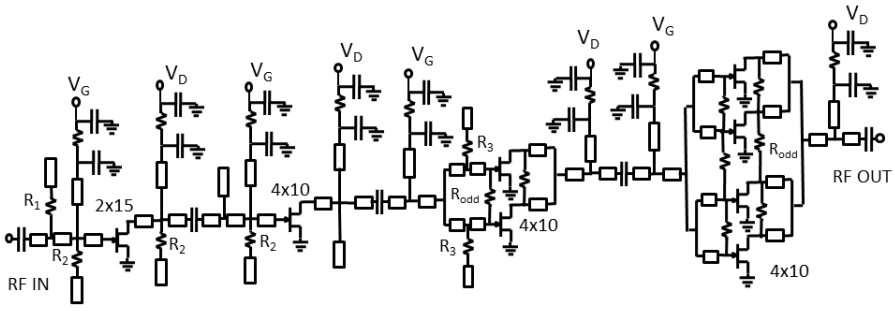

Fig. 5 Schematic circuit diagram of the 200 GHz power amplifier.

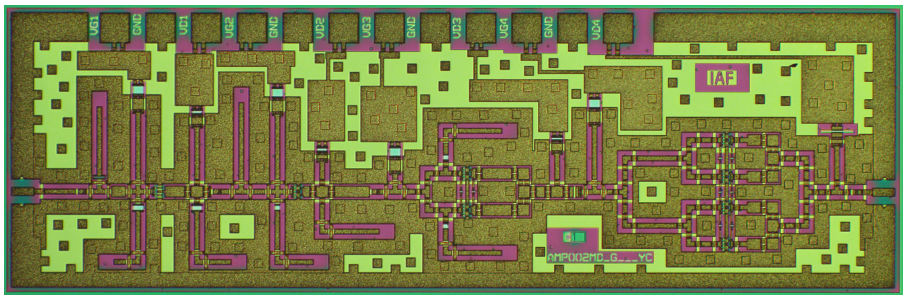

Fig. 6 Chip photograph of the MMIC power amplifier.

This amplifier is based on transistors in common-source configuration. The gate width of these active devices is 2×15 μm for the first stage, and 4×10 μm for the other three stages.

In order to minimize losses in the passive networks, this MMIC is based on a 50 μm GG environment. A smaller GG distance provides higher compactness, but the lines are more lossy. For a 50 μm GG spacing and using a stack of both metallizations, the losses are 0.9 dB/mm at 200 GHz, whereas transmission lines with a 14 μm GG spacing show 3.1 dB/mm, if they are based only on the first metallization level, or 2.4 dB/mm, if both metallizations are stacked to form the center conductor strip. The three previous values correspond to measured results on real test structures. To make a complete comparison, a transmission line with 50 μm GG spacing has been simulated using only the first metallization. The predicted losses in this case are 1.1 dB/mm.

Stability is one of the key issues in the design of power amplifiers. This MMIC has been stabilized by using open-ended stubs loaded with NiCr resistors. These resistive components for stabilization (R_1,R_2,R_3) are pointed out in the circuit schematic diagram (see Fig. 5). Also resistors (R_{odd}) are inserted between parallel branches to prevent odd-mode oscillations. Finally, shunt RC networks were added at the end of the gate and drain bias stubs to suppress the excessive gain at low frequencies.

Full-wave EM simulations have been executed to predict the performance of several passive elements, which were considered especially critical by different criteria. Most of them included modifications of the standard layout cells from the available Fraunhofer IAF library. For example, some of the T-junction combining structures required flattened layout cells to achieve compactness or presented some asymmetries due to the proximity of isolation resistors. Open terminations were also selected due to their impact on stability. Thus the final simulation of the power amplifier combines analytical models (for the most simple passive structures and for the active devices) and 3D EM models of these critical parts (represented in Fig. 7). The results of the EM simulations were exported in Touchstone format and imported in the form of S-parameter blocks into ADS simulator.

Figs. 8 and 9 show the comparison between measured and simulated performance of the amplifier MMIC. Both small-signal and power measurements

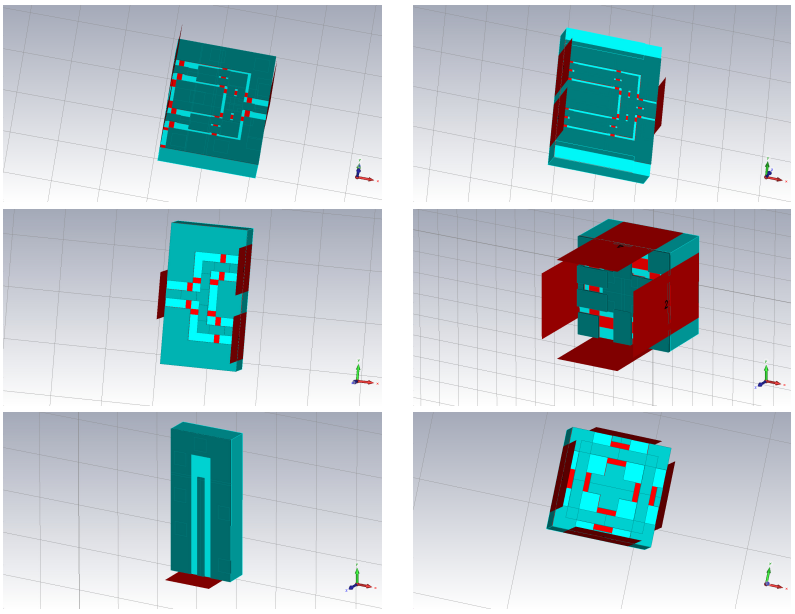

Fig. 7 Simulated 3D models of GCPW structures present in the amplifier layout.

were made directly on-wafer. The former measurements were performed using an Agilent PNA-X network analyzer with two VDI 4.3 frequency extension modules, achieving a peak small-signal gain of 12.7 dB (at 196 GHz).

Output power was measured by using a G-band Elva power meter. Fig. 10 shows the schematic diagram. In order to generate enough input power to drive the amplifier at least close to saturation, a commercial diode-based frequency-doubler module (from Virginia diodes) is employed, who is driven by an in-house W-band power amplifier. The input signal for this amplifier is generated by a commercial source module. This measurement set-up can generate up to 0 dBm of output power at the chip input reference plane. For all stages, the bias voltages were set to: $V_G = 0.04\,V$, $V_D = \ 1.0\,V$. In Fig. 9, all power levels are normalized to the probe tip reference plane. The amplifier exhibits a gain expansion before compression. This expansion is a nonlinear phenomenon that can be observed in some amplifiers and is often related to distortion minima [11]. The 1 dB compresssion point of the PA is 7.3 dBm (output power). This P_{1dB} value is determined by assuming that the nominal gain is the maximum gain, which occurs at an input power of - 10 dBm. For a 0 dBm input signal, the MMIC demonstrates a measured output power of 8.7 dBm. Since the amplifier has an output periphery of 4×4×10 μm, this corresponds to an output power density of 46.3 mW/mm. A maximum PAE of 4.5 % has been measured. The experimental performance compares well with the literature referred to mHEMT power amplifiers (see Table I in [9]). Also a good agreement has been obtained between simulation and measurements.

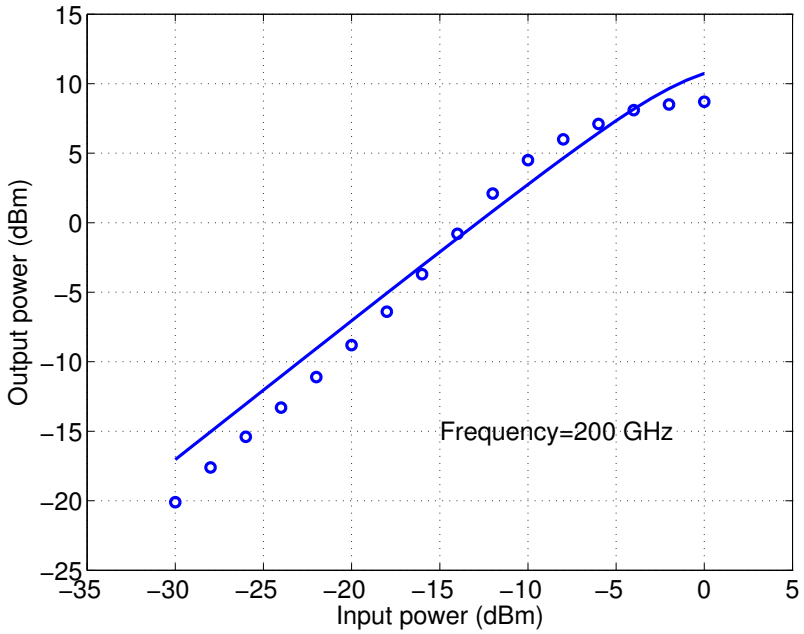

Fig. 8 Large-signal measured and simulated performance of the power amplifier MMIC.

5 Conclusion

3D full-wave EM models of GCPW structures may be time-consuming to evaluate when taking into account every detail. This investigation has proven that some simplifications in the EM modelling can be applied that allow for an important reduction in computation time while keeping a high accuracy. This is especially important for design applications, which very often involve optimizations. A state-of-the-art 200 GHz power amplifier MMIC is experimentally demonstrated. For an input power of 0 dBm, the MMIC achieves an output power of 8.7 dBm (output power density of 46.3 mW/mm) and a PAE of 4.5%. Following the proposed methodology, EM models for the most critical discontinuities in the amplifier layout have been generated and used together with analytical models for the remaining structures. The global simulation of the amplifier achieves a good agreement with the experimental results.

In the future, these results could be extended by considering temperature dependence of material parameters in the EM simulations as well as temperature-dependent measurements. Another interesting investigation would be to consider frequency dependence of conductivity and surface impedance models to find a good compromise between accuracy and computational complexity even in a broader bandwidth.

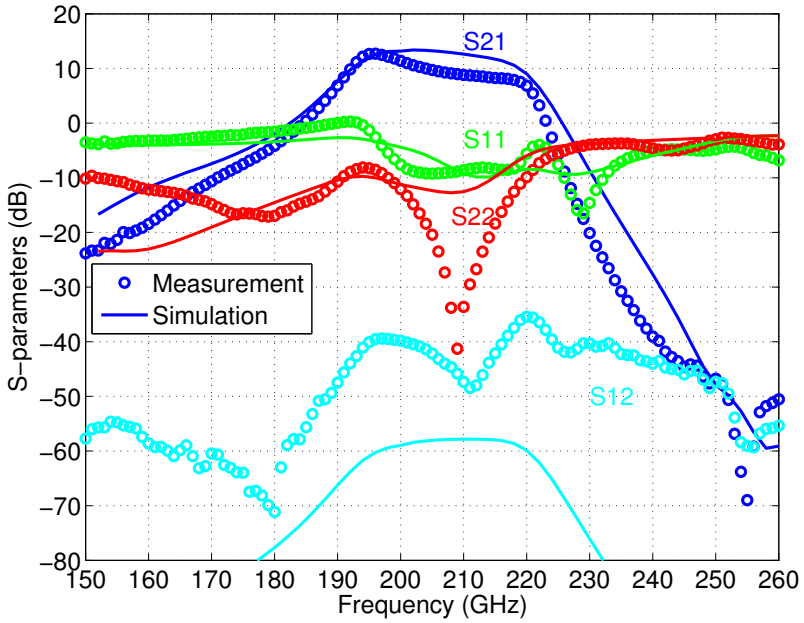

Fig. 9 Small-signal measured and simulated performance of the power amplifier MMIC.

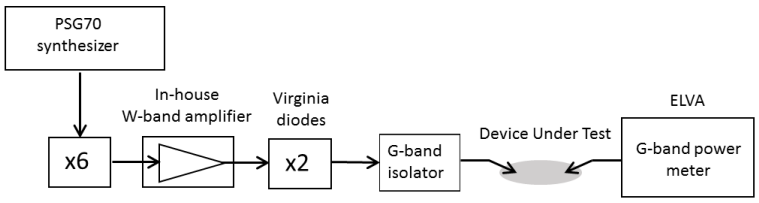

Fig. 10 Power measurement set-up.

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