THIS IS AN EARLIER VERSION OF THE PAPER WITH DOI: 10.1109/TTHZ.2018.2801562

Analysis and Development of Submillimeter-wave Stacked-FET Power Amplifier MMICs in 35-nm mHEMT Technology

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***Abstract*—This paper reports on the first stacked field effect transistor (stacked-FET) submillimeter-wave monolithic integrated circuit (S-MMIC) power amplifier cell operating at 0.3 THz and the first stacked-FET medium power amplifier (MPA) at 240 GHz. Both circuits are fabricated using a 35 nm InGaAs-on-GaAs metamorphic high electron mobility transistor (mHEMT) technology with grounded coplanar waveguide (GCPW) lines. In both cases, compactness and performance are enhanced thanks to the use of an in-house process, based on three metallization layers, instead of the usual two-layer process. The single stacked-cell exhibits an ultra-wide small-signal 3-dB relative bandwidth (RBW) of $47.3\,\%$, with output power levels higher than 4.3 dBm from 280 to 308 GHz (9.5 %). The MPA MMIC combining four triple-stacked mHEMT cells in parallel achieves a small-signal 3-dB RBW of 24.2 %, 10.8 dBm of output power and a power-added efficiency of 5.02 %. These values outperform the state-of-the-art results of MPAs published within a comparable technology.**

***Index Terms*—Stacked-FET, Dolph-Chebyshev, power amplifier, submillimeter-wave monolithic integrated circuit (S-MMIC), metamorphic high electron mobility transistor (mHEMT).**

I. Introduction

The importance of integrated power amplifiers (PAs) at millimeter and submillimeter-wavelengths (mmW and sub-mmW) has already been pointed out in numerous publications due to their wide range of applications. Among the most relevant ones are high-resolution imaging radar systems for security, safety and health, and high-data rate communications [1], [2],[3]. In this frequency range compactness, low weight and wide available bandwidth are important requirements.

However, at mmW and sub-mmW frequencies PA monolithic integrated circuits (MMICs) present low efficiency and gain, as well as limited breakdown voltages of the active devices, which are the main bottlenecks to be overcome. Low breakdown voltage is the main factor that limits the achievable output power, so that one of the conventional solutions is to use power combining and distribution networks that are costly in terms of area [4]. For example, Tandem-X structures cascade several couplers together and split the input power just into two outputs (1:2 hybrid) [5]. In order to increase supply voltages and RF voltage swing without sacrificing much reliability, stacked field effect transistor (stacked-FET) topologies have been implemented and widely considered in the literature to develop power amplifiers up to W-band [6], [7].

To the best of the authors' knowledge, the only publication about stacked-FET PA cells (with more than two transistors in series) beyond W-band up to now is [8], which demonstrates results of single cells at 240 and $280\,\mathrm{GHz}$. These results were obtained by using a $50\,\mathrm{nm}$ metamorphic high electron mobility (mHEMT) process and two metallization layers.

The H-band (200-300 GHz) PA cell presented here is based on a different process ($35\,\mathrm{nm}$ and 3 metallization layers), which has allowed to increase the operating frequency. This PA outperforms the results in [8] in terms of bandwidth, output power and power added efficiency (PAE).

Parallel combining of several stacked-FETs can lead to higher output power levels. For example, in [9] 4 stacked-FET cells are combined in parallel to achieve $20\,\mathrm{W}$ of output power at S-band (2-$4\,\mathrm{GHz}$), and in [10] eight stacked-FET unit power cells are used in a distributed power amplifier to get $17.5\,\mathrm{dBm}$ at $110\,\mathrm{GHz}$.

This parallel design strategy has also been considered in this work. In addition to the H-band single-cell, a $240\,\mathrm{GHz}$ medium PA (MPA) is presented based on a parallel combination of stacked-FETs. The experimental performance of this MPA overcomes the state-of-the-art results obtained with comparable technologies.

The paper is organized as follows. In Section II, a description of the technology used to develop the two MMICs is included. Section III covers the design and experimental results of the H-band stacked-FET power amplifier cell. In Section IV, the same aspects are discussed for a $240\,\mathrm{GHz}$ MPA that combines four triple-stacked FET power cells in parallel by using Dolph-Chebyshev structures. Furthermore, Section IV includes a discussion comparing the experimental performance with the state of the art. Finally, the conclusions of this work are summarized in Section V.

II. Technology

The technology used to process both MMICs is based on InGaAs mHEMT heterostructures on 4" GaAs substrate, using a length of $35\,\mathrm{nm}$ for the T-gates. By molecular beam epitaxy (MBE) the linearly graded InGaAlAs buffer is grown on

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Manuscript received April XX, XXXX; revised August XX, XXXX.

TABLE I
ELECTRICAL DC- AND RF-PARAMETERS OF THE 35 NM MHEMT PROCESS ($W_G = 2 \times 10$ µm).

Parameter	Symbol	Unity	Values
Gate length	L_g	nm	35
Indium content of composite channel	In	%	80
Transit frequency	f_T	GHz	515
Max. osc. frequency	f_{max}	GHz	1000
Max. transconductance	$g_{m,max}$	mS/mm	2500
Max. drain current density	$I_{d,max}$	mA/mm	1600
Off-state breakdown voltage	$BV_{off-state}$	V	2
On-state breakdown voltage	$BV_{on-state}$	V	1.5

4" semi-insulating substrates. To adapt the lattice constant, the buffer is graded so that the $Al_{0.52}Ga_{0.48}As$ (GaAs) layer is linearly exchanged to $Al_{0.52}In_{0.52}As$ (InAs). This metamorphic buffer is placed between the GaAs substrate at the bottom and the InGaAs channel beneath the T-shaped gate contact [11]. A Pt-Ti-Pt-Au layer sequence is used for gate metallization. To suppress substrate modes the wafers are thinned down to 50 µm.

To increase the carrier mobility, the 35 nm gate-length technology features a channel indium content of 80 %. In comparison to other in-house mHEMT processes (with 100 and 50 nm gate lengths), the transit frequency (f_T) and maximum oscillation frequency (f_{max}) increase to up to 515 GHz and 1 THz, respectively, as described in [12]. This allows the design of MMICs in the submm-wave frequency range. Moreover, a transconductance of $g_{m,max} = 2500\,\mathrm{mS/mm}$ and a maximum drain current of $I_{DS,max} = 1600\,\mathrm{mA/mm}$ are achieved.

However, with shorter gate and channel lengths, the field intensity increases so that a reduction of the drain-source voltage is needed to prevent the transistor from breakdown. The off-state breakdown voltage is $BV_{off-state} = 2\,\mathrm{V}$ for a common-source (CS) transistor. That voltage reduction lowers the available output power of the device, so that a trade-off between output power and cutoff frequency has to be found.

The MMICs processed in this work are based on a three-metallization layer process as shown in Fig. 1. In comparison to the previous in-house two-layer process, this process is based on three top metal stacked-layers, that can be used for the signal path, and the addition of a second extra BCB layer between the two thin Au layers (MET1 and MET2) [13], [14]. MET1 and MET2 are electron evaporated Au layers with the same 0.3 µm thickness, while METG is an Au layer produced by galvanic metallization and has a thickness

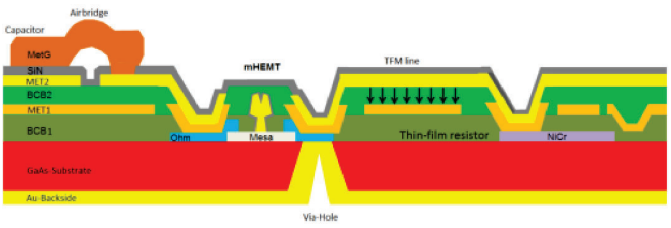

Fig. 1. Cross-section of the 3-metallization layer 35 nm mHEMT tecnhnology of Fraunhofer IAF.

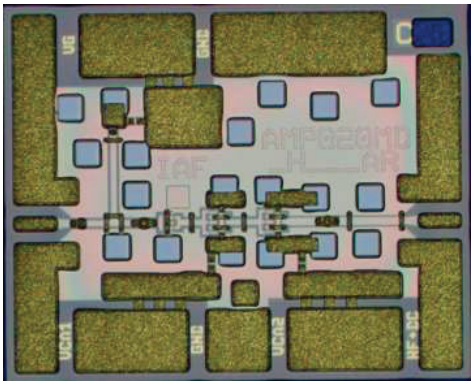

Fig. 2. Chip photograph of the single stacked-FET cell. Its die area is $0.54 \times 0.65\,\mathrm{mm}^2$.

of 2.7 µm. In the two-layer process, the signal-path can be directly implemented in MET1 or use a metallization stack based on the combination of MET1 and METG. The three-layer process adds an additional Au metal layer (second metallization or MET2), which is constructed with the same material (gold) and thickness (0.3 µm) as the first metal layer.

Therefore, the four metal layers that constitute the 35 nm process are MET1, MET2, METG and the ohmic layer, that can be used as an additional interconnect layer for short distances with a sheet resistance of $0.8\,\Omega/sq$. The number of metallization layers used for the central strip line (where the signal propagates) depends on the requirements of the concrete MMIC. For example, whereas the single stacked-FET cell described in Section III uses only one metal layer (MET1), the MPA considered in Section IV includes also MET2 and METG at the output drain $\lambda/4$ stub to enhance the conductivity as well as to reduce the DC drain bias losses that is applied to the transistors.

Another important characteristic of the novel 3-layer process is the thickness reduction of the SiN layer. In this case, the passivation layer is 80 nm thick, whereas in the two-metallization process it has a thickness of 250 nm. That leads to an increment of the capacitance value per area, which is $0.8\,\mathrm{fF}/\mu\mathrm{m}^2$ in the 3-layer process in comparison to $0.225\,\mathrm{fF}/\mu\mathrm{m}^2$ in the 2-layer process. As a consequence, less die area is needed to achieve the same capacitance value, resulting in more compactness.

III. 300 GHZ SINGLE-CELL STACKED-FET PA

In [8] the first stacked-FET at 280 GHz is demonstrated. This design was based on a different in-house process (with 50 nm gate length and two metallization layers). In this section, a re-design of this cell is done at 300 GHz to enhance the bandwidth, gain, output power level and PAE. In order to achieve this, a 35 nm technology with the three-layer process is employed. The S-MMIC is realized with 14 µm ground-to-ground grounded coplanar waveguide (GCPW) lines.

A. Design topology

The chip photograph of the processed circuit and its equivalent schematic diagram are shown in Figs. 2 and 3, respectively. The chip die area is $0.54 \times 0.65\,\mathrm{mm}^2$. The gate width

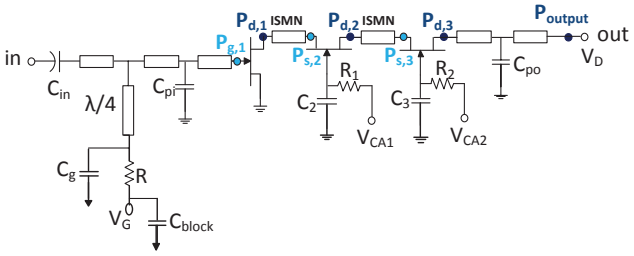

Fig. 3. Schematic diagram of the single stacked-FET cell.

for each transistor is 40 µm. The designed gate capacitors, C_1 and C_2, were obtained by optimization which considered stability as well as output power goals. Simulations were carried out using Keysight's Advanced Design System (ADS). The resistor R at the input matching network is used to avoid low-frequency instabilities, whereas the resistors R_1 and R_2 are employed to avoid in-band instabilities.

At the input, a conventional matching network is used to match the input impedance of the amplifier cell to the reference impedance $R_o = 50\,\Omega$, whereas at the output a large-signal matching (according to the Cripps load) to a 50 Ω impedance has been realized and the drain DC voltage (V_D) is applied externally from the RF output port (see Fig. 3). Because of that, only one DC blocking capacitor (C_{in}) is placed at the input. At the output the series capacitor has not been included as shown in Fig. 3

B. Experimental performance

Small-signal and large-signal measurements were carried out with the processed MMICs. An Agilent N5224A vector network analyzer system with two Oleson V03VNA2 T/R frequency extension modules and two Picoprobe Infinity GSG 60 microwave probes were used for the S-parameter measurements [15]. The large-signal characterization was done by using a scalar measurement system, based on an H-band Erikson power sensor. In order to generate enough input power to drive the amplifier close to saturation, a Virginia diode-based frequency-tripler module and an in-house driver MPA module were used. The calibration was performed using the SOLR (Short-Open-Load-Reciprocal) method, described in [16].

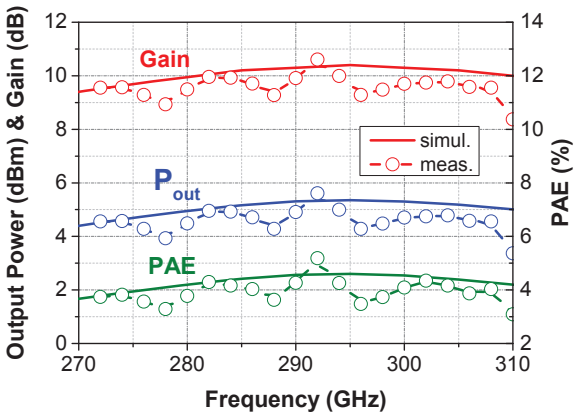

Fig. 5. Measured (line with circle symbols) and simulated (straight line) power, gain and PAE frequency sweep when $P_{input} = -5$ dBm.

The small-signal results and their comparison with the simulation performed in ADS are included in Fig. 4. The simulated and measured results are in good agreement. These S-parameter measurements were obtained when applying the following bias conditions: $V_D = 2.7$ V, $V_G = 0.2$ V, $V_{CA1} = 0.9$ V and $V_{CA2} = 2$ V. These linear results demonstrate a maximum small-signal gain (S_{21}) of 12.7 dB at 259 GHz, with a remarkable 3-dB relative bandwidth (RBW) of 47.3 % (from 187 GHz to 303 GHz).

Not only the small-signal results demonstrate broadband performance, but also the large-signal measurements (see Fig. 5) exhibit a good performance in a wide frequency range. For these measurements, different DC bias conditions are applied with the aim of achieving higher output power. Therefore, the results plotted in Fig. 5 are obtained when $V_G = 0.1$ V and $V_D = 3.4$ V. V_{CA1} and V_{CA2} are not biased in this case (they

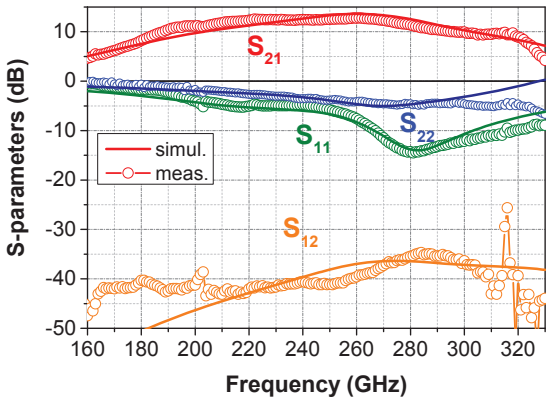

Fig. 4. Small-signal measurement (line with circle markers) and simulation (straight line) results for the processed MMIC.

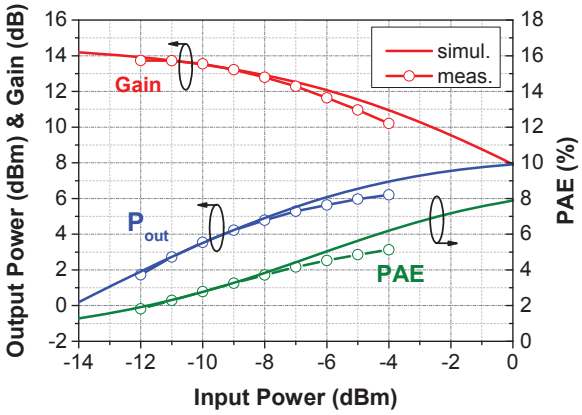

Fig. 6. Measured (line with circle symbols) and simulated (straight line) large signal measurements at 292 GHz.

act as floating terminals).

It can be observed in the measured results (line with circle symbols) that a maximum output power of $5.6\,\mathrm{dBm}$ is demonstrated at $292\,\mathrm{GHz}$ when the applied input power was $P_{in} = -5\,\mathrm{dBm}$, which corresponds to the 4-dB compression point. Besides that, at this point the PAE is remarkably high (PAE = $5.2\,\%$), which is better than the values already achieved by the state-of-the-art PA in [17]. It is also shown in Fig. 5 that at $P_{in} = -5\,\mathrm{dBm}$ the cell produces an output power higher than $4.3\,\mathrm{dBm}$ from $280\,\mathrm{GHz}$ up to $308\,\mathrm{GHz}$ (RBW = $9.5\,\%$). In this frequency range the PAE is higher than $3.3\,\%$ and the 4-dB compressed gain achieves values better than $9\,\mathrm{dB}$. Fig. 5 also shows a very good agreement between simulation and measurement results.

The output power, gain and PAE results for different input power levels at $292\,\mathrm{GHz}$ are presented in Fig. 6. These results have been obtained by applying the following DC bias voltages: $V_G = 0.1\,\mathrm{V}$, $V_{CA1} = 1.23\,\mathrm{V}$, $V_{CA2} = 2.36\,\mathrm{V}$ and $V_D = 3.4\,\mathrm{V}$. In this case, the output power is increased, with a maximum of $6.2\,\mathrm{dBm}$ for $P_{in} = -4\,\mathrm{dBm}$ at $292\,\mathrm{GHz}$. This input power produces also a good PAE performance ($5.1\,\%$) and a high gain of $10.2\,\mathrm{dB}$.

Compared to the triple stacked-FET cell demonstrated in [8], which exhibits a small-signal RBW of $35\,\%$, an output power of $3.5\,\mathrm{dBm}$ at $280\,\mathrm{GHz}$ in its 2-dB compression point and a PAE of $3.2\,\%$. The PA cell presented in this work enhances bandwidth, output power and efficiency performance.

IV. 240 GHz Parallel Stacked-FET MPA

According to the theory explained in [18], by using the stacked-FET topology, the limit of the maximum number of transistors (n_{max}) after which one the output power does not further improves depends on the operation frequency (f) of the circuit and the f_T of the concrete FET technology employed. Therefore, for the $35\,\mathrm{nm}$ mHEMT technology, a device operating at $240\,\mathrm{GHz}$ presents the following limit of transistor number:

$$n_{max} \leq \left[ln\left(1 + \frac{f}{f_T}\right)\right]^{(-1)} \Rightarrow n_{max} \leq 2.74. \qquad (1)$$

Thus, the maximum number of transistors in a stacked-FET configuration is limited to three. When the output power provided by a series or stacked connection is not sufficient for a certain application, parallel combining techniques can be used [19].

That approach is investigated by implementing a two stage MPA. The in-phase combiner that is used is the Dolph-Chebyshev structure, due to the fact that it allows a combination of four branches in parallel with low net losses ($1.2\,\mathrm{dB}$ per Dolph combiner at $240\,\mathrm{GHz}$), so that the output power can be nearly ideally increased by a factor of four ($6\,\mathrm{dB}$).

A. Design topology

The schematic diagrams of the processed circuit based on series-connected transistors are shown in Figs. 7 and 8. In Fig. 7 the whole design is sketched. The last stage is based

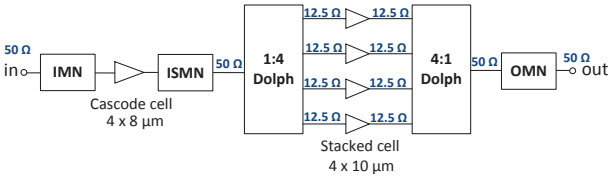

Fig. 7. Schematic diagram of the cascode-stacked PA by using Dolph-Chebyshev (1:4) divider/combiner.

on Dolph-Chebyshev divider/combiner structures and triple-stacked FET cells. It is seen that the inputs of the stacked-FET cells are matched to $R_{in} = 12.5\,\Omega$ because the combiner transforms the input impedance of $50\,\Omega$ to $12.5\,\Omega$ for each output branch. Similarly, the outputs of the stacked-FET cells are matched to $R_{out} = 12.5\,\Omega$. The interstage and output matching networks (ISMN and OMN) are needed to bias the first CS stage at the gate (V_G) and the last common gate-like (CG-like) FET at the drain (V_D). In Fig. 8, the triple-stacked FET cell included in each branch of the parallel structure is drawn. As mentioned before, $R_{in,opt} = R_{L,opt} = 12.5\,\Omega$, that has been achieved throughout the input and output matching networks composed by the parallel capacitors C_{pi} and C_{po}, and $50\,\Omega$ lines. Open/shorted stubs are not included because the lack of space between the parallel branches make them difficult to layout. The gate capacitors at the CG-like FETs are decisive for the stability and the gate voltage swing to fulfill the stacked-FET topology. Besides that, in this case they play also an essential role in the gate biasing for the different branches, that has been performed by connecting the gate bus of the CG-like capacitors in parallel through C_1 and C_2.

As shown in Fig. 7, the MPA test structure includes a cascode pre-amplifier stage (composed of a CS and a CG-FET with a line in between). In particular, this stage drives the last stacked-FET stage into saturation by increasing the linear gain of the amplifier. The UGW of the cascode cell is smaller than that of the stacked cells ($32\,\mu\mathrm{m}$ for the cascode, and $40\,\mu\mathrm{m}$ per stacked-FET) with the aim of providing high gain. Each of the transistors in the single stacked-FET cells has identical size. The same occurs for the cascode cell, where the UGWs of the CS and the CG transistors are the same. This is done to ensure equal current handling capability and prevent one device from being saturated before the other [20].

The associated chip photograph of the manufactured MMIC is shown in Fig. 9, in which RF pads are used and GPPGPPG

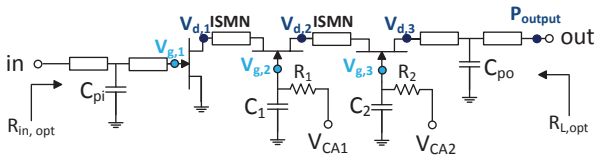

Fig. 8. Schematic of the triple-stacked FET power cell included between the Dolph-Chebyshev (1:4) divider and combiner.

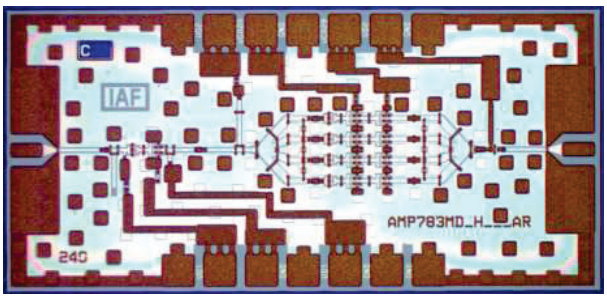

Fig. 9. Chip photograph of the 240 GHz mHEMT MPA. The die area is $1.5 \times 0.75\ \mathrm{mm}^2$.

(G for ground and P for power) DC pads are placed at the top and bottom side of the MMIC to provide the correct bias for class-A operation. In any stacked-FET topology, the DC drain voltage of the last FET should be N times the one of the CS device, N being the number of devices in the series connection. Furthermore, by choosing also the right gate bias, the supply voltage is equally distributed among all the transistors avoiding instabilities, without exceeding the FET breakdown voltages (the maximum is $N \times BV_{DS}$) and obtaining high RF output power [21].

In Fig. 10 the simulated representative gate and drain voltage waveforms of the single cell stacked-FET structure at the center frequency of 240 GHz are shown. The DC drain voltage applied is $V_{D2} = 3.9\,\mathrm{V}$ so that with each FET of the triple-stacked configuration a DC drain voltage of 1.3 V is supplied. The cascode pre-amplifier configuration is designed with the same DC bias conditions, so that, as $V_{D1} = 2.6\,\mathrm{V}$, a voltage of 1.3 V is supplied separately to the CS- and to the CG-transistors. When applying an equally distributed DC voltage to all the devices, the drain-to-ground RF voltage swings of the transistors should be also homogeneous and fulfill the following condition to avoid the breakdown of the FETs [4]:

$$V_{d,k} \cong \frac{k}{k-1} \cdot V_{d,k-1}. \tag{2}$$

The simulated gate peak-to-peak voltage swings for each

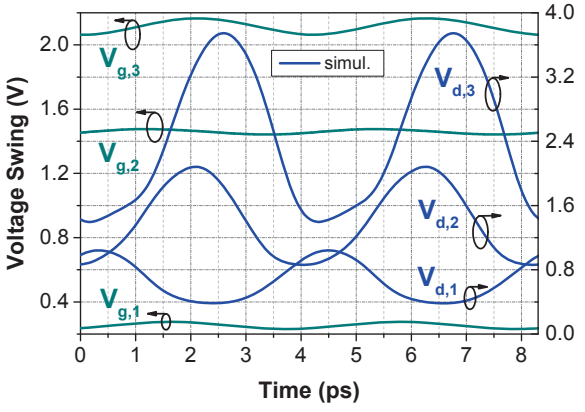

Fig. 10. Simulated gate and drain voltage waveforms for the CS and CG-like transistors at 240 GHz, for $V_{D2} = 3.9\,\mathrm{V}$, $V_{D1} = 2.6\,\mathrm{V}$ and $V_{G1} = V_{G2} = 0.1\,\mathrm{V}$, $V_{CA} = 1.4\,\mathrm{V}$, $V_{CA1} = 1.43\,\mathrm{V}$, $V_{CA2} = 2.74\,\mathrm{V}$

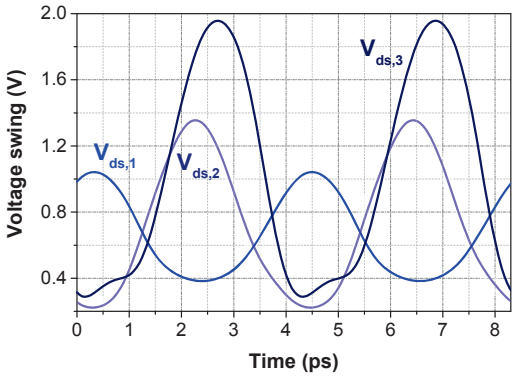

Fig. 11. Simulated drain-gate voltage waveforms for the CS and CG-like transistors at 240 GHz, for $V_{D2} = 3.9\,\mathrm{V}$, $V_{D1} = 2.6\,\mathrm{V}$ and $V_{G1} = V_{G2} = 0.1\,\mathrm{V}$, $V_{CA} = 1.4\,\mathrm{V}$, $V_{CA1} = 1.43\,\mathrm{V}$, $V_{CA2} = 2.74\,\mathrm{V}$

k-th FET ($V_{pp,gk}$) are $V_{pp,g1} = 0.194\,\mathrm{V}$, $V_{pp,g2} = 0.131\,\mathrm{V}$ and $V_{pp,g3} = 0.353\,\mathrm{V}$, as shown in Fig. 10. At the drain the peak-to-peak voltages are higher, so that $V_{pp,d1} = 0.658\,\mathrm{V}$, $V_{pp,d2} = 1.21\,\mathrm{V}$ and $V_{pp,d3} = 2.34\,\mathrm{V}$. It can be observed from these values that $V_{d,2} = 2 \cdot V_{d,1}$ (as depicted by Eq. 2) and $V_{d,3} = 2 \cdot V_{d,2}$. Although according to Eq. 2, $V_{pp,d3} = \frac{3}{2} \cdot V_{pp,d2} = 1.815\,\mathrm{V}$, that value is deliberately exceeded to obtain a higher output power, but it has to be verified that the third transistor is not driven into breakdown at this operating condition.

The simulated drain-gate voltage waveforms at the center frequency of 240 GHz are shown in Fig. 11. It is observed that the waveforms of the two CG transistors ($V_{dg,2}$ and $V_{dg,2}$) are in phase and are almost sinusoidal, except for a slightly higher harmonic content that is visible in $V_{dg,3}$ due to the device non-linearity [22]. The gate-drain peak-to-peak voltages for each of the FETs are $V_{pp,dg1} = 0.785\,\mathrm{V}$, $V_{pp,dg2} = 1.124\,\mathrm{V}$ and $V_{pp,dg3} = 2.019\,\mathrm{V}$. As mentioned in [20], the gate-drain bias is a critical parameter that can drive the amplifier into breakdown. In this case it is seen in Fig. 11 that the maximum drain-source bias of the last FET does not exceed the off-state

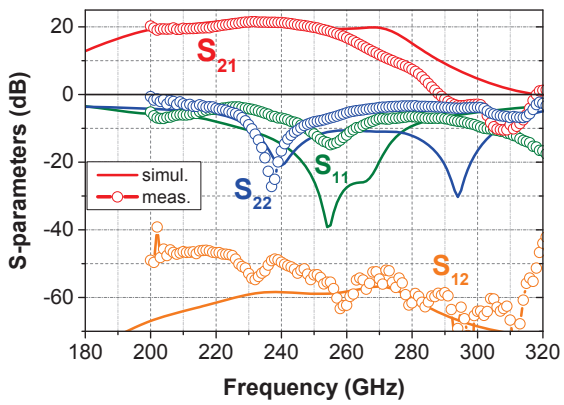

Fig. 12. Small-signal measurement (line with circle symbols) and simulation (straight line) results for the processed MMIC.

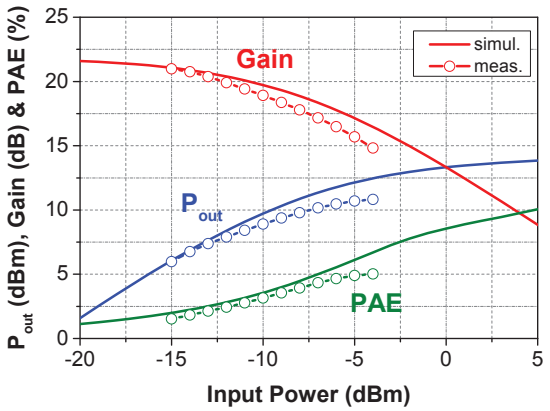

Fig. 13. Large-signal measurement (line with circle symbols) and simulated (straight) results at 240 GHz of the processed 4-parallel stacked MPA.

breakdown of 2 V.

Due to the in-phase behavior of the gate-source, drain-source and gate-drain voltage waveform at the CG-FETs as well as an RF voltage swing at the upper drain FET that is around $N = 3$ times the RF drain voltage of a single FET, it is concluded that the MPA behaves similarly to a stacked-FET topology. Concretely, the CS and the first CG of the stacked-FET are designed to follow a cascode configuration to obtain high gain, while the third transistor is a CG that transfers not just gain, but also power, and generates the final output power from the MPA. As the stacked stage behaves partly as a cascode, a stage ratio of 1:5 (32 µm driving the $4 \times 40\mu\text{m} = 160$ µm) is feasible. Otherwise the cascode will saturate the last stage too early.

B. Measurement results

The small- and large-signal parameters of this MMIC were also measured. The S-parameters shown in Fig. 12 are obtained when biasing the MPA with the DC voltages as indicated in the caption of Fig. 10. At 231 GHz a peak linear gain of $S_{21} = 21.5\,\text{dB}$ is measured and it results in a 3-dB RBW of 24.2 % (ranging from 200 to 255 GHz). The

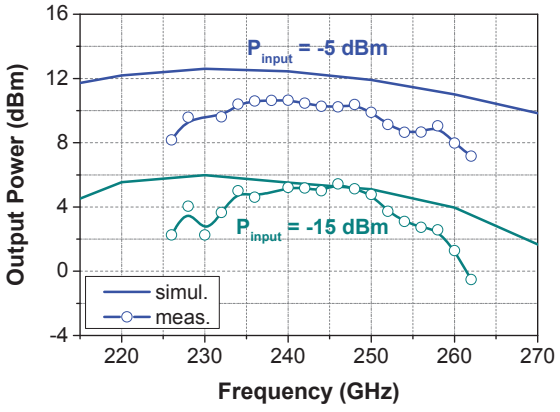

Fig. 14. Simulated and measured output power sweep for two input power levels.

S-parameters were not measured at lower frequencies than 200 GHz. However, at 200 GHz the gain is still high where still high, so that the bandwidth is expected to be even wider.

The measured and simulated output power, PAE and gain versus input power for the PA MMIC are shown in Fig. 13. This amplifier has achieved an output power of 10.8 dBm at 240 GHz when the linear gain is compressed by 6 dB, with an associated gain of 14.8 dB, so that even higher output power levels could be achieved. The PAE is high taking into account the high losses at these frequencies, demonstrating a maximum value of 5.02 %. To the authors' best knowledge, this is the highest PAE obtained at this frequency within a GaAs mHEMT technology. This is due to the fact that as the upper FET behaves as a stacked-FET, the resulting PAE (as well as output power) is better that the one that would be obtained by a triple cascode topology [23].

The frequency sweep graph for two input power levels ($P_{input} = -15\,\text{dBm}$ and $-5\,\text{dBm}$) is shown in Fig. 14. For $P_{in} = -5\,\text{dBm}$ it is observed that an output power level exceeding 10.4 dBm is measured between 234 and 248 GHz, which represents a 6 % power RBW. Furthermore, the MMIC achieves an output power higher than 9 dBm from 228 GHz to 258 GHz, which is equivalent to a 12.3 % power RBW.

C. Comparison with the state of the art

In Tab. II a comparison of the reported PA MMICs operating near 240 GHz is included. The maximum output power is achieved in [24]-[26] because of the higher breakdown voltages that those technologies provide, so that a higher DC drain voltage can be applied (2 V for [25], in comparison to 1.3 V in this work). When comparing the processed amplifier with the MMICs fabricated using the same technology (GaAs mHEMT), it is observed that it achieves the highest output power of 10.8 dBm with a high associated compressed gain of 15 dB. [27] achieves a higher output power density due to the use of two-finger transistors with smaller TGW (80 µm versus 160 µm). The combination through the Dolph-Chebyshev structures reduces the power density of a single ended amplifier from 104 mW/mmto 75.1 mW/mm. Besides that, the PAE in this work has been improved in comparison to the results obtained by [27] and [17] and one of the highest bandwidths is obtained (at least 24.2 %), thanks to the stacked-FET configuration and the three-metallization layer process. It is expected that this 3-dB RBW is even higher. As shown in fig. 12, the MMIC has only been characterized in H-band (200 GHz – 330 GHz), but the 3-dB RBW may also extend down to frequencies below 200 GHz.

V. Conclusion

The first triple stacked-FET power cell at 0.3 THz has been implemented demonstrating an ultra-broadband performance in H-band (with a 3-dB RBW of 47.3 %) and an output power level of 5.4 dBm for a 3-dB compressed gain, outperforming the previous results in [8]. Additionally, by parallel combining of four triple stacked-FET cells, the requirements of high output power and high bandwidth have been achieved using

TABLE II
COMPARISON OF MMIC PAS OPERATING AROUND 240 GHz USING III-V SEMICONDUCTOR PROCESSES.

Technology †	250 nm InP HBT	50 nm InP HEMT *	250 nm InP HBT	35 nm GaAs mHEMT	50 nm GaAs mHEMT	35 nm GaAs mHEMT
Frequency (GHz)	235	225	244	250	260	240
P_{out} **(dBm)**	21	18.8	20	10	6.2	> 10.8
Power density +	1.31	79	0.013	125	104	75.1
Linear gain (dB)	26.7	17	25	32.5	29.2	21.5
BW (RBW)	46.2 GHz (12.5 %)	20 GHz (9.3 %)	50 GHz (21.7 %)	17 GHz (6.8 %)	69 GHz (29 %)	55 GHz (> 24.2 %)
4 **Comp.gain (dB)**	10	11	17	18	8	15
PAE (%)	2.02	5.1	3.4 %	2.9	3.2	5
$V_{d,DC}$ **(V) per FET**	1.98	2	2.5 V	1.1	1.6	1.3
Reference	[24]	[25]	[26]	[27]	[17]	This work

* Calculated values considering losses of waveguide module integration.
† Values referred to emitter area for HBT and gate length for HEMT.
+ Output power density is measured in $mW/\mu\mathrm{m}^2$ for [24] and in mW/mm for the rest.

a 35 nm GaAs mHEMT technology with a three-layer metallization process.

To the best of the author's knowledge, parallel combination of stacked-FET (>2 transistors) cells for PA implementation has only been demonstrated up to W-band [12], whereas the only publication about triple stacked-FET PA cells beyond W-band up to now is [8], with single operating cells working at 240 and 280 GHz. Although, in general, a broadband power amplifier as in [17] does not produce high output power (just 6.2 dBm in this case), and to enhance output power usually narrowband MMICs are produced ([27]), in this case both requirements have been fulfilled. With a small-signal 3-dB RBW higher than 24.2 %, this MMIC achieves a peak output power of 10.8 dBm at 240 GHz, a peak PAE of 5.02 % and output power levels higher than 9 dBm for a RBW of 12.3 %. These results reveal the potential of the stacking approach for RF power generation even at (sub-) mmW frequencies.

ACKNOWLEDGMENT

The authors would like to thank their colleagues at the Fraunhofer IAF for all the help, advice and for their excellent contribution done during the model development as well as epitaxial growth and wafer processing. Furthermore, they would like to thank to Dr. J. Kühn and Dr. M. Schlechtweg too for their continuous support throughout this work.

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