THREE-LEVEL THREE-PHASE QUASI-Z-SOURCE NEUTRAL-POINT-CLAMPED INVERTER WITH NOVEL MODULATION TECHNIQUE FOR PHOTOVOLTAIC APPLICATION

Oleksandr Husev (corresponding author)[1,3], Carlos Roncero-Clemente[2], Enrique Romero-Cadaval[2], Dmitri Vinnikov[1], Tanel Jalakas[1]

[1]Department of Electrical Engineering, Tallinn University of Technology, Ehitajate tee 5, 19086, Tallinn, Estonia, +37257868042, e-mail: oleksandr.husev@ieee.org

[2]Power Electrical and Electronics Systems (Pe&eS), University of Extremadura, Avda. Elvas s/n, 06006, Badajoz, Spain;

[3]Department of Biomedical Radioelectronic Apparatus and Systems, Chernihiv National University of Technology, Shevchenko str. 95, 14027, Chernihiv, Ukraine

Abstract— This paper presents a three-phase three-level neutral-point-clamped quasi-Z-source inverter as a novel solution for photovoltaic applications. The topology was derived by combining properties of the quasi-Z-source networks with those of three-level neutral-point-clamped inverters. A case study system, a steady state analysis and a novel special modulation technique for shoot-through states distribution during the whole operation period are described. Component design guidelines for a three-phase system are presented. All theoretical findings have been confirmed by simulation and experimental results. A "full SiC" experimental prototype was developed. A comprehensive study of the converter's efficiency is provided.

Key words — three-level inverter, quasi-Z-source network, shoot-through states, photovoltaic system.

Abbreviations

3P 3L NPC qZSI - three-phase three-level neutral-point-clamped quasi-Z-source inverter

CCM - continuous conduction mode

LS-PWM - level shifted PWM

MCBC - maximum constant boost control

MBC - maximum boost control

MPP - maximum power point

MSVMBC - modified space vector modulation maximum boost control

PV – photovoltaic

PWM - pulse width modulation

qZSI - quasi-Z-source inverter

SBC - simple boost control

SVM - space vector modulation

THD – total harmonic distortion

VSI - voltage source inverter

ZSI - Z-source inverter

1. Introduction

Shortage of energy resources is a current concern. At the same time, renewable energy sources have become extremely popular. Photovoltaics (PV), wind turbines and fuel cells are most popular among renewable sources. By the end of 2013, the installed capacity of wind and solar PV power generation reached 318 GW and 139 GW, correspondingly [1].

Each source has its pros and cons. A common feature lies in their unstable operation that depends on many parameters. The main target of the power electronics converters is to provide stable output voltage despite unstable input parameters at the highest efficiency, cost and size optimization. As a result, many new types of interface converters have been developed. In PV applications, the main drawback in the present solutions lies in the narrow range of the input voltage regulation, cost and size optimization. Different solutions have been proposed [2]-[6].

Intermediate voltage boost dc-dc converters are used to overcome the narrow range of the input voltage regulation. At the same time, topologically, this solution is more complex and harder to control because of the two-stage power conversion. Another solution is based on the intermediate impedance-source network, classified as a single-stage energy conversion solution. Several review papers have been published [7]-[9].

This paper proposes a novel solution based on the Three-Phase Three-Level Neutral-Point-Clamped Quasi-Z-Source Inverter (3P 3L NPC qZSI) illustrated in Fig.1. The

general concept of the single-phase 3L NPC qZSI is described in [10] and experimentally verified in [11]. The three-phase 3L NPC qZSI is intended for applications that require a wide operation range of the input voltage along with the Continuous Conduction Mode (CCM) of the input current. It is important to note that even though the system presented in Fig. 1 includes the PV panels ground capacitance [12] and the LCL filter is directly connected to the dc bus central point since it attenuates the high frequency components of the voltage across the PV parasitic capacitance [13], problematics related to leakage current paths, common-mode voltage and radiated electromagnetic emissions are considered out of the scope of this paper. Once this topology and modulation method would be validated, further works will deal with this problematic and its possible solutions [14]-[15] in PV inverter transformer-less applications.

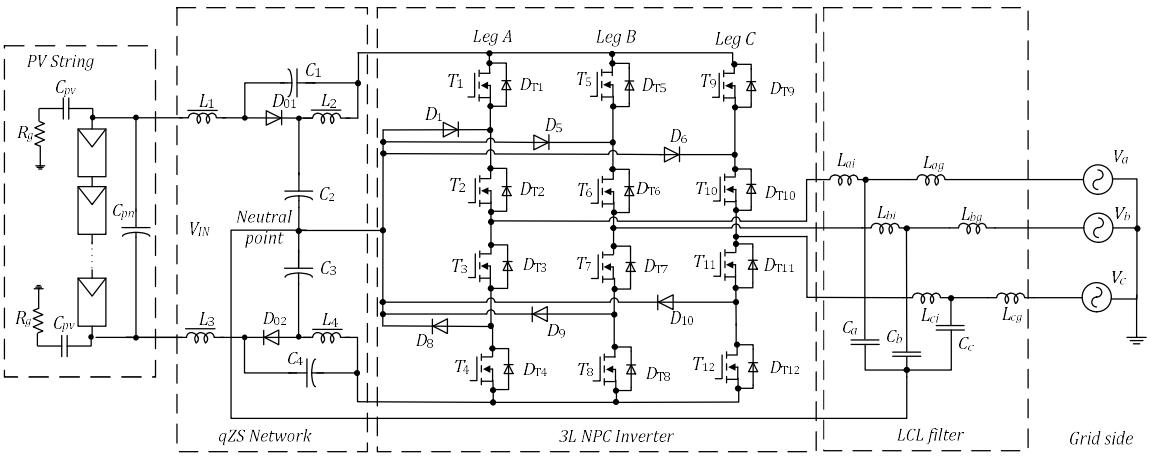


Fig. 1. Proposed novel 3P 3L NPC qZSI.

1.1 Case study system description

A PV installation of 18 serial panels is a voltage source for the converter topology. Fig. 2 shows the resulting input PV curve. It is well known that solar panels provide limited voltage and current that follows an exponential *I-V* curve.

Several models have been reported for solar panel simulations [16]-[20]. A mathematical model based on the *I-V* exponential curves and parameters provided in the manufacturer's datasheet is used to simulate the PV array. Its mathematical foundation is detailed in [21]. Table 1 presents main specifications of a commercial solar module (LDK 185D-24(s)) [22].

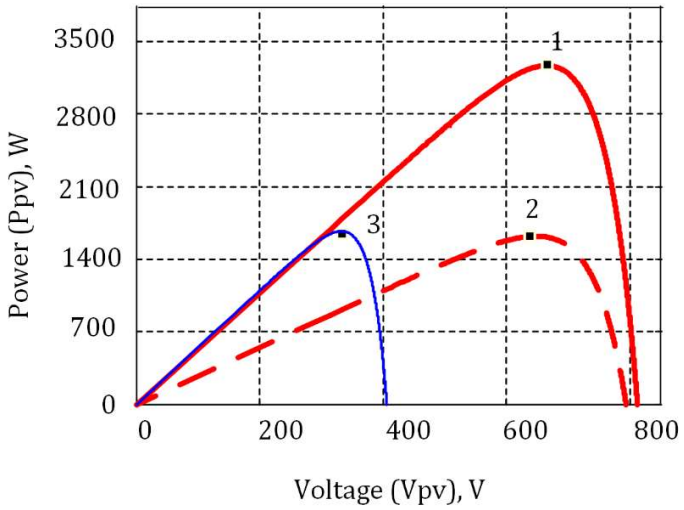


Fig. 2. PV curve of the case study.

Several working points are marked in Fig. 2. Even low but equally distributed solar irradiation does not require extremely high boost (point 2). High boost capabilities are demanded in a partly shadowed mode where only some of the panels in the array have lower irradiation (point 3). It can be seen that the Maximum Power Point (MPP) with maximum irradiation corresponds to the Voltage Source Inverter (VSI) mode that requires no voltage boost feature (point 1).

Table 1
Main parameters from the panel datasheet [18].

Parameters	Unit	Value
Nominal output power (Pmax)	W	185
Voltage at Pmax	V	36.9
Current at Pmax	A	5.02
Open circuit voltage (Voc)	V	45.1
Short circuit current (Isc)	A	5.48

Section 2 below describes the proposed solution in detail. Section 3 explains the new modulation technique developed for such applications. Section 4 presents the results of simulation and experiment verification.

2. Description of the proposed solar inverter

The Quasi-Z-Source Inverters (qZSIs) proposed in [23], [24] were intended to further improve the traditional Z-Source Inverters (ZSI).

Besides the advantages inherited from the ZSIs [23], the qZSIs have reduced passive component ratings and continuous input current. In contrast to the two-level VSI, the 3L NPC inverter has many advantages, such as lower voltage stress across semiconductors, lower required blocking voltage capability, decreased dv/dt, higher switching frequency due to the lower switching losses, and better harmonic performance [24], [25]. In addition, several papers [26]-[28] have reported that 3L topology has better elimination capability of the common mode leakage current, and as a result, no additional common mode filters are required.

2.1 Operation principle and steady state analysis of the proposed topology

Each branch of the inverter has three output voltage levels: *0, ± V_{DC}/2*, where V_{DC} is the peak of the dc-link voltage. The operating period of the 3P 3L-NPC qZSI in the CCM may be divided into several time intervals. Table 2 shows all possible switching states of the transistors in the topology. Taking into account that the inverter has three branches, each of which may have three states, altogether 27 states are possible. At the same time, in a traditional three-phase system, states where all branches have positive or negative output voltage values are excluded.

Table 2
Switching states of transistors in 3P 3L NPC qZSI.

switching states	Mode	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}
1	active	1	1	0	0	0	1	1	0	0	1	1	0
2		1	1	0	0	1	1	0	0	0	1	1	0
3		1	1	0	0	0	1	1	0	1	1	0	0
4		1	1	0	0	0	0	1	1	0	1	1	0
5		1	1	0	0	0	1	1	0	0	0	1	1
6		1	1	0	0	1	1	0	0	0	0	1	1
7		1	1	0	0	0	0	1	1	1	1	0	0
8		1	1	0	0	0	0	1	1	0	0	1	1
9		0	1	1	0	1	1	0	0	1	1	0	0
10		0	1	1	0	1	1	0	0	0	1	1	0
11		0	1	1	0	0	1	1	0	1	1	0	0
12		0	1	1	0	0	0	1	1	0	1	1	0
13		0	1	1	0	0	1	1	0	0	0	1	1
14		0	1	1	0	1	1	0	0	0	0	1	1
15		0	1	1	0	0	0	1	1	1	1	0	0
16		0	1	1	0	0	0	1	1	0	0	1	1
17		0	0	1	1	0	1	1	0	0	1	1	0
18		0	0	1	1	1	1	0	0	0	1	1	0
19		0	0	1	1	0	1	1	0	1	1	0	0
20		0	0	1	1	0	0	1	1	0	1	1	0
21		0	0	1	1	0	1	1	0	0	0	1	1
22		0	0	1	1	1	1	0	0	0	0	1	1

23		0	0	1	1	0	0	1	1	1	1	0	0
24		0	0	1	1	1	1	0	0	1	1	0	0
25	zero	0	1	1	0	0	1	1	0	0	1	1	0
26	shoot-through	1	1	1	1	1	1	1	1	1	1	1	1

Finally, due to the qZS network, another shoot-through state is added when all the transistors are conducting. During this state, energy is accumulated in the inductors and is transferred to the capacitors and output load within other states. As a result, the peak dc-link voltage is regulated only by adjusting the shoot-through duty cycle. This switching state is excluded for traditional VSIs because it causes a short circuit of the dc-link capacitors.

Considering all the time intervals presented above, the behavior of the qZS network can be represented by means of three equivalent circuits shown in Fig. 3. Accordingly, all the switching states can be separated into three main modes: zero state (Fig. 3 a), active states (Fig. 3 b) and shoot-through state (Fig. 3 c) that can be applied within the zero state. However, such approach is valid for a three-phase symmetric system.

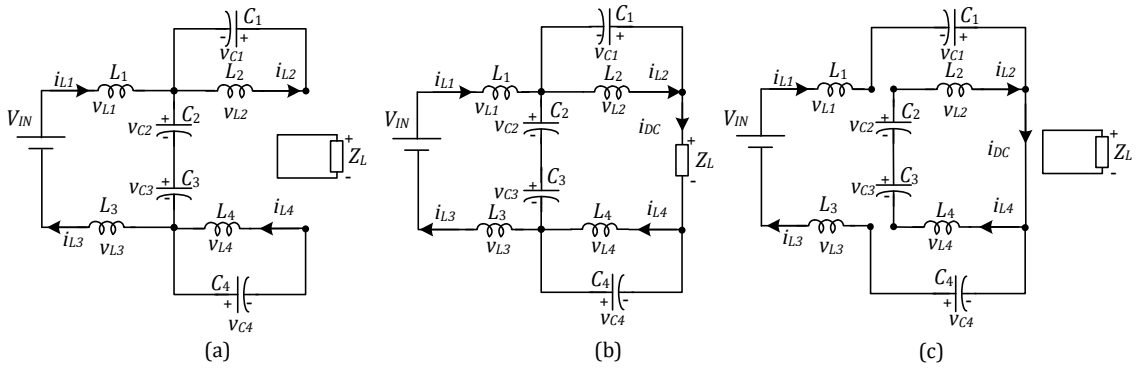


Fig. 3. Equivalent circuits of the 3P 3L-NPC qZSI: zero state (a), active state (b), shoot-through state (c).

To estimate values of the passive components and recommend guidelines for semiconductor selection, the steady state analysis was performed. In the analysis, the voltage balance across the inductors and current balance across the capacitors were used. The operating period of the converter in the CCM is represented as

$$\frac{t_A}{T}+\frac{t_Z}{T}+\frac{t_S}{T}=D_A+D_Z+D_S=1, \quad (1)$$

where D_A is the duty cycle of the active state, D_Z is the duty cycle of the zero state, and D_S is the duty cycle of the shoot-through state. T is a fundamental switching period. The sum of the capacitor voltages defines the peak of the dc-link voltage:

$$V_{DC}=V_{C1}+V_{C2}+V_{C3}+V_{C4}, \quad (2)$$

where V_{C1}, V_{C2}, V_{C3}, V_{C4} are average voltages across the capacitors over one period. Taking into account that the qZS network is symmetric, it was assumed that $L_1=L_3$, $L_2=L_4$ and $C_1=C_4$, $C_2=C_3$. Accordingly, voltages are $v_{L1}=v_{L3}$, $v_{L2}=v_{L4}$, and $V_{C1}=V_{C4}$, $V_{C2}=V_{C3}$. The voltage on the capacitors can be found from the voltage balance of the inductors over one switching period. Taking into account the conditions above, the voltages across the capacitors can be obtained as:

$$V_{C1}=V_{C4}=\frac{D_S\ V_{IN}}{2-4\ D_S}, \quad (3)$$

$$V_{C2}=V_{C3}=\frac{V_{IN}\ \left(1-D_S\right)}{2-4\ D_S}. \quad (4)$$

The final equation for the boost factor is obtained:

$$B=\frac{V_{DC}}{V_{IN}}=\frac{V_{C1}+V_{C2}+V_{C3}+V_{C4}}{V_{IN}}=\frac{1}{1-2\ D_S}. \quad (5)$$

Since the converter must operate both in the islanding mode and in the grid connected mode, the output phase to the neutral point voltage RMS value has to be maintained around V_{OUT} =230 V. In the three-phase system, the phase to the neutral voltage is derived:

$$V_{OUT} = M \frac{V_{DC}}{2\sqrt{2}} = M \frac{V_{IN}}{2\sqrt{2}\left(1-2D_S\right)}. \quad (6)$$

Since the modulation index M has to be in a range of $M \leq 1-D_S$ and the output voltage is constant, dependences between the input voltage V_{IN} and the shoot-through duty cycle D_S are

$$V_{OUT} = \frac{\left(1-D_S\right) V_{IN}}{2\sqrt{2}\left(1-2D_S\right)}. \quad (7)$$

2.2 qZS-network estimation

In a real system, the operating waveforms of the 3P 3L-NPC qZSI are distorted by the ripple, as shown in Fig. 4. At a symmetric three-phase load, the input current has high frequency ripple, which is connected with the high frequency shoot-through duty cycle switching.

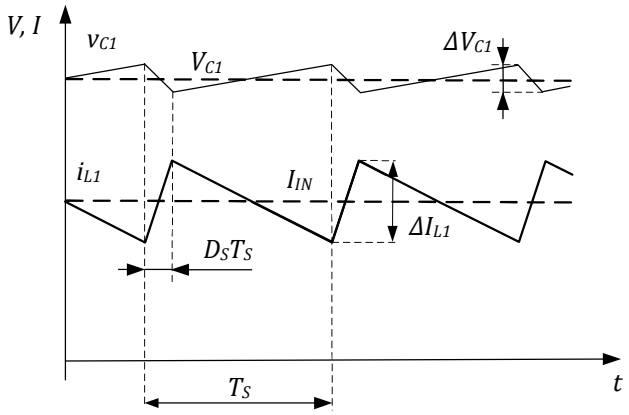


Fig. 4. Sketch of the input current ripple and voltage ripple on the capacitors.

The rising speed depends on the inductor and capacitor voltages. It means that the high frequency ripple of the current can be found from the shoot-through interval:

$$\Delta I_{L1} = \int_0^{T_S \; D_S} \frac{di_{L1}}{dt} \quad dt = \int_0^{T_S \; D_S} \left(\frac{V_{IN} + V_{C1} + V_{C4}}{2 \quad L}\right) \quad dt = \left(\frac{V_{IN} + V_{C1} + V_{C4}}{2 \quad L}\right) \quad T_S \quad D_S , \tag{8}$$

where T_S is the switching period. In order to maintain the CCM operation of the converter, the input current ripple ΔI_{L1} should be smaller than the average input current I_{IN}. The average input current can be defined from the power balance:

$$P_{IN} = V_{IN} \quad I_{IN} = P_{OUT} . \tag{9}$$

At the CCM condition with the predefined current ripple, from Eqs. (3), (8) and (9), it can be written as:

$$K_L = \frac{\Delta I_{L1}}{I_{IN}} = \frac{4 \quad V^2{}_{OUT} \quad (1-2 \quad D_S)}{(1-D_S) \quad L \quad P_{OUT}} T_S \quad D_S , \tag{10}$$

The minimum value of the inductance in order to guarantee a ripple in the inductor current to maintain the CCM operation of the proposed inverter can be defined as:

$$L \geq \frac{4 \quad V^2{}_{OUT} \quad (1-2 \quad D_S)}{(1-D_S) \quad K_L \quad P_{OUT}} T_S \quad D_S . \tag{11}$$

. Capacitor voltage ripple can be defined in a similar way:

$$\Delta V_{C1} = \Delta V_{C4} = \frac{1}{C_1} \int_0^{D_S T_S} i_C(t)dt = \frac{1}{C_1} \int_0^{D_S T_S} i_{L1}(t)dt . \tag{12}$$

Since the inductance current has linear character, expression (12) can be simplified:

$$\Delta V_{C1} = \Delta V_{C4} = \frac{1}{C_1} \quad I_{IN} \quad T_S \quad D_S . \tag{13}$$

The required value of the capacitance of C_1 to maintain the desired voltage ripple factor K_{C1} can be obtained as:

$$K_{C1} = \frac{\Delta V_{C1}}{V_{C1}} = \frac{T_S \quad P_{OUT} \quad (1 - D_S)^2}{4 \quad C_1 \quad V_{OUT}^2 \quad (1 - 2D_S)}, \tag{14}$$

As a result, the capacitor can be calculated as:

$$C_1 = C_4 \geq \frac{T_S \quad P_{OUT} \quad (1 - D_S)^2}{4 \quad K_C \quad V_{OUT}^2 \quad (1 - 2D_S)}. \tag{15}$$

Capacitor voltage ripple on the capacitors C_2 and C_3 can be defined in a similar way:

$$\Delta V_{C2} = \Delta V_{C3} = \frac{1}{C_2} \int_0^{D_S T_S} i_C(t)\,dt = \frac{1}{C_2} \int_0^{D_S T_S} i_{L2}(t)\,dt \ . \tag{16}$$

Taking into account that inductors' currents are equal, the required value of the capacitance of C_2 and C_3 to maintain the desired voltage ripple factor K_{C2} can be obtained as:

$$K_{C2} \geq \frac{T_S \quad P_{OUT} \quad (1 - D_S) \quad D_S}{4 \quad C_2 \quad V_{OUT}^2 \quad (1 - 2D_S)}. \tag{17}$$

Finally, capacitance values for capacitors C_2, C_3 are defined as:

$$C_2 = C_3 \geq \frac{T_S \quad P_{OUT} \quad (1 - D_S) \quad D_S}{4 \quad K_{C2} \quad V_{OUT}^2 \quad (1 - 2D_S)}. \tag{18}$$

To demonstrate how the input voltage range influences the passive elements of the qZS network, from expressions (7), (11), (15) , and (18), it can be written as:

$$L \geq \frac{2 \quad T_S \quad V_{OUT} \quad V_{IN}}{\sqrt{2} \quad K_L \quad P_{OUT}} \quad \frac{2\sqrt{2} \quad V_{OUT} - V_{IN}}{4\sqrt{2} \quad V_{OUT} - V_{IN}} \ , \tag{19}$$

$$C_1 = C_4 \geq \frac{2 \quad T_S \quad P_{OUT}}{K_{C1} \quad V_{IN}} \quad \frac{1}{4\sqrt{2} \quad V_{OUT} - V_{IN}}, \tag{20}$$

$$C_2 = C_3 \geq \frac{T_S \quad P_{OUT}}{\sqrt{2} \quad K_{C2} \quad V_{OUT} \quad V_{IN}} \cdot \frac{2\sqrt{2} \quad V_{OUT} - V_{IN}}{4\sqrt{2} \quad V_{OUT} - V_{IN}} \quad . \tag{21}$$

Fig. 5 illustrates the dc-link voltage and values of passive elements as functions of the input voltage.

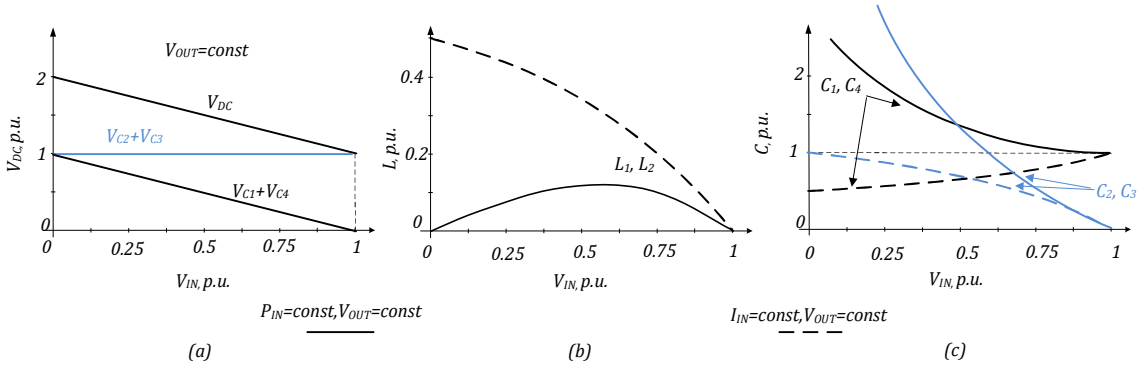


Fig. 5. 3P 3L NPC qZS inverter: dc-link and capacitors voltage (a), inductance (b) and capacitances (c) versus input voltage.

All dependences are presented in the relative units where one voltage unit corresponds to $2\sqrt{2}\cdot V_{OUT}$. Relative units of the passive elements are defined as:

$$L = \frac{4 \quad T_S \quad V_{OUT}^2}{K_L \quad P_{OUT}} = 1 p.u. \tag{22}$$

$$C = \frac{T_S \quad P_{OUT}}{K_C \quad 4 \quad V^2_{OUT}} = 1 p.u. \tag{23}$$

where $K_C = K_{C1} = K_{C2}$ is a voltage ripple factor on the capacitors. It should be noted that in the buck mode, a converter works like a traditional VSI and an impedance network is not involved in its operation. Therefore, only the boost mode is considered in the figure. Solid lines show passive element values as a function of the input voltage under constant input power. At the same time, dotted lines illustrate similar dependences under constant input current that correspond to the PV curve. This figure shows that

the highest inductance corresponds to the lowest input voltage. The same conclusion applies to the capacitors.

As a result, passive component values necessary to provide predefined voltage and current quality can be estimated.

2.3 Selection of semiconductors

Voltage stress is one of the key parameters for semiconductor selection. Voltage stress on the transistors, as well as on the diodes, is equal to half the dc-link voltage. As shown above and illustrated in Fig. 5 a, the dc-link voltage depends on the input voltage:

$$V_{DC} = 4\sqrt{2} \quad V_{OUT} - V_{IN}. \tag{24}$$

Similarly, voltage on the capacitors that defines the dc-link voltage can be derived:

$$V_{C1} = V_{C4} = \sqrt{2} \quad V_{OUT} - \frac{V_{IN}}{2}. \tag{25}$$

$$V_{C2} = V_{C3} = \sqrt{2} \quad V_{OUT}. \tag{26}$$

The main conclusion from the presented figure is that higher dc-link voltages correspond to the smallest input voltage. Thus, in order to provide the input voltage range from 300 V up to 800 V, semiconductors must withstand the dc-link voltage in a range of 650 V - 1000 V. It means that the maximum voltage stress on the transistors and on all the diodes is equal to 500 V (half the dc-link voltage) plus the switching spike. At the same time, it is evident that the sum of the capacitor voltage $V_{C2}+V_{C3}$ is constant in the boost mode and can be used like a controlled value in a closed loop system. It should be mentioned that in the three-phase topology without the neutral

point dc-link voltage, capacitor voltage can be reduced by means of third harmonic injections.

There are several appropriate semiconductor solutions. Classical IGBT with a 1200 V blocking voltage can be used. The main advantage of this solution is its reliability. The drawback lies in a low switching frequency that forces use of larger passive elements. Recently, MOSFETs based on SiC have appeared as a new family of fast high-voltage switches. Derived from experimental investigations [6], [11] of the dc-dc and dc-ac converters based on the qZS network, it can be concluded that out of all solutions for the qZS diode, only Shottky diodes suit. Because of relatively high voltage, SiC based Shottky diodes can be used.

3. Special shoot-through modulation technique

3.1 Review of existing strategies

Several modulation techniques or shoot-through control methods for the three-phase two-level Z-source inverters have been reported [29]-[36]. These controls are mainly classified as: Simple Boost Control (SBC) [29], Maximum Boost Control (MBC) [30], Maximum Constant Boost Control (MCBC) [31], and Modified Space Vector Modulation Control (MSVMBC) [32]. Among other techniques, they have been used to control converters in such applications as PV solar energy and fuel cells [33], [34].

MCBC has been selected because of its advantages over other control methods. Recent studies have focused on multilevel inverter topologies, modulation and control methods [37]-[44]. As a result, numerous modulation techniques have been proposed, each one featured by its advantages and disadvantages depending on the application.

A good comparison between different modulation methods is presented in [39]. The authors divide the modulation methods for a multilevel converter into two main groups: space vector based methods and carrier based methods. Space Vector Modulation (SVM) or multicarrier Pulse Width Modulation (PWM) is recommended for high frequency applications. In the first case, the reference voltage is represented as a reference vector to be tracked by the power converter. All the discrete possible switching states are matched as state vectors. Finally, the reference voltage is calculated as a linear combination of these state vectors; an averaged output voltage is obtained equal to the reference in one switching period [43]. In the second case, the reference voltage is compared with multiple carriers to control each power switch. In this method, carriers can be arranged in phase shifted or level shifted dispositions.

In addition, a table in [39] shows different levels of applicability of each modulation method to the multilevel inverter topologies reproduced in Table 3.

Table 3
Applicability of modulation methods to multilevel topologies.

Topology	NPC	Flying Capacitor	Cascaded H-Bridge
Modulation method			+
Space vector modulation	+	+	+
Level shifted PWM	+	+	+
Phase shifted PWM	-	+	+
Hybrid modulation	-	-	+
Selective harmonic elimination	+	+	+
Space vector control	0	+	+
Nearest level control	0	+	+

At the same time, several solutions based on the SVM control were designed for 3L ZSIs [45]-[49]. Early developments in switching signal generation for this inverter family

are reported in [45]. To enhance the boost factor, the injection of the third harmonic offset [46] is also added to the reference signals. Further development of SVM techniques was devoted to simplify implementation and to improve the output voltage harmonic spectrum [48], [49].

According to the aforementioned characteristics of each modulation method and their applicability to different topologies, a carrier-based Level Shifted PWM (LS-PWM) in phase disposition with MCBC as a novel solution for the 3P 3L NPC qZSI. This modulation technique is detailed below.

3.2 New carrier-based PWM control strategy

Fig. 6 shows a sketch of the novel LS-PWM in phase disposition with MCBC for the 3P 3L NPC qZS inverter using a frequency modulation index (mf) equal to 4.

Three modulating waves (one per phase) and two triangular carriers (upper $\in$[0,1] and lower $\in$ [-1,0]) were compared to obtain different normal states. Generation of the gate signals for transistors T_1 and T_2 is demonstrated in Fig. 6. It corresponds to the reference signal Ref A. T_3 and T_4 have their complementary state, respectively. The third harmonic injection is commonly used in a three-phase inverter system to increase the modulation index range *M* and in consequence, the system voltage gain range as well. According to [30], the maximum *M* is equal to $2/\sqrt{3}\approx1.15$ when $1/6\approx0.19$ of the third harmonic is injected.

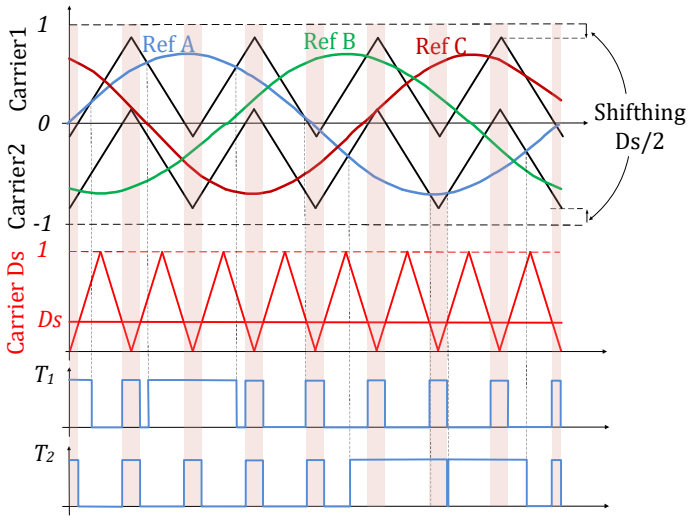


Fig. 6. Sketch of LS-PWM in phase disposition with MCBC.

Another carrier signal ($\in[0,1]$), but at double frequency, is used to generate the shoot-through states (Sst) by means of comparison with the constant value of *Ds*. Operating in this way, uniformly distributed shoot-through states with the constant width during the whole output voltage period are achieved. Due to the insertion of the shoot-through states, the output average phase to neutral voltages is modified, which is necessary to solve the problem. In order to maintain the constant output average voltage, upper and lower carriers are displaced *Ds/2* to assure the reference value.

At the same time, the proposed modulation technique has double switching frequency shoot-through generation, which allows reducing passive components of the impedance networks.

It means that the converter can operate at lower switching frequency under the maximum power point and losses can be minimized. Voltage boost is not required in this point. At the voltage boost, the power is reduced and shoot-through generation frequency can be raised to shrink the passive elements of the qZS network.

4. Simulation and experimental study of the 3P 3L NPC qZSI

4.1 Simulation study

In order to verify the proposed concepts, a comprehensive simulation study was performed in the PSCAD simulation tool. Table 4 shows all the parameters used in the simulation and experimental studies. The *LCL*-filter was designed according to [50] in order to provide an 8% lower THD of the output current (voltage). Switching frequency was 100 kHz in the shoot-through states generation mode. At the same time, without shoot-through states generation, switching frequency was twice reduced, which corresponds to the proposed modulation technique.

Table 4
List of parameters used for simulation and experimental setup.

Parameters	Unit	Value in each working point		
		1	2	3
Inductors L_1,L_2,L_3 and L_4	(mH)	0.9		
Capacitors C_1,C_2,C_3 and C_4	(μF)	200		
W	(W/m2)	1000	500	1000
Panels in series *(Ns)*		18		
Arrays in parallel *(Np)*	Unit	1		
Vpv	(V)	650	565	325
Ppv	(W)	3333	1534	1666
L_{f1}	(mH)	0.5		
L_{f2}	(mH)	0.2		
C_f	(μF)	0.47		
m		≃1	1	0.7
Third harmonic	%	0	19	19
D_S		0	0	0.3
Switching frequency (with shoot-through states generation)	(kHz)	100 kHz		

Fig. 7 illustrates several simulation results for the first operating point: Fig. 7 a -the waveforms of the output voltages; Fig. 7 b - the dc-link voltage; Fig. 7 c - voltages in the

capacitors; Fig. 7 d - input current and input voltage. In the first working point, the input voltage is equal to 650 V.

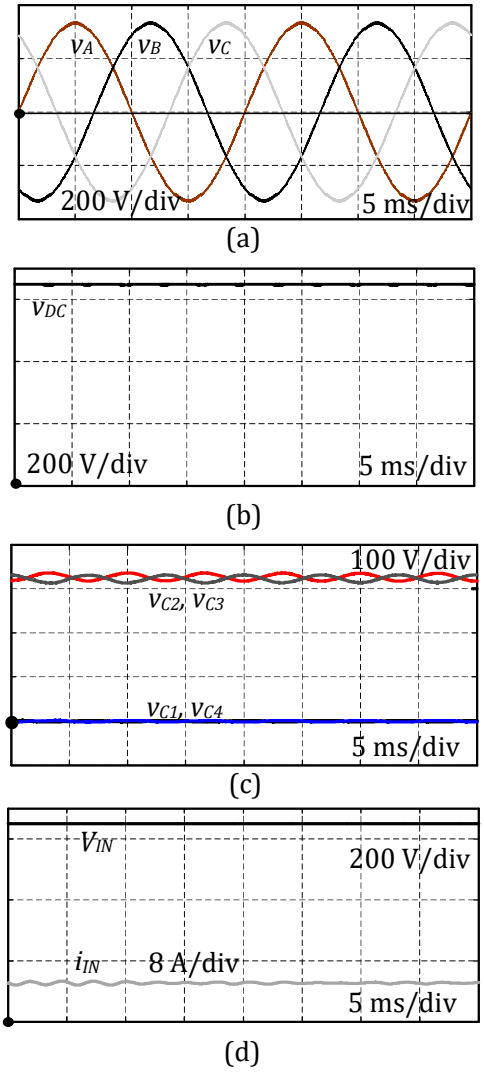


Fig. 7. Simulation waveforms for the first point in the VSI mode without the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

No voltage boost occurs, the third harmonic injection and shoot-through generation are not activated. A solar inverter works in the VSI mode. As can be seen, no ripples are present in the input current or the dc-link voltage because shoot-through switching states are not activated. Voltage on the capacitors C_1, C_4 is equal to zero.

Fig. 8 shows identical simulation results for the second operating point.

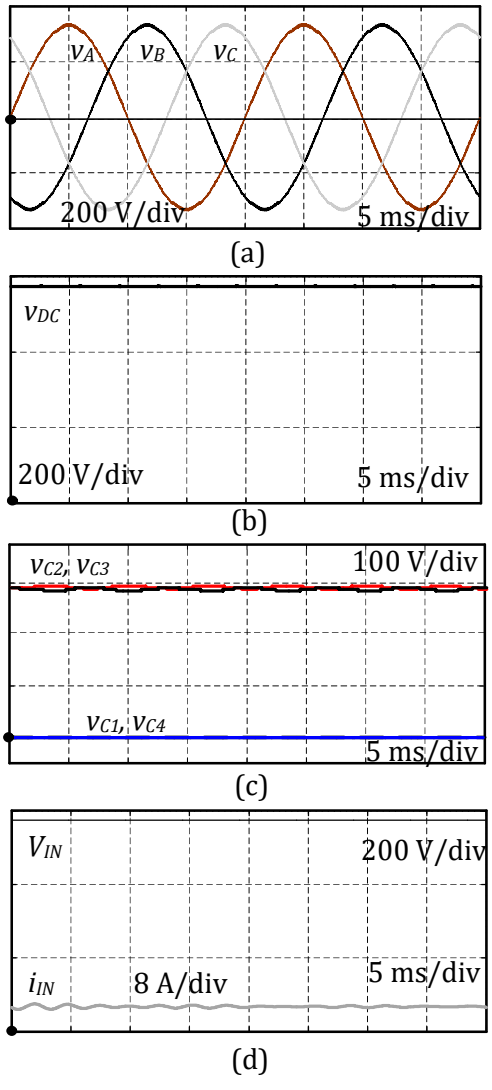


Fig. 8. Simulation waveforms for the second point in the VSI mode with the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

It can be seen that the input voltage is equal to 565 V. The third harmonic injection is present while shoot-through states generation is unactivated.

Fig. 9 depicts the main waveforms obtained for the third working point.

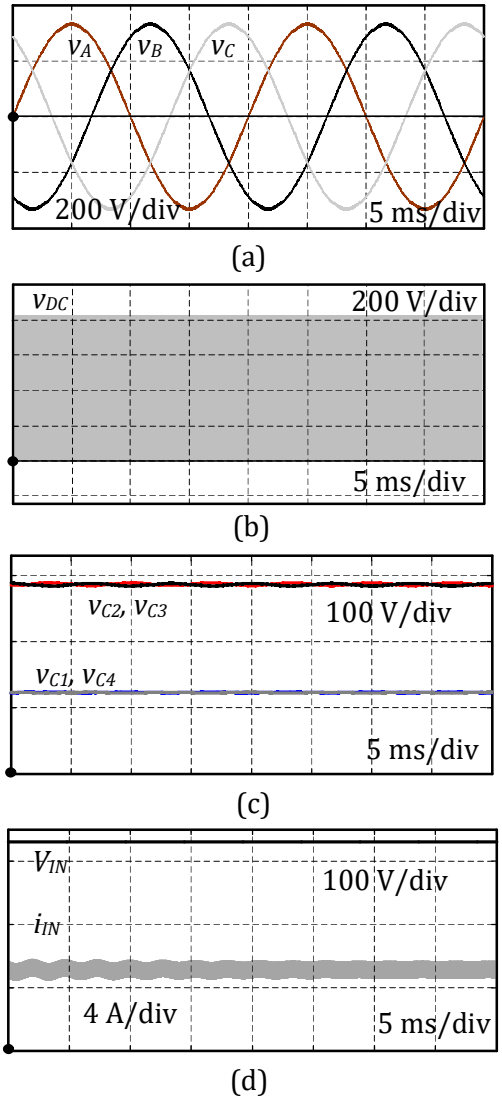


Fig. 9. Simulation waveforms for the third point with the third harmonic injection and shoot-through states generation: output voltages (a), dc-link voltage (b), input current and input voltage (c).

In this point, maximum boost capability is required by the third harmonic injection along with the shoot-through states to maintain 230 V phase to neutral voltages. Input voltage is equal to 365 V. The output voltage has very good quality. DC-link voltage has equally distributed shoot-through states. As a result, despite the low input voltage, the output voltage is equal to the nominal value.

4.2 Experimental study of the 3P 3L NPC qZSI

This section presents the experimental results of the topology described above. Fig. 10 shows the experimental prototype, which was finally assembled in a 3U box. It consists of four main PCB boards with external qZS inductors and output filters.

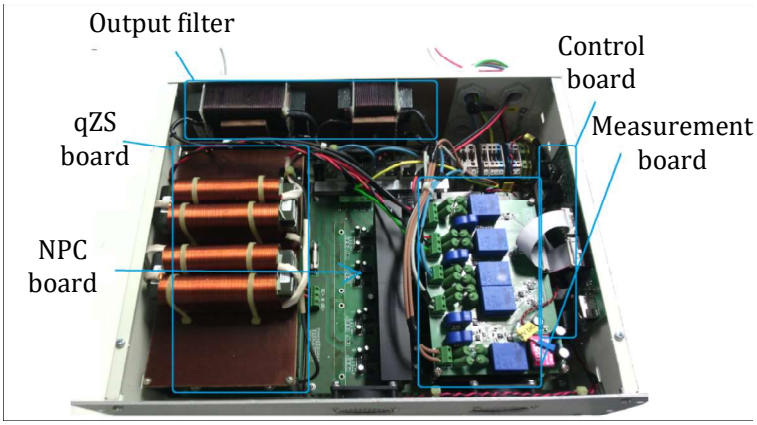


Fig. 10. Photo of the experimental prototype of the 3P 3L NPC qZSI.

Our experimental study was conducted to confirm the simulation results and investigate the overall efficiency of the converter. Several operation points were tested in full accordance with the simulation results. Parameters of the passive components and case study points are listed in Table 4. Advanced specification of the experimental prototype is presented in Table 5. All measurements were made by a digital oscilloscope Tektronix MDO4034B-3, current probes Tektronix TCP0150, and voltage probes Tektronix TPA-BNC.

Table 5
Specification of the experimental prototype

Parameter/Component	Value/Type
Output voltage (Line to line)	400 V
Input-voltage range	300 V – 800 V
Nominal power	3.5 kW
THD	≤8%
Control unit	Cyclon IV EP4CE22E22C8
Transistors driver	ACPL H342
Transistors	SiC C2M0080120D
Diodes	SiC C3D10065A
Current measurement	LEM LTS 15-NP
Voltage measurement	LEM_LV25-P

Fig. 11 shows several oscilloscope waveforms for the first operation point. The order of the measured parameters is in full correspondence with the simulation results depicted in Fig. 7. The voltage on the capacitors C_3 and C_4 is not shown since it coincidences with the voltage on the capacitors C_1 and C_2 correspondingly. It can be seen that no ripples are present in the input current or the dc-link voltage because shoot-through switching states are unactivated.

At the same time, Fig. 12 illustrates the experimental results for the second operation point. The results obtained are very similar to the simulation results shown in Fig. 8. Finally, Fig. 13 shows our experimental results for the third operation point. Obviously, these are close to the simulation results in Fig. 9. In summary, it could be concluded that our experiment confirms the theoretical and simulation analyses.

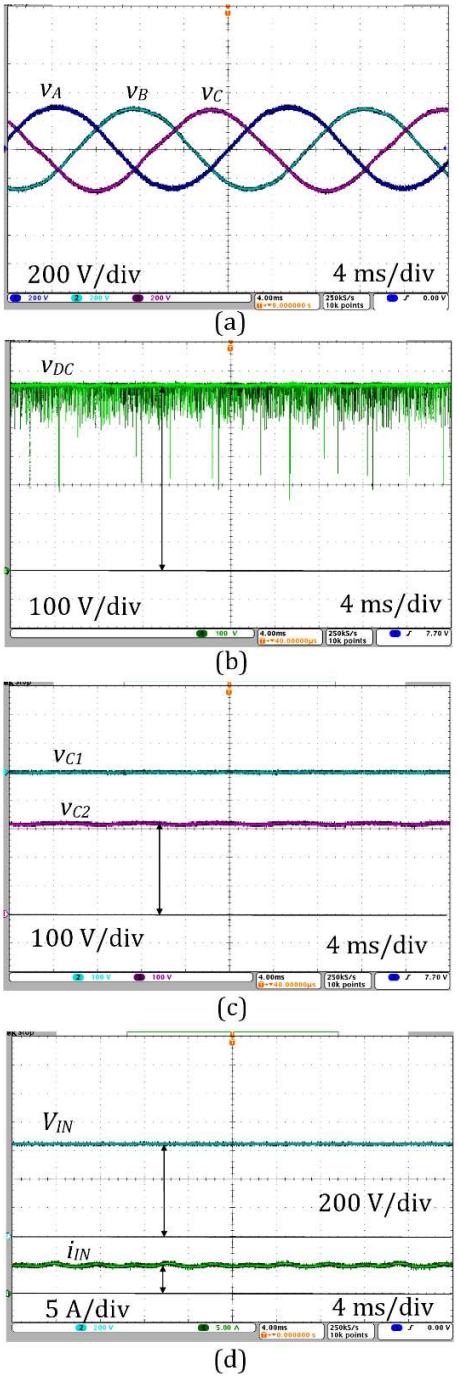


Fig. 11. Experimental waveforms for the first point in the VSI mode without the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

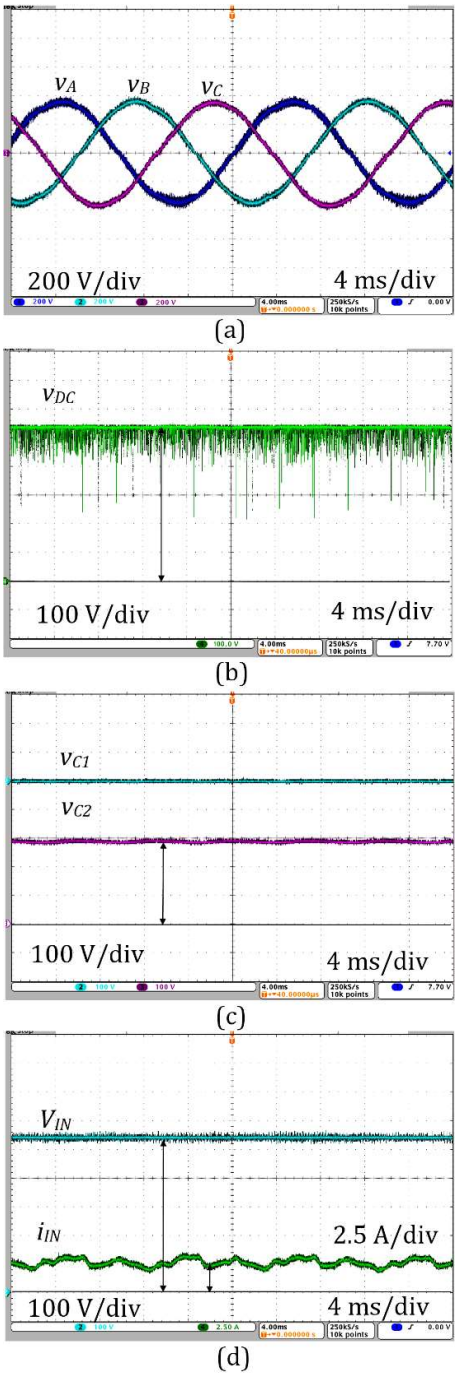


Fig. 12. Experimental waveforms for the second point in the VSI mode with the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

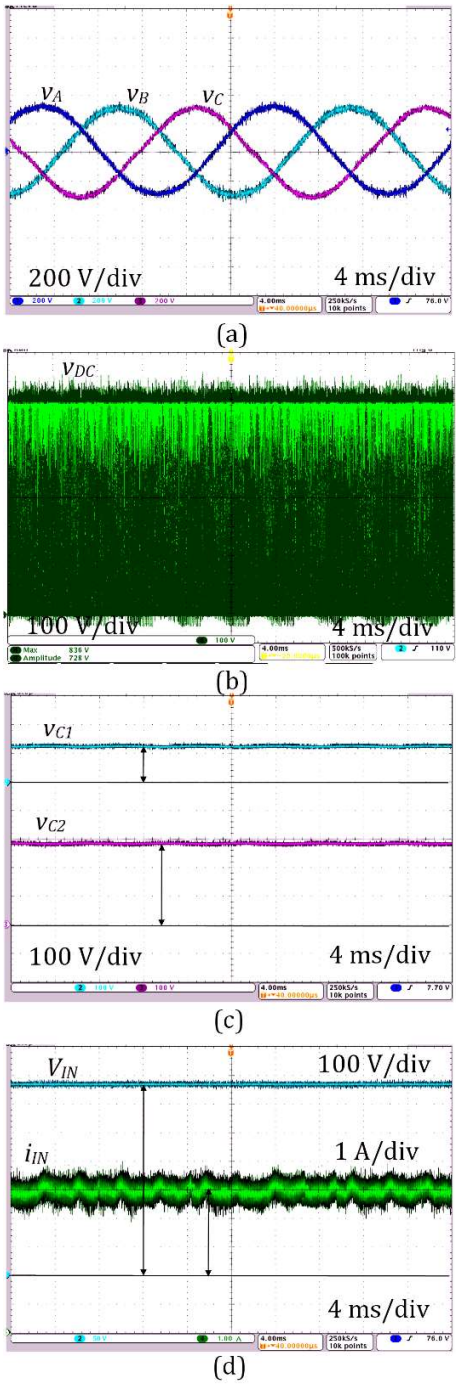
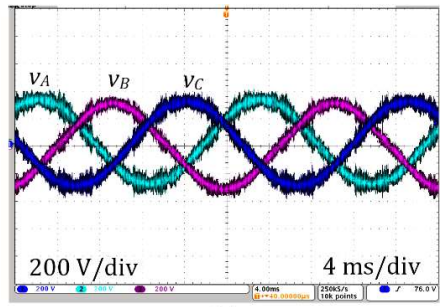


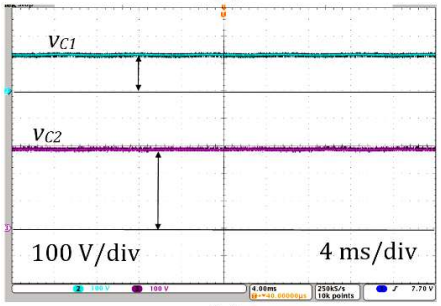
Fig. 13. Experimental waveforms for the third point with the third harmonic injection and shoot-through states generation: output voltages (a), dc-link voltage (b), input current and input voltage (c).

Table 6 summarizes the comparison of the results obtained. It can be seen that our experimental results are in good agreement with the theoretical results. At the same time, some differences in the absolute values of the input current capacitor ripples relate to variations in the real passive elements. Further, it should be noted that simulation and experimental waveforms have some minor low frequency ripples, which can be explained by the resonance nature of any impedance network, especially with the high-Q circuit.

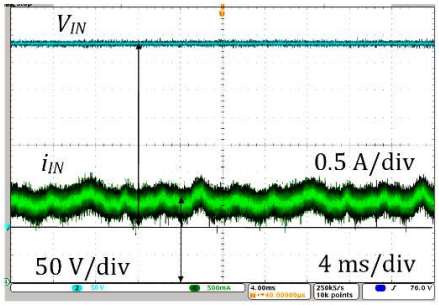
Fig. 14 shows additional experimental results under light load operation. Input power was about 450 W at the input voltage of 325 V. This operation is very similar to the third operation point that corresponds to the partial shadowing. In this case, low solar irradiation along with partial shadowing occur. Specifically, Fig. 14 a shows oscilloscope waveforms of the output three-phase voltage. It can be seen that the quality of the output voltage is worse than in the previous case. The reason is that output filter was designed for the nominal power and cannot provide the same quality under light load operation. At the same time, it should be underlined that output voltage disturbances belong to the high switching harmonics. 50 kHz and higher switching harmonics are out of the measuring range by standards. Voltage on the capacitors (Fig. 14 b) remains unchanged and is similar to Fig. 13 c. Fig. 14 c shows the input current and the input voltage. The average value of the input current is about 1.4 A at the high frequency ripple of about 0.9 A. It should be noted that input current still has CCM.



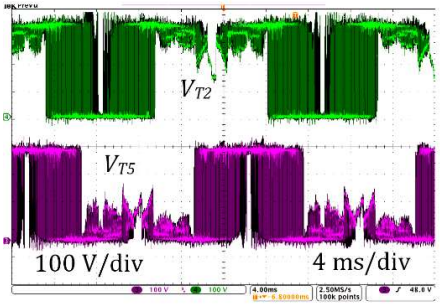
(a)



(b)



(c)



(d)

Fig. 14. Oscilloscope waveforms of the experimental prototype under light load operation: the output phase to the neutral voltage (a), voltage on the capacitors (b), input current and the input voltage (c), voltage stress on the semiconductors (d).

Table 6
Comparative analysis of theoretical (theor), simulation (sim) and experimental (exp) results.

Parameter	Unit	1			2			3		
		theor	sim	exp	theor	sim	exp	theor	sim	exp
Average input current I_{IN}	(A)	5.12	5.1	5	2.71	2.7	2.7	5.12	5.1	5
Input current ripple ΔI_{L1}	(A)	0	0	0	0	0		0.96	1	0.9
Average voltage on the capacitors C_1, C_4	(V)	0	0	0	0	0		122	122	122
Voltage ripple ΔV_{C1} on the capacitors C_1, C_4	(V)	0	0	0	0	0		0.08	0.08	0.1
Average voltage on the capacitors C_2, C_3	(V)	325	325	324	282.5	283		284	284	283
Voltage ripple ΔV_{C2} on the capacitors C_2, C_3	(V)	0	0	0	0	0		0.08	0.08	0.1

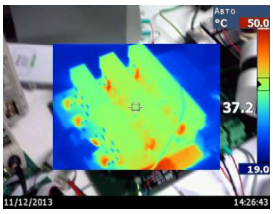
Voltage stress on the semiconductors is illustrated in Fig. 14 d. It is evident that no significant spikes occur on the transistors, which confirms good dynamic behavior of the SiC semiconductors. Excellent dynamic performance of the chosen SiC semiconductors leads to a very small voltage switching spike, which enhances the reliability of the converter.

4.3 Study of power losses

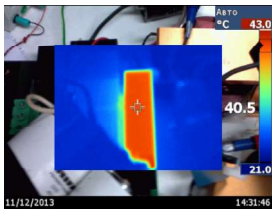
Fig. 15 illustrates the estimated efficiency of the described inverter. The study was conducted by using the method of summation of losses and the support of a thermal camera (Fluke Ti10), as well as the measurement equipment listed in section 4.2. Fig. 15 a shows the thermal picture of the NPC board. Fig. 15 b shows the qZS network

board. Despite the maximum power, the temperature of the heat sink does not exceed 40 ^{0}C. Therefore, no external fans are required. Further, as it was expected, qZS diodes are the main source of losses, but the temperature of the semiconductor junction is quite low. Fig. 15 c and Fig. 15 d illustrate the final efficiency diagram based on the power dissipation in the power semiconductors and magnetic components, which was experimentally estimated. Fig. 15 c shows the dependence of the efficiency versus the input voltage and the input power. It should be noted that this surface belongs to the constant irradiation level when the input voltage and power depend on the partial shadowing effect.

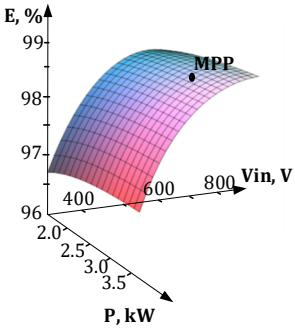
Fig. 15 d shows the losses distribution for the expected MPP with a maximum efficiency (3.3 kW and 650 V input voltage). Losses in different semiconductor components were estimated by means of temperature measurement of heat sinks and the thermal resistances of thermofilm and heat sink from datasheet parameters. The magnetic losses calculation was obtained by means of subtraction from the overall efficiency the semiconductor losses. In this point, the converter works in the VSI mode with $D_S=0$ and it can achieve an efficiency of 98.5%. In the worst case, the total efficiency was about 96.7%. The decrease in the efficiency is connected with the shoot-through states generation, which increases the switching losses in the transistors. In conclusion, transistor losses are about 28% of the total losses. At the same time, only two qZS diodes lead to 37% of the total losses, as shown in Fig. 15 d.



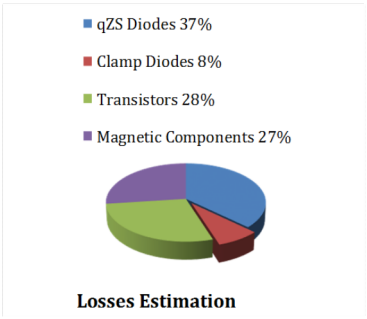
(a)



(b)



(c)



(d)

Fig. 15. Thermal pictures for the first operating point (a, b) and efficiency versus input voltage and input power (c), distribution of the losses for a maximum power point (d).

Fig. 16 shows the comparison of the efficiency curves both with maximum input current and light load operation. Input current as well as output voltage were constant at each point but input voltage changed. In the first case (dotted line), input current is about 5 A, which corresponds to the maximum level. In the second case (solid line), input current is about 1.4 A, which corresponds to the light load operation.

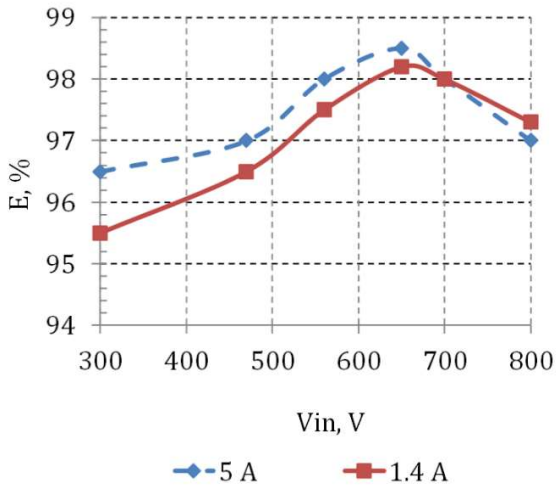


Fig. 16. Dependence of the efficiency on the input voltage with different input current levels.

It can be seen that in the second case, the efficiency was slightly worse, especially at the low input voltage level, with an efficiency of about 95.5 %. At the same time, in the nominal input voltage point, the efficiency is almost equal, which corresponds to the MPP and is even slightly higher at the maximum voltage level. The results obtained agree with the expectation, since for any type of a converter, light load operation is often a problem from the efficiency point of view.

5. Conclusions

This paper proposes the 3P 3L NPZ qZSI as a novel solution for PV applications. The converter combines advantages of the qZSI and 3L NPC VSI topologies. Low voltage stress on the switches, single-stage buck-boost power conversion, continuous input current, short-circuit immunity, and reduced output voltage and current THD are the main benefits. Thanks to the modern SiC semiconductors, high switching frequency is achievable. Therefore, a more compact impedance source network and low pass output filter are used. All these benefits could finally help to develop a more compact, lightweight and reliable inverter with improved performance.

A special new carrier-based modulation technique for the three-phase 3L topology with double frequency and uniformly distributed shoot-through generation was developed. The simulation and experimental results proved all theoretical expectations. Finally, efficiency measurement confirmed an outstanding performance

of the inverter. In the nominal operation point, an efficiency higher than 98% and in the shoot-through generation mode, not lower than 95.5 % was achieved.

Acknowledgments

This research work was financed by the Estonian Ministry of Education and Research (project SF0140016s11), Estonian Research Council (Grant G8538) European Social Fund, MOBILITAS Postdoctoral Research Grant (MJD391) and also supported by ECPE network. Advanced thanks to J-Lasslop Company for support in the design of the magnetic components.

References

[1] Renewables 2014 Global Status Report, Renewable Energy Policy Network for the 21st Century, Paris, France, June 2014.
[2] D. Meneses, F. Blaabjerg, O. Garcıa, J. A. Cobos, Review and comparison of step-up transformerless topologies for photovoltaic AC-module application, IEEE Trans. Power Electron. 28 (6) (2013) 2649-2663.
[3] S.B. Kjaer, J.K. Pedersen, F. Blaabjerg, A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules, IEEE Trans. Ind. Appl. 41 (5) (2005) 1292- 1306.
[4] The Fuel Cell Industry Review 2012, Fuel Cell Today, Royston, United Kingdom, 2012.
[5] G. Tsengenes, G. Adamidis, Investigation of the behavior of a three phase grid-connected photovoltaic system to control active and reactive power, Electric Power Systems Research 81 (2011) 177–184.
[6] M. Abbes, J Belhadj, New control method of a robust NPC converter for renewable energy sources grid connection, Electric Power Systems Research 88 (2012) 52– 63.
[7] L. Yushan, H. Abu-Rub, G. Baoming, Z-Source/Quasi-Z-Source Inverters: Derived Networks, Modulations, Controls, and Emerging Applications to Photovoltaic Conversion, IEEE Ind. Electron. Mag. 8 (4) (2014) 32-44.
[8] Y.P. Siwakoti, F.Z. Peng, F. Blaabjerg, P.C. Loh, G.E. Town, Impedance Source Networks for Electric Power Conversion Part-I: A Topological Review, IEEE Trans. Power Electron. 30 (2) (2015) 699-716.

[9] Y.P. Siwakoti, F. Peng, F. Blaabjerg, P. Loh, G.E. Town, Impedance Source Networks for Electric Power Conversion Part-II: Review of Control Method and Modulation Techniques, IEEE Trans. Power Electron. 30 (4) (2015) 1887 – 1906.
[10] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, S. Stepenko, Single phase three-level neutral-point-clamped quasi-Z-source inverter, IET PEL. 8 (4) (2015) 1-10.
[11] O. Husev, S. Stepenko, C. Roncero-Clemente, E. Romero-Cadaval, R. Strzelecki, Experimental investigation of high frequency 3L-NPC qZS inverter for photovoltaic application, In: Proceedings of IECON 2013 - 39th Annual Conference on IEEE Industrial Electronics Society, 10-14 November, 2013, pp. 5967 – 5972.
[12] O. López, F. D. Freijedo, A.G. Yepes, P. Fernández-Comesaña, J. Malvar, R. Teodorescu, J. Doval-Gandoy, "Eliminating Ground Current in a Transformerless Photovoltaic Application", IEEE Transactions on Energy Conversion, vol. 25, no. 1, march 2010.
[13] Giacomini, J.C., Michels, L., Schuch, L., Pinheiro, H., Rech, C., "Design of a LCL filter for leakage current reduction in transformerless PV grid-connected three-level inverter", IEEE Applied Power Electronics Conference and Exposition (APEC), pp.239-245, 15-19 March 2015.
[14] M. C Cavalcanti, A. M. Farias, K.C. Oliveira, F. A. S. Neves and J.L. Afonso, "Eliminating Leakage Currents in Neutral Point Clamped Inverters for Photovoltaic Systems", IEEE Transactions on Power Electronics, vol.28, no.4, pp.2856-2866, June 2013.
[15] V. Erginer, M.H. Sarul, "A novel reduced leakage current modulation technique for Z-source inverter used in photovoltaic systems", IET Power Electron., 2014, Vol. 7, Iss. 3, pp. 496–502.
[16] A. D. Rajapakse, D. Muthumuni, Simulation tools for photovoltaic system grid integration studies, 39th Electric Power & Energy Conference EPEC, 2009, p. 1-5.
[17] R.C. Campbell, A circuit based photovoltaic array model for power system studies", Power Symposium, North American, 2007, pp. 97-101.
[18] K. Seul- Ki, K. Eung- Sang, A. Jong-Bo, Modeling and control of a grid-connected Wind/PV hybrid generation system", Transmission and Distribution Conference and Exhibition, IEEE PES, 2006, pp. 1202- 1207.
[19] J. Xue, Y. Zhongdong, W. Bingbing, J. Peng, Design of PV Array Model Based on EMTDC/PSCAD, Power and Energy Engineering Conference, APPEEC2009. Asia- Pacific, 2009, pp. 1-5.
[20] K. Seul-Ki, J. Jin-Hong, C. Chang-Hee, K. Eung-Sang, A. Jong-Bo, Modeling and simulation of a grid-connected PV, generation system for electromagnetic transient analysis, Solar Energy, 83 (5) (2009), 664-678.
[21] C. Roncero-Clemente, E. Gonzalez-Romera, E. Romero-Cadaval, M.I. Milanes-Montero,V. Minambres-Marcos, PSCAD/EMTDC model for photovoltaic modules with MPPT based on manufacturer specifications, 8th International Conference on Compatibility and Power Electronics (CPE), 5-7 June, 2013, pp.69-74.

[22] LDK 180D(s)-200D(s) datasheet. http://www.gsenergy.eu/doc/ldk/LDK-180D-200D-24Module_en.pdf. Consulted on 21st of November 2013.
[23] J. Anderson, F.Z. Peng, A Class of quasi-Z-source inverters, Industry Applications Society Annual Meeting, IAS '08, 5-9 October, 2008, pp.1-7.
[24] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M. M. Prats, The age of multilevel converters arrives, IEEE Ind. Electr. Mag. 2 (2) (2008) 28–39.
[25] S. Kouro, M. Malinowski, K Gopakumar, J. Pou, L.G Franquelo, B. Wu, J. Rodriguez, M.A. Perez, J.I. Leon, Recent advances and industrial applications of multilevel converters, IEEE Trans. Ind. Electron. 57 (8) (2010) 2553-2580.
[26] K.R.M.N. Ratnayake, Y. Murai, A novel PWM scheme to eliminate common-mode voltage in three-level voltage source inverter, Power Electronics Specialists Conference, PESC 98, 1998, pp. 269 – 274.
[27] M.C. Cavalcanti, K.C. de Oliveira, A.M.de Farias, F.A.S. Neves, G.M.S.Azevedo, F.C. Camboim, Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems, IEEE Trans. Ind. Electron. 57 (4) (2010) 1360 - 1368.
[28] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, T. Lu, Hybrid Selective Harmonic Elimination PWM for Common-Mode Voltage Reduction in Three-Level Neutral-Point-Clamped Inverters for Variable Speed Induction Drives, IEEE Trans. Power Electron. 27 (3) (2012) 1152 - 1158.
[29] M. Shen, Z-source inverter design, analysis, and its application in fuel cell vehicles, PhD thesis, Michigan State University, 2006.
[30] F. Z. Peng, M. Shen, and Z. Qian, Maximum boost control of the Z-source inverter, IEEE Trans. Power Electron. 20 (4) (2005) 833-838.
[31] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L.M. Tolbert, D.J. Adams, Constant boost control of the Z-source inverter to minimize current ripple and voltage stress, IEEE Trans. Industry Applic. 42 (3) (2006) 770-778.
[32] O. Ellabban, J. Van Mierlo,P. Lataire, Comparison between different PWM control methods for different Z-source inverter topologies, 13th IEE European Conference on Power Electronics and Applications, EPE '09, 8-10 September, 2009, pp.1-11.
[33] Y. Huang, M.S. Shen, F.Z. Peng, J.Wang, Z-Source inverter for residential photovoltaic systems, IEEE Trans. on Power Electro. 21 (6) (2006) 1776-1782.
[34] R. Badin, Y. Huang, F.Z. Peng, H.G. Kim, Grid Interconnected Z-Source PV System, in Proc. IEEE PESC'07, Orlando, FL, June, 2007, pp. 2328-2333.
[35] D. Sun, B. Ge, D. Bi, F.Z. Peng, Analysis and control of quasi-Z source inverter with battery for grid-connected PV system, Electrical Power and Energy Systems 46 (2013) 234–240.
[36] O. Ellabban, H. Abu-Rub, G. Baoming, Z-source inverter: basics, modeling, controling, topology modifications and applications. Tutorial in IECON 2013 - 39th Annual Conference on IEEE Industrial Electronics Society, Vienna, Austria, 10-13 November, 2013.

[37] J.I. Leon, R. Portillo, L.G. Franquelo, S. Vazquez, J.M. Carrasco, E. Dominguez, New space vector modulation technique for single-phase multilevel converters, In: Procedding of IEEE International Symposium on Industrial Electronics, ISIE, 4-7 June, 2007, pp.617-622.
[38] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, Multilevel voltage-source-converter topologies for industrial medium-voltage drives, IEEE Trans. Ind. Electro. 54 (6) (2007) 2930–2945.
[39] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M. M. Prats, The age of multilevel converters arrives, IEEE Ind. Electro. Mag. 2 (2) (2008) pp. 28–39.
[40] W. Yao, H. Hu, Z. Lu, Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter, IEEE Trans. Power Electron. 23, (1) (2008), pp. 45–51.
[41] D. G. Holmes, T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Piscataway, NJ: IEEE Press, 2003.
[42] F. Wang, Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters, IEEE Trans. Ind. Appl. 38 (2) (2002) pp. 500–506.
[43] N. V. Nho, M.-J. Youn, Comprehensive study on space-vector-PWM and carrier-based-PWM correlation in multilevel invertors, Proc. Inst. Elect. Eng.—Elect. Power Appl., vol. 153, no. 1, Jan., 2006, pp. 149–158.
[44] J. Rodríguez, J.S. Lai, F.Z. Peng, Multilevel inverters: a survey of topologies, controls, and applications, IEEE Trans. Ind. Electron. 49 (4) (2002) pp. 724-738.
[45] P.C. Loh, F. Gao, F. Blaabjerg, S. Y. C. Feng and N. J. Soon, Pulse-width-Modulated Z-Source Neutral-Point-Clamped Inverter, IEEE Trans. Ind. Appl. 43 (5) (2007) pp. 1295-1308.
[46] P.C. Loh, F. Blaabjerg and C.P. Wong, Comparative Evaluation of Pulsewidth Modulation Strategies for Z-Source Neutral-Point-Clamped Inverter, IEEE Trans. Power Electron. 22 (3) (2007) pp. 1005-1013.
[47] P.C. Loh, D.G. Holmes, Y. Fukuta, T.A. Lipo, Reduced common-mode modulation strategies for cascaded multilevel inverters, IEEE Trans. Ind. Appl., 39 (5) (2003) pp. 1386-1395.
[48] P.C. Loh, F. Gao, F. Blaabjerg, W.L. Sok, Operational Analysis and Modulation Control of Three-Level Z-Source Inverters With Enhanced Output Waveform Quality, IEEE Trans. Power Electron., 24 (7) (2009), pp. 1767-1775.
[49] F.B. Effah, P. Wheeler, J. Clare, A. Watson, Space-Vector-Modulated Three-Level Inverters With a Single Z-Source Network, IEEE Trans. Power Electron. 28, (6) (2013) pp. 2806-2815.
[50] O. Husev, A. Chub, E. Romero-Cadaval, C. Roncero-Clemente, D. Vinnikov, Voltage distortion approach for output filter design for off-grid and grid-connected PWM Inverters, Journal of Power Electronics 15 (1) (2015) pp. 288-297.