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Keyword:	three level NPC inverter, impedance source inverter, quasi-Z-source inverter, Z-source inverter, hysteresis current control

Hysteresis Current Control with Distributed Shoot-Through States for Impedance Source Inverters

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This paper presents a hysteresis current control technique with shoot-through states distribution. This control algorithm could be applied to three- and multi-level inverters with any impedance source network where reference current control signal along with shoot-through states are required. Possible modifications of the presented algorithm are discussed. The steady state analysis was made to explain the operation principle of the algorithm. As a result, the link between the band ratio of the hysteresis current controller, the input voltage and the desired dc-link voltage was obtained. All theoretical predictions were proved by simulation and experimental results. Future applications are discussed.

Key words: Three-level NPC inverter, impedance source inverter, quasi-Z-source inverter, Z-source inverter, hysteresis current control.

I. INTRODUCTION

Renewable energy sources have become extremely popular. As a result, many new types of interface converters have emerged. The family of the single stage buck boost inverters based on Z-Source (ZS) network or any other Z-source-derived network (Fig. 1) is highlighted.

The ZS network proposed in [1] can overcome main drawbacks of the Voltage Source Inverter (VSI) and the Current Source Inverter (CSI). The main merit of this topology is the buck-boost operation capability. Voltage regulation within a single-stage inverter is achieved by means of cross conduction of transistors – shoot-through switching states. Many other new Impedance Source (IS) networks have been proposed recently. Fig. 2 shows some of those networks. The Quasi-Z-Source (qZS) inverter topology proposed in [2] has continuous input current, which is preferable in renewable energy applications [3]-[5].

In the further development, it was intended to extend the regulation capability by means of coupled inductors whose turn ratios can be different. A trans-Z-source (or T-source) network was proposed in [6]-[8]. Extended voltage gain and reduced element count are the main advantages of the Trans-Z-Source (TZS) network over the ZS and qZS networks.

The trans-Quasi-Z-Source (TQZS) network shown in Fig. 2 *d* is a variant of the TZS. As compared to the TZS, double reduced capacitance of the TQZS with a unity turns ratio can be can be achieved. However, after capacitance replacing, the shape of the input current will worsen and a discontinuous input current is introduced [9]. Many other topologies are available to increase the gain factor [10]-[15], the TZ-source network being among them [14]. Logical deviation of an inductor's coupling idea occurred in the Y-source

network (Fig. 2 *f*). Turns ratio and winding placement of the 3-winding inductor can be designed to achieve the desired gain, while maintaining a small switch duty ratio [15].

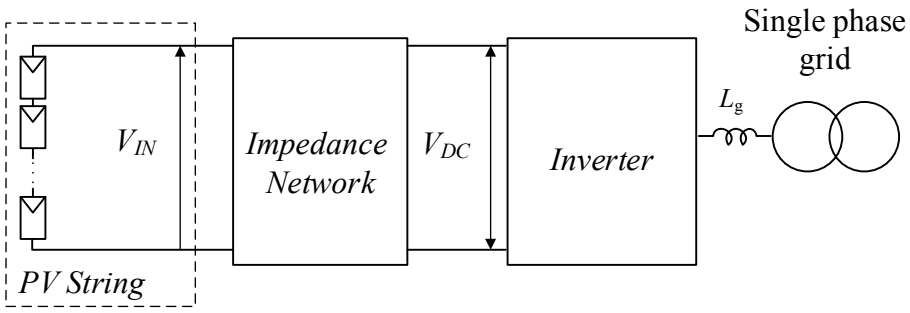


Fig. 1. Case study system.

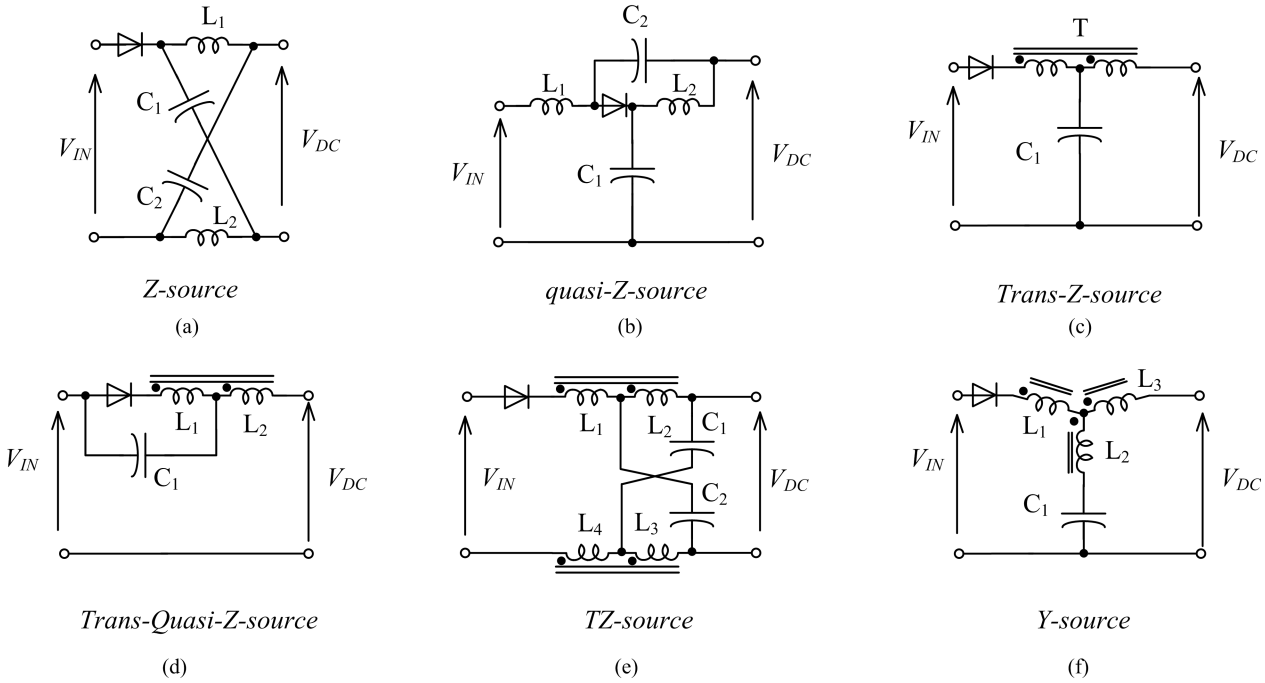


Fig. 2. Impedance source networks.

The IS networks described above have been demonstrated for dc-ac, dc-dc and ac-ac applications [16], [17]. Such new generation of dc-ac converters with single stage energy conversion can realize grid connection along with the Maximum Power Point Tracking (MPPT) function with a wider input voltage range operation than in conventional inverter topologies. Traditionally, modulation techniques for IS inverters with boost control are used in similar applications [18]-[23]. The classification is summarized in Fig. 3.

For instance, maximum boost control was proposed in [16]. The main drawback of that approach is low-frequency input current ripple. Maximum Constant Boost Control (MCBC) solves the problem by using the constant shoot-through duty ratio along with the third harmonic injection [19]. Typically, a three-phase system is discussed, but all of them can be modified for single-phase applications as well as for multilevel inverter topologies [23]-[27].

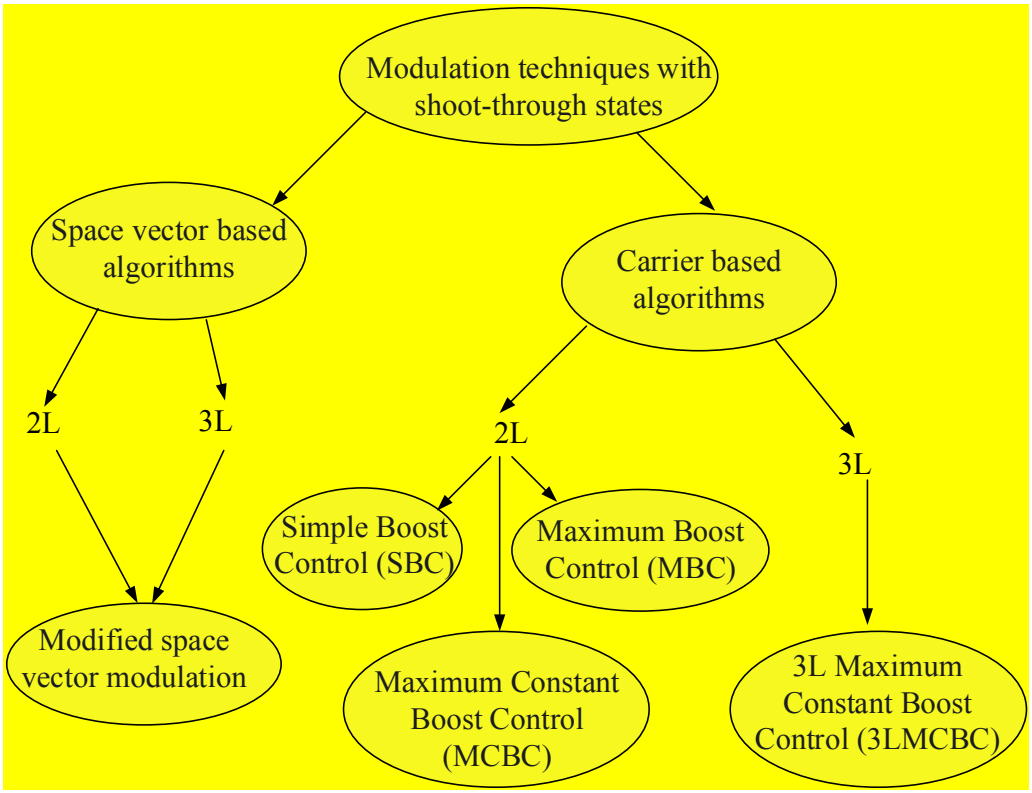


Fig. 3. Summarized classification of existing modulation techniques for IS inverters.

Further, many special space vector modulation techniques with embedded shoot-trough duty cycle have been developed [28]-[30]. The main drawback of such solutions is high demands to the control system. As a result, industrial applications are limited [31].

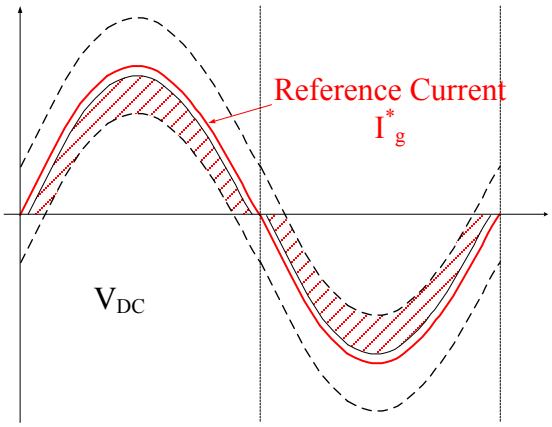
Hysteresis current control, which is based on the current reference signal, is often used in traditional CSI and VSI solutions [32]-[37]. In addition, several approaches for multilevel converters are described in [38], [39]. Commonly, hysteresis control is preferable due to simplicity, fast deadbeat transient response and overcurrent protection. But it is difficult to implement it in the system with shoot-through states.

This paper proposes a novel hysteresis current control for a single-phase inverter based on any IS network with distributed shoot-through states. Section II explains the novel algorithm in detail. The steady state analysis is presented in section III. Section IV describes the simulation along with experimental results. Finally, conclusions are presented in section V. This paper is based on earlier preliminary publication [40] and includes a comprehensive theoretical analysis and experimental results, however, not presented there.

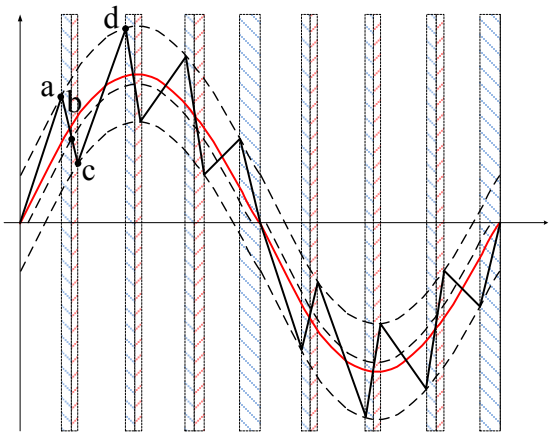
II. New Hysteresis Current Control Methods

A. Novel Simple Hysteresis Current Control

The novel hysteresis control is outlined in Fig. 4. The main idea is to use a modified hysteresis control with shoot-through states distribution. Total hysteresis current band ΔI defines the current error and includes a main band ΔI_0 (Fig. 4 *c*) and an auxiliary shoot-through current band ΔI_S. The control system requires a reference grid current I^*_g at the input.



(a)



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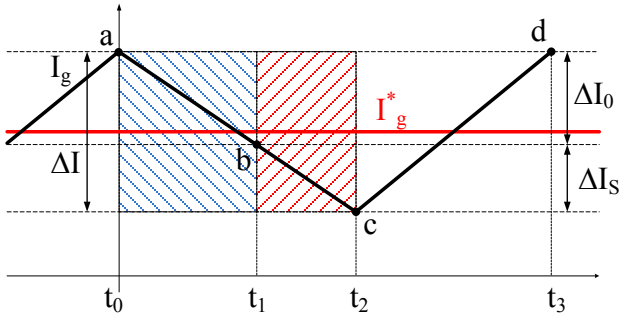


(c)

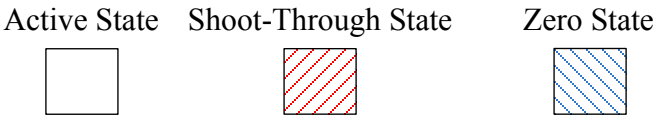


Fig. 4. Novel hysteresis current control: basic principle (a), example of control (b), and detailed commutation principle during a single switching period.

When the grid current I_g reaches the upper current limit (point a in Figs. 4 *b* and *c*), the zero state is switched on and the grid current starts falling.

At the instant when the grid current crosses the boundary line between ΔI_0 and ΔI_S (point b), the shoot-

through state appears. In point c the grid current reaches a lower limit and the active state is switched on up to point d.

The band ratio between the auxiliary band ΔI_S and the total band ΔI defines the necessary boost factor. Fig. 4c shows the time diagram of the single switching cycle upon an assumption that the reference current remains constant in a switching cycle.

B. Modified Hysteresis Control Methods

Fig. 5 illustrates several modified hysteresis control methods. The first idea lies in the modulation of hysteresis bands. Fig. 5 *a* shows this principle with sinusoidal modulation.

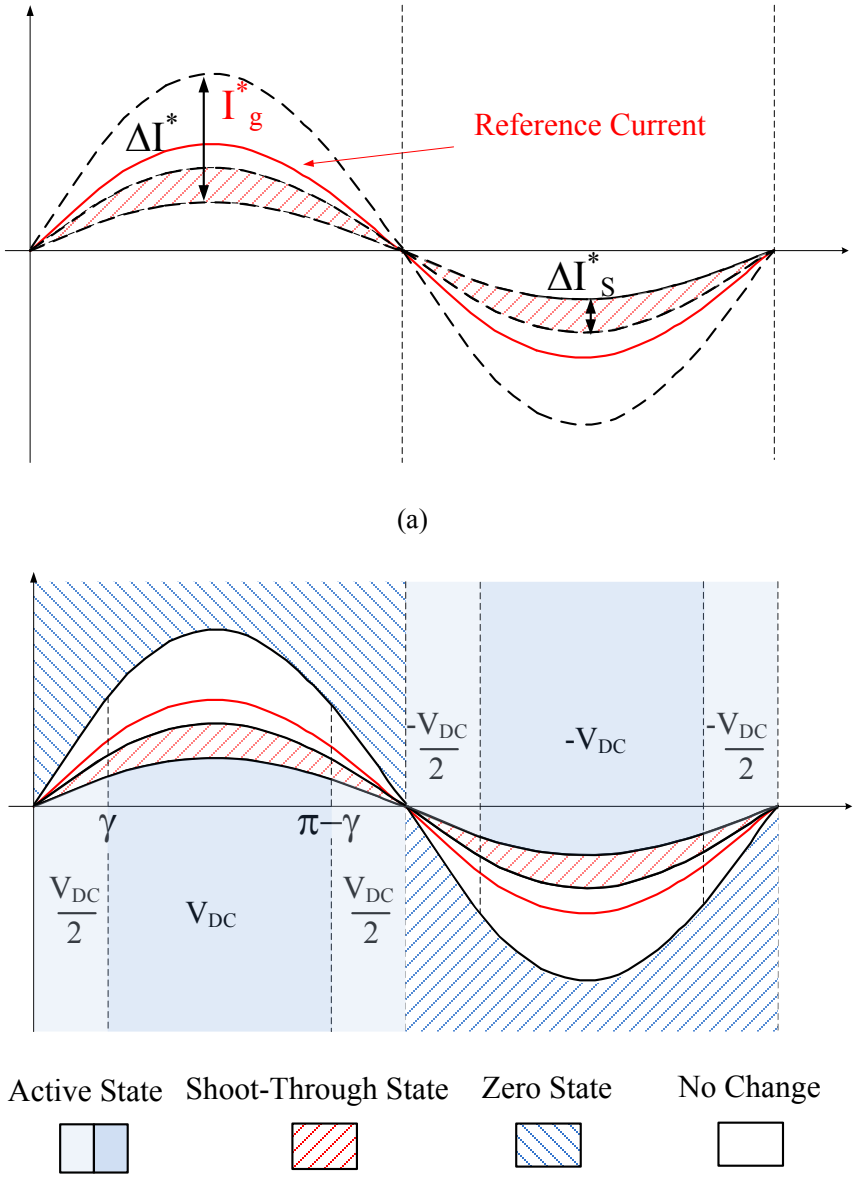


Fig. 5. Modified hysteresis control method: basic principle (a) and example of control of 2L (when γ=0) and 3L inverters (b).

Typically, the switching frequency is higher near zero crossing points where the derivative of the

reference current waveform has maximum value and higher waveform distortion. The aim of such modification is to decrease the Total Harmonic Distortion (THD) of the current and to smoothen switching losses. Though the switching frequency is even higher near zero current value, switching losses are minor.

It should be noted that many other modification possibilities based on the hysteresis band modulation exist [29]-[33].

Fig. 5 *b* illustrates a multilevel application possibility of the proposed hysteresis approach. The corresponding states are defined by the region where current is detected. The idea of such approach is to separate the active states into several levels in accordance with the number of converter levels.

In the five-level topology, in the time domain of the half cycle from 0 to γ and from π-γ to π, half of the dc-link voltage V_{DC} is applied. In the complementary time domain from γ to π-γ, full dc-link voltage is applied. Such approach can be generalized and applied for any N-level topology.

Further analysis was made considering an L-filter at the output. However, the high order grid side filters, like LCL, are common in high power applications to satisfy power quality standards and ensure acceptable power density. A combination of a high order filter and the hysteresis control can lead to an unstable operation [41]. Undesirable resonance in the grid side filter can be suppressed with active and passive damping [42]. Active damping shows good performance in systems with a hysteresis current controller and an LCL filter [43], while the control system design with active damping requires a complicated analysis [44]. Passive damping approach is the simplest solution for filter stabilization, while it employs additional passive network with resistors, which results in higher losses [45]. A digital hysteresis control system can also improve stability of the IS inverter at constant switching frequency, which limits the output current spectrum [46].

Another issue that could limit the performance of the proposed control system is an inherent instability of the IS inverters. Operation of the IS inverters changes significantly at transition between the continuous and the Discontinuous Conduction Modes (DCM) [47]. The IS network usually contains inductors and capacitors, which leads to the non-minimum phase dynamic behavior and the presence of resonance frequencies [48], [49]. However, in practice the influence of these factors can be mitigated with passive damping, limited switching frequency range, or improved two-loop control [50].

III. Steady State Analysis of the Proposed Methods

To define the correlation between band ratios and boost properties, the steady state analysis was made. For a generalization, the five-level topology in this analysis is discussed. It is easy to proceed to the Three-Level (3L) inverter assuming $\gamma = 0$.

A general equation that describes the behavior of the grid current during the time interval t_0 - t_1 and t_1 - t_2 (Fig. 4 *c*):

$$L_g \frac{di_g(t)}{dt} = V_{inv}(t) - V_g = V_{inv}(t) - V_M \cdot \sin(\omega t), \quad (1)$$

where V_M is the amplitude of the grid phase-to-neutral voltage and $V_{inv}(t)$ is the instantaneous output voltage of the inverter.

Time interval t_0 - t_1 corresponds to the zero state and t_1 - t_2 to the shoot-through state where $V_{inv}(t)=0$ and assuming that the minimum switching frequency is well over the grid frequency, as a result, the time interval can be estimated as:

$$t_2\text{-}t_0 = \frac{\Delta I(t)\cdot L_g}{V_M \cdot \sin(\omega t)}, \tag{2}$$

where $\Delta I(t) = \alpha \cdot I^*_g(t)$

A general equation that describes the behavior of the grid current during the active state in the time interval t_2 - t_3:

$$L_g \frac{di_g(t)}{dt} = \hat{V}_{inv}(t) - V_M \cdot \sin(\omega t), \tag{3}$$

where $\hat{V}_{inv}(t)$ is the instantaneous peak value of the inverter output voltage. It equals either $V_{DC}/2$ or V_{DC} for a positive half-wave. The function in a phase domain for a positive half wave of the current, as shown in Fig. 5b can be defined as:

$$\hat{V}_{inv}(\omega t) = \begin{cases} \frac{V_{DC}}{2}, \text{if } 0 \le \omega t \le \gamma \text{ or } \pi - \gamma \le \omega t \le \pi \\ V_{DC}, \text{if } \gamma \le \omega t \le \pi - \gamma \end{cases} \tag{4}$$

Similarly, the time interval can be estimated as:

$$t_3 - t_2 = \frac{\Delta I(t)\cdot L_g}{(\hat{V}_{inv}(t) - V_M \cdot \sin(\omega t))}. \tag{5}$$

From the equations above, it is possible to obtain the shoot-through duty ratio for the single switching cycle:

$$d_S = \frac{(t_2 - t_1)}{(t_3 - t_0)}. \tag{6}$$

From Fig. 4 *c*, the ratio between the time intervals can be defined as:

$$t_2 - t_1 = (t_2 - t_0)\cdot\frac{\Delta I_S}{\Delta I} = (t_2 - t_0)\cdot\Delta_S, \tag{7}$$

where $\Delta_S = \Delta I_S/\Delta I$ is an auxiliary band ratio. The shoot-through duty ratio can be expressed as:

$$d_S(t) = \Delta_S \cdot \left(1 - \frac{V_M \cdot \sin(\omega t)}{\hat{V}_{inv}(t)}\right). \tag{8}$$

An average value of the shoot-through duty cycle can be calculated as (integrating in a phase domain, where $\omega t = \phi$, over a half fundamental period):

$$D_S = \frac{1}{\pi} \cdot \int_0^{\pi} d_S(\phi) d\phi =$$

$$= \frac{1}{\pi} \cdot \int_0^{\pi} \Delta_S \cdot (1 - \frac{V_M \cdot \sin(\phi)}{\hat{V}_{inv}(\phi)}) d\phi =$$

$$= \frac{1}{\pi} \cdot (2 \cdot \int_0^{\gamma} \Delta_S \cdot (1 - \frac{2 \cdot V_M \cdot \sin(\phi)}{V_{DC}}) d\phi + \quad (9)$$

$$+ \int_{\gamma}^{\pi-\gamma} \Delta_S \cdot (1 - \frac{V_M \cdot \sin(\phi)}{V_{DC}}) d\phi) =$$

$$= \Delta_S \cdot (1 - \frac{4}{\pi} \cdot \frac{V_M}{V_{DC}} (1 - \frac{1}{2} \cdot \cos(\gamma))).$$

From previous studies [1]-[4], it can be concluded that constant output voltage is achieved by maintaining the constant capacitance voltage (C_1 in Fig. 2):

$$V_C = V_{IN} \cdot \frac{1 - D_S}{1 - 2 \cdot D_S}, \quad (10)$$

while the dc-link voltage strictly depends on the input voltage:

$$V_{DC} = 2V_C - V_{IN}. \quad (11)$$

Substituting Eqs. (10) and (11) into Eq. (9), the expression that links the input voltage V_{IN}, the auxiliary band ratio Δ_S, the angle γ, and the capacitor voltage V_C all together can be obtained as:

$$\Delta_S = \frac{V_C - V_{IN}}{2V_C - V_{IN} - \frac{2}{\pi} V_M (2 - \cos(\gamma))}. \quad (12)$$

Fig. 6 illustrates the dependences of the auxiliary band ratio Δ_S versus the input voltage V_{IN}, while the capacitor voltage V_C remains constant and equal to the amplitude of the grid voltage V_M. Angle $\gamma=0$, which corresponds to the Two-Level (2L) topology. The maximum value of the auxiliary band ratio corresponds to the minimum value of the input voltage. $\Delta_S=1$ corresponds to the minimum possible value of the input voltage with maximum dc-link utilization. In the 3L topology (dotted line), an increase in the angle γ leads to a decrease in the input voltage operation range. The benefit of the 3L topology is the quality of the output current.

Controlling the capacitor voltage is a relatively simple approach. But at the same time, from Eq. (11) it is evident that the dc-link will vary in a wide range similar to the MCBC in [19]. As compared to hysteresis control, the capability of dc-link use in most carrier-based controls is worse .

To achieve maximum performance of dc-link use, we will find dependences between the auxiliary band ratio Δ_S, the input voltage V_{IN}, and the dc-link voltage V_{DC}.

In most cases, in the impedance topologies described above, the boost factor is:

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - 2 \cdot D_S}. \quad (13)$$

Taking into account Eq. (13), auxiliary band ratio Δ_S dependences can be expressed from Eq. (9) as a

function of the input voltage, the desired dc-link voltage and the angle of the applied voltage of the converter:

$$\Delta_S = \frac{\Delta I_S}{\Delta I} = \frac{V_{DC} - V_{IN}}{2 \cdot (V_{DC} - \frac{4}{\pi} V_M \cdot (1 - \frac{1}{2} \cdot \cos(\gamma)))}. \quad (14)$$

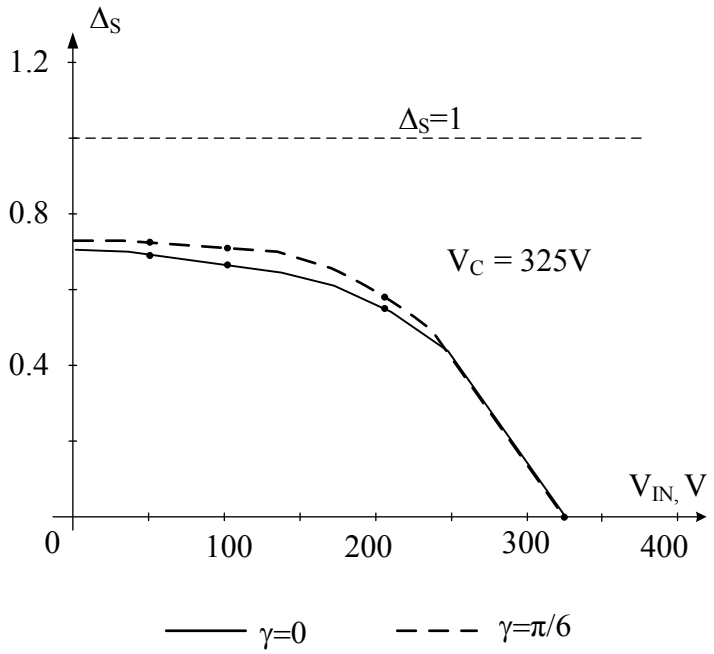


Fig. 6. Voltage step-up capability of the proposed hysteresis control approach with different parameters: $\gamma = 0$ and $\gamma = \pi/6$.

Fig. 7 illustrates the dependences of the auxiliary band ratio Δ_S versus the input voltage V_{IN}, while the dc-link voltage remains constant. Fig. 7 *a* shows several curves with different dc-link voltages and the angle $\gamma=0$, which corresponds to the 2L topology. The maximum value of the auxiliary band ratio corresponds to the minimum value of the input voltage. $\Delta_S=1$ corresponds to the minimum possible value of the input voltage with maximum dc-link utilization. It should be noted that rise of the dc-link voltage leads to a decrease in the required auxiliary band ratio Δ_S in a steady state mode. It means that when current rise up time shrinks while current fall down time remains the same.

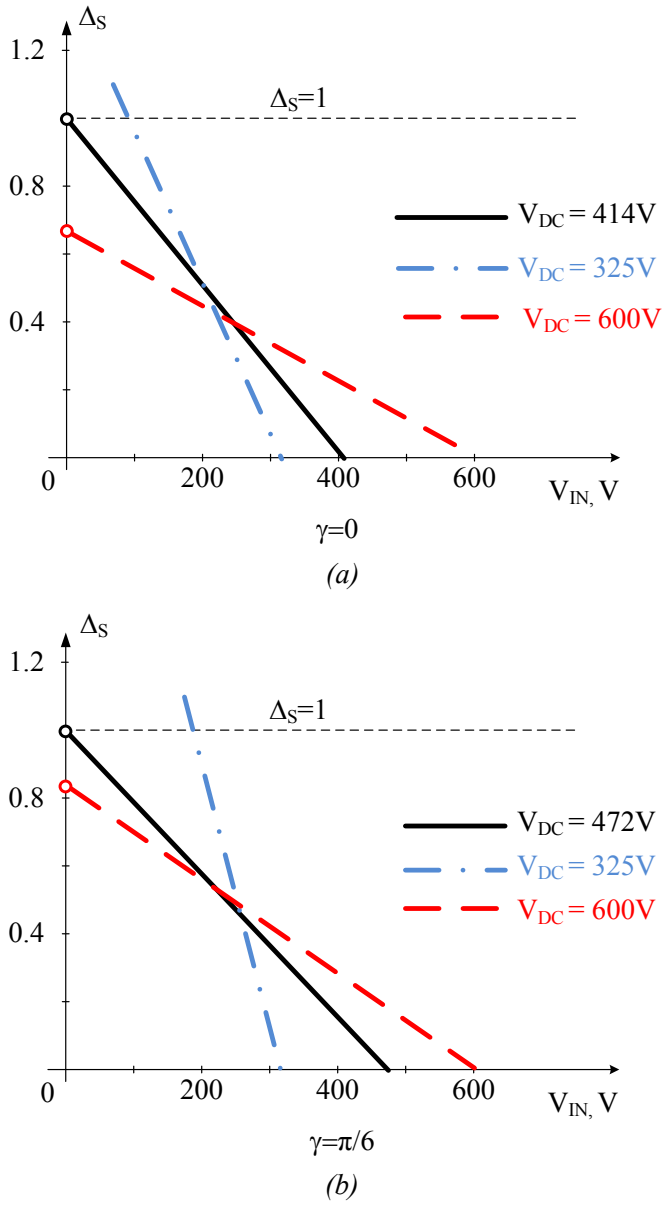


Fig. 7. Boost capability of the proposed hysteresis control approach with different parameters: $\gamma = 0$ (a), $\gamma = \pi/6$ (b).

In the 3L topology, as can be seen, an increasing angle γ leads to a decreasing input voltage operation range. The benefit of the 3L topology is the quality of the output current. This phenomenon is demonstrated in Fig. 7 *b*.

Fig. 7 *b* enables us to predict that an optimal dependence between the auxiliary band ratio Δ_S and the input voltage V_{IN} with maximum dc-link utilizing performance exists. The minimum value of V_{DC} for each V_{IN} can be found. When V_{IN} is very low, the highest value of the auxiliary band ratio (Δ_S=1) can maintain the required boost level. From (14) that curve can be derived analytically. On the other hand, minimum dc-link voltage is limited by the amplitude of the grid voltage.

Fig. 8 illustrates presented above reasoning. In the first region, Δ_S=*1* and V_{DC} declines from a maximum value to V_M. In the second region, $V_{DC} = V_M$ and Δ_S is decreasing from 1 to 0. Both regions correspond to the boost mode. Finally, the third region meets classical hysteresis control in the buck mode.

IV. Simulation and Experimental Feasibility Study of The Proposed Hysteresis Methods

To verify all theoretical predictions, several simulations and experimental tests were carried out. Fig. 9 shows the case study system. The ZS and qZS networks with an H-bridge inverter were chosen for the simulation study with synchronous sampling. Passive elements are the same for both cases.

This inverter was connected to the grid through a simple L-filter. Regulated dc power supply was used as the input voltage. Table I shows the parameters used for the simulation and the experimental setup.

The PSIM software was used for our simulation analysis. Fig. 10 shows the first simulation results of the study of the boost capability along with dc-link utilization. Similar to Fig. 8, it shows the hysteresis band and the dc-link voltage dependences versus the input power. The main goal was to define a minimum dc-link voltage with a sinusoidal injected to the grid current. An open loop control system with manual tuning Δ_S was used.

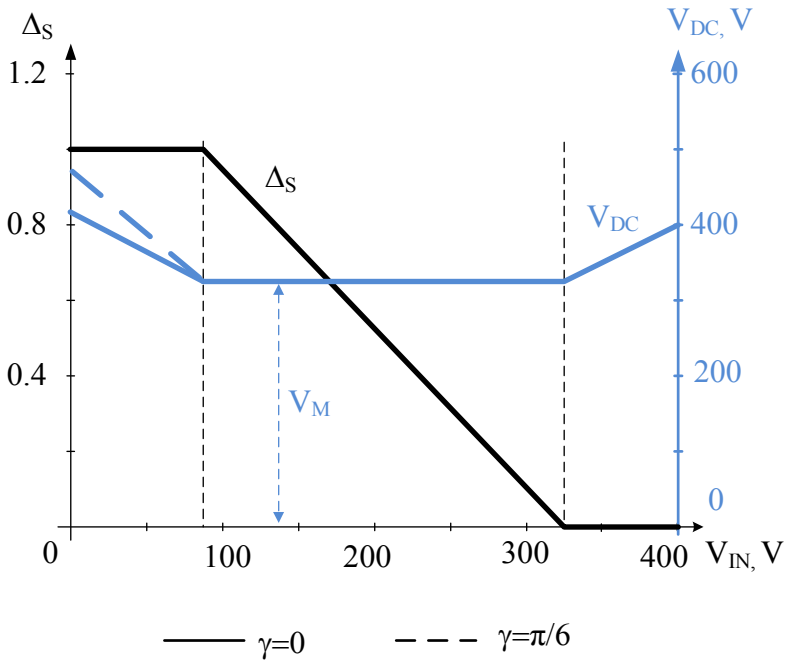


Fig. 8. Voltage boost capability of the proposed hysteresis control approach with different parameters: $\gamma = 0$ (a), $\gamma = \pi/6$ (b).

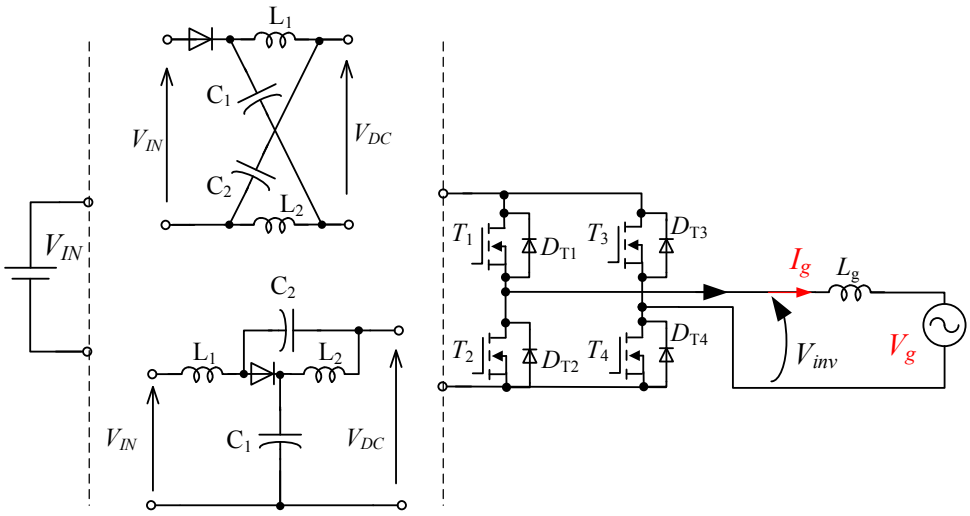
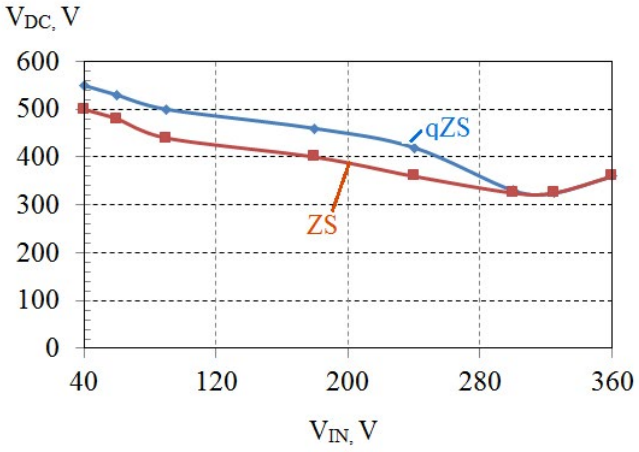
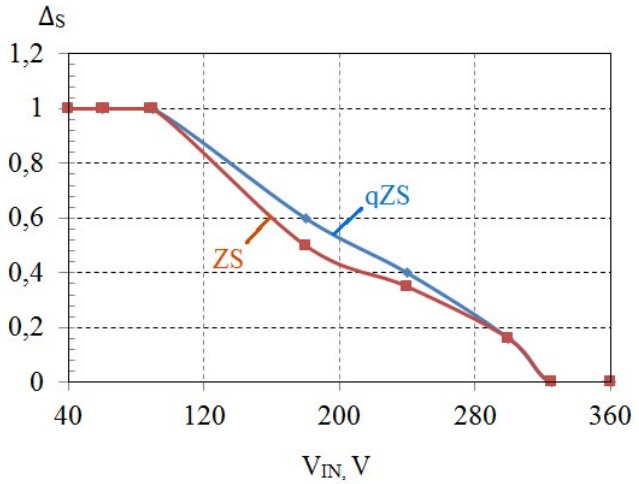


Fig. 9. Single-phase ZS/qZS inverter.



(a)



(b)

Fig. 10. Simulated results on dc-link utilization: (a) dc-link voltage and (b) shoot-through auxiliary band ratio versus input voltage.

Fig. 10 *a* illustrates the dependence of the dc-link voltage V_{DC} versus the input voltage V_{IN}, while Fig. 10 *b* shows the dependence of the auxiliary band ratio Δ_S versus the input voltage V_{IN}. Total hysteresis band was equal to *2 A*. Reference RMS output current was about *5 A* for all simulated points.

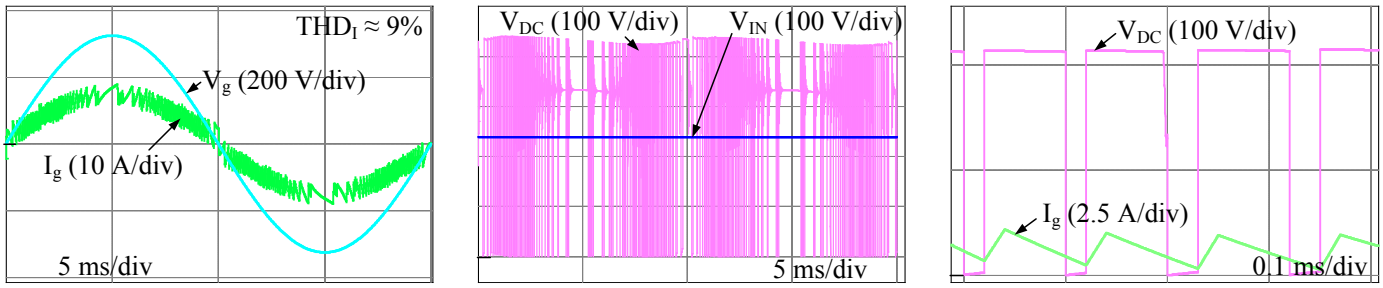
The results obtained are close to those theoretically predicted in Fig. 8. At the same time, it can be seen that in the low input voltage area, the dc-link voltage is slightly higher than that theoretically expected. If (or when) the input voltage rises, the dc-link voltage tends to that theoretically expected. It should be noted that simulation model was adjusted in accordance with the experimental prototype, taking into account all parasitic parameters.

The main reason of difference in the theoretical and simulation results lies in finite passive component values. Due to single-phase power fluctuation, capacitor oscillations in the ZS and qZS networks lead to the dc-link fluctuation. As a result, the minimum level can be significantly lower and the sinusoidal shape of the injected current is not achieved despite the high average dc-link level. At the same time, this phenomenon is insignificant at higher input voltages where high voltage boost is not required.

At the same time, Fig. 10 reveals the difference between the ZS and qZS networks. It can be seen that in the qZS network V_{DC}, the voltage and Δ_S are higher than in the ZS network. The reason is that the qZS network is sensitive to the current conduction mode. In the DCM, the desired instantaneous dc-link voltage level can be lower and therefore it requires additional increase in the auxiliary band ratio Δ_S, which in turn, causes additional rise in the peak dc-link voltage.

Figs. 11 and 12 show a set of simulation diagrams in the steady state mode for the qZS network. Fig. 11 illustrates the simulation results for the *240 V* input voltage and simple hysteresis control. Figs. 11 *a* and *b* show the grid current along with the voltage and the dc-link voltage along with the input voltage over one fundamental period respectively. Fig. 11 *c* illustrates several switching cycles of the dc-link voltage along with the output current.

Despite lower input voltage, the dc-link voltage level is sufficient to inject current to the grid. Switching frequency ranges from *5* to *25 kHz*. It should be mentioned that low switching frequency matches the zone with the largest amplitude of the grid current.



(a) (b) (c)

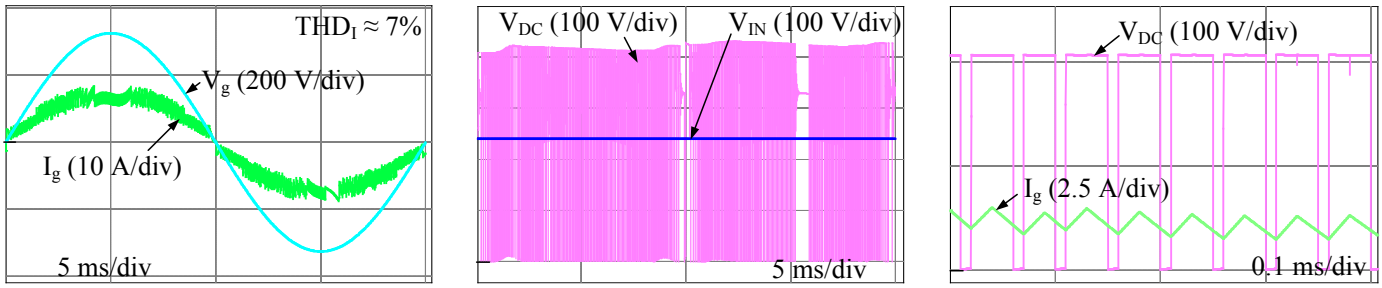
Fig. 11. Simulation waveforms of the hysteresis current control with shoot-through states in the steady state mode: grid current and voltage (a), dc-link and input voltages (b), dc-link voltage and output current (c).

Fig. 12 corresponds to the same input voltage but with modified hysteresis control. Total hysteresis band was equal to *2 A* in both cases and the auxiliary shoot-through hysteresis band was equal to *0.8 A* (Δ_S=*0.4*). RMS output current was about *5 A*. It means that by controlling that value, we can control the necessary boost capability of the inverter. That parameter and the value of the grid-connected inductance L_g strictly define the switching frequency range and the THD_I of the injected current. It can be noted that minor

changes in the THD_I of the injected current and switching frequency within hysteresis modifications. In the studied point, the THD decreased from *9 %* to *7 %*, maximum switching frequency increased from *25* to *40 kHz*.

Finally, to prove our theoretical and simulation predictions, a simple low voltage low power qZS based dc-ac experimental prototype was assembled. Passive element values corresponded to those used in the simulation. Fig. 13 shows the experimental waveforms in the steady state mode in accordance with the simulation results. A modified 2L hysteresis control method was used. The control board was based on the low cost FPGA. Fast external AD converters enable high sampling frequency (*250 kHz*) to be achieved.

The grid current and the grid voltage are depicted in Fig. 13 *a.* The RMS value of the grid voltage was about *58 V* and current was *2.5 A*, and the injected power was about *150 W*.

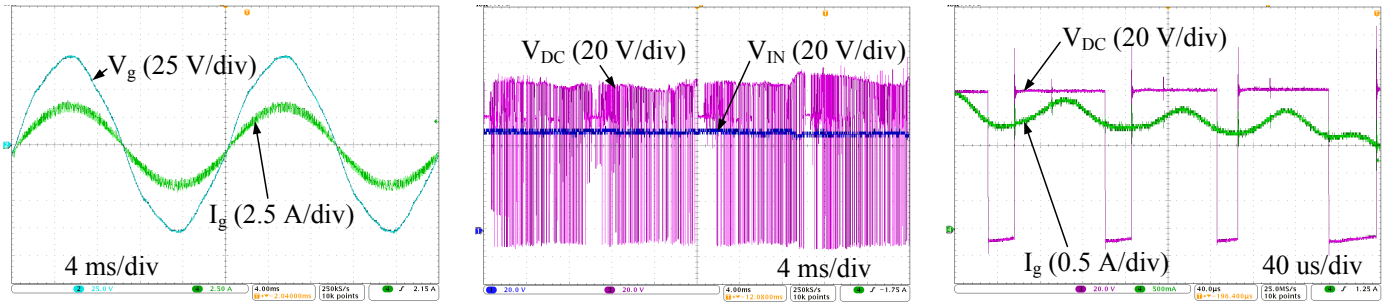


(a) (b) (c)

Fig. 12. Simulation waveforms of the modified hysteresis current control with shoot-through states in the steady state mode: grid current and voltage (a), dc-link and input voltages (b), dc-link voltage and output current (c).

The dc-link voltage and the input voltage are shown in Fig. 13 *b*. It confirms the presence of shoot-through states along with the dc-link boost. At the same time, Fig. 13 *c* illustrates the hysteresis shoot-through algorithm. Several shoot-through states, when the dc voltage is equal to zero, are applied when current flows through the auxiliary shoot-through hysteresis band. Input voltage was equal to *70 V*, dc-link amplitude voltage reached *110 V*. Maximum total hysteresis band was set to *0.5 A*, while the maximum auxiliary shoot-through hysteresis band was *0.2* (*0.1 A* – absolute value).

It should be noted that in this simple case, the switching frequency was in a range from almost zero to *10 kHz*, while the measurement sample frequency was *250 kHz*.



(a) (b) (c)

Fig. 13. Experimental waveforms in the steady state mode: grid current and voltage (a), dc-link and input voltages (b), dc-link voltage and output current (c).

V. CONCLUSIONS

This paper presents a novel hysteresis current control technique with the distribution of shoot-through states. The operation principle of the novel algorithm is provided by a detailed description and the steady state analysis.

The steady state analysis for the ZS/qZS network showed that such approach provides a wide input voltage gain regulation capability along with maximum dc-link utilization. Several possible modifications presented are intended for current quality improvement and extension for three- and multi-level inverter applications.

Simulation and experimental results confirmed our theoretical hypothesis. Slight deviations from the results theoretically expected are explained by the assumptions that were accepted within analysis.

This control algorithm could be applied in any buck-boost single-stage inverter topology with IS network where shoot-through states are required. Due to the features presented above it is well suited for any renewable energy grid-connected applications.

Hysteresis current control based closed-loop system for grid-connected applications can be easily realized by means of a low cost FPGA or a microcontroller. Also, such advanced control functions as active filtering can be easily implemented in such control strategy.

For practical reasons, switching frequency range must be limited during the design in order to avoid possible resonance problems in the IS network and the output filter. In the case of IS networks (qZS) with continuous input current, attention should be paid to careful passive element design in order to avoid the DCM. This phenomenon and general dc-link voltage fluctuations in any IS network require deeper analysis.

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TABLE I. SYSTEM PARAMETERS USED FOR SIMULATION AND EXPERIMENTS

Input DC voltage V_{IN}	40-360 V
Output AC RMS voltage V_M	230 V
Capacitance value of the capacitors C_1, C_2	2 mF
Inductance value of the inductors L_1, L_2	580 μH
Inductance of the filter inductor L_f	2.2 mH
Sampling frequency	250 kHz