Three-Level T-type qZ Source Inverter as Grid-Following Unit for Distributed Energy Resources

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***Abstract*—Distributed energy resources (DER) such as solar photovoltaics (PV) are required to achieve a high performance and an efficient use of generated renewable power in grid-integrated applications, both in normal and fault operating conditions. In this paper, a grid-following multi-functional control strategy for a three-phase three-level T-type quasi-impedance source inverter (3L-T-type qZSI) is studied through simulation and experimental tests. The grid-following functionality is achieved by a PI-based *dq* current controller for the active and the reactive power tracking. A PI-based dc controller is used for the dc-link voltage control by taking advantage of the quasi-impedance source network ability for input voltage boosting. The dc-ac power conversion is accomplished through a space vector pulse-width modulation (SVPWM) with inner capacitors voltages balancing capability and minimum common-mode voltage generation. Besides, a low voltage ride-through strategy was implemented to fulfill the fault requirements imposed by the Spanish standard. The simulation and experimental results demonstrate the above-mentioned functionalities and validate the stability and good dynamic response of the grid-connected 3L-T-type qZSI. Thus, this work supposes a novel contribution due to the few works previously reported in the literature concerning the performance of this relatively recent inverter topology in grid-tied applications.**

***Index Terms*— dc-link voltage control, distributed generation, grid-connected converters (GCCs), low voltage ride-through (LVRT), quasi-impedance source (qZS), three-level T-type inverter.**

I. INTRODUCTION

DISTRIBUTED power generation systems (DPGs) are recently acquiring a fundamental role in the ecological transition to renewable energies. Among these DPGs, photovoltaic (PV) systems are a promising option, where the grid integration represents an essential aspect for an efficient utilization of the generated power. In this context, transformerless grid-connected inverters have proved to be a suitable option for the power conversion, manifesting a different behavior than conventional generators that spins synchronously with the grid frequency. This difference mainly relies in the fact that most inverter-based DPGs act as grid-following (GFL) converters, using a phase-locked-loop (PLL) to synchronize with the grid voltage phase. As opposed to GFL converters, other solutions use the concept of grid-forming (GFM) control by generating their own internal voltage reference angle, acting in a more similar way to that of synchronous generators (SGs) [1]. GFM converters play a fundamental role in microgrids where the voltage and frequency of the grid must be maintained stable. However, GFM converters are more susceptible to instability problems under stiff grid operating conditions compared to their GFL counterparts. Since weak electrical grids such as microgrids are not within the scope of this work, the GFL structure will be the one addressed throughout the paper for its application in DPGs.

Among GFL multilevel converter solutions, the combination of a three-level T-type (3L-T-type) inverter with a quasi-impedance source (qZS) network has demonstrated to be a suitable single-stage configuration for renewable energy applications. This relatively recent multilevel inverter topology offers benefits such as reduced switching losses, enhanced harmonic distortion and simple structure [2], [3], compared to other existing solutions in the literature. In addition, the qZS network makes it possible to dispense with the dc-dc step-up converter, integrating both the boost ability and the dc-ac power conversion in a single power stage. This boosting ability is possible due to the short-circuit of the inverter leg branches during the so-called shoot-through (ST) switching states. The qZS network merges as an enhanced topology within the family of impedance-source (Z-source) inverters, with the advantage of continuous input current and reduced component ratings [4]. Since the first proposal by Peng [5], this family of converters have been subject to wide research in the literature. A complete overview of the different Z-source topologies is carried out in reference [6]. Several studies delve into the combination of two symmetrical qZS network with three-level inverters [7]–[9],

This research was funded in part by the Junta de Extremadura (Spain) with the project (IB20165), the program "Ayudas Talento" (TA18003), the "Funding for Research Groups" (GR21162), and by national (Portugal) funds through FCT - Fundação para a Ciência e a Tecnologia, under project UIDB/50021/2020. (Corresponding *author: C. Roncero-Clemente).*

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highlighting the promising characteristics of this inverter topology. Nonetheless, the design of modulation techniques for the three-phase three-level T-type quasi-impedance source inverter (3L-T-type qZSI) has several challenges to overcome, such as reducing the common-mode voltage (CMV), balancing the neutral point voltage, and obtaining low harmonic distortion in the output currents. References [10], [11] present a comparative overview of different modulation schemes for three-level Z-source inverters. Roughly, the control algorithms for multilevel converters can be classified into two main groups: (a) carrier-based pulse-width modulation and (b) space vector pulse-width modulation (SVPWM). The first group generates phase voltages by comparing high-frequency carrier waveforms to the reference voltage. Authors in [12] propose a modified carrier-level-shifted modulation for the 3L-T-type qZSI implementing capacitor voltage imbalance compensation. On the contrary, SVPWM techniques employ a vectorial representation of the inverter switching states. Reference [13] analyses a SVPWM algorithm addressing neutral point voltage control. Both CMV reduction and neutral-point control is achieved in [14] through a simple implementation of the SVPWM technique. This algorithm implements both functionalities by using the redundant small vectors in order to mitigate the inner capacitors voltages imbalance.

Although many works regarding the modulation techniques of the 3L-T-type qZSI can be found in the literature mostly focused in off-grid examples, few studies address the control of the qZS inverter topology in grid tied applications. Furthermore, the results presented by most of these studies were obtained by means of simulations, motivating the validation under experimental tests. Authors in [15] analyze through a simulation study a control system based on proportional-resonant (PR) current controller in the αβ-stationary reference frame for a grid-connected 3L-T-type qZSI. A model predictive control was simulated in grid-connected application for a 3L-T-type qZSI in [16]. Reference [17] analyze through simulation the performance of a grid-connected 3L-T-type qZSI employing a PR current regulator in combination with a LCL filter.

Dynamic models based on small signal analysis of the asymmetrical qZS have been developed to effectively design closed-loop control methods for grid integration. Authors in [18] propose a two-stage control method for a qZS two level grid-connected inverter, decoupling the dc-side and the ac-side controllers. In this reference, the dc-side controller modeling is carried out by small-signal analysis of the qZS dynamic behavior. This dynamic model for a single qZS network can be effectively extended to the design of the 3L-T-type qZSI dc control loop in grid-tied application. Regarding the ac side control, the current regulation can be achieved in a synchronous *dq* reference frame, in a stationary *abc* or in *αβ* reference frame. In reference [19], several current controllers for grid-connected applications in DPGs are analyzed. More recent works regarding the ac side control for the 3L-T-type inverter topology can be found in [20]–[23]. A decoupled *dq* current control is a popular approach since simple proportional-integral (PI) controllers can be used in combination with a voltage feed-forward component for an improved harmonic performance [24]. This approach was applied in a qZS-cascaded H-bridge inverter in order to perform optimal control of active and reactive power through day and night operation of the system [25]. Also, stability issues associated with the application of wide-bandgap (GBW) devices in Z-source grid-tied inverters have been addressed. The dynamic interaction between the qZS network and the LCL output filter has been investigated in gallium nitride (GaN)-based qZS grid connected inverter [26].

In addition to basic functionalities such as grid synchronization, dc side voltage control or output current regulation, the increase in the penetration level of PV systems demands a new generation of multi-functional PV control inverter systems, capable of providing intelligent services such as fault-ride-through or reactive power compensation. New grid requirements for grid-connected PV systems are being established in many countries, imposing that PV power plants must stay connected to the grid in case of a voltage sag during a fault scenario. This capability, known as low voltage ride-through (LVRT), is intended to support the grid recovery through the injection of reactive current by the PV system. The authors in [27] carry out a comprehensive review of LVRT strategies under different types of grid faults in PV systems.

Essentially, grid faults can occur under balanced or unbalanced conditions. Current regulation methods discussed above such as the PI controller in the *dq* reference frame or the PR controller are suitable only under balanced voltage fault conditions. More advanced control methods have been proposed for grid-tied inverters under unbalanced fault condition [28], [29].

Additionally, references [30] and [31] both present photovoltaic inverters with LVRT capability, [30] for a three-phase T-type topology, while [31] deals with a single-phase quasi-Z source 2-level topology. Nevertheless, unlike the present paper, none of the existing research addresses the dynamic response and performance with the combination of a double quasi-Z source network and a three-phase 3-level T-type inverter topology under a low-voltage fault.

Summarizing, the main contribution of this paper are as follows:

1. The implementation of a GFL inverter using a single-stage 3L-T-type qZS topology, which simultaneously boosts and adjusts the dc-link voltage to the variable PV voltage. Besides, it can operate in the maximum power point tracking (MPPT) mode or directly configuring active and reactive power setpoints and stay connected to the grid during a voltage sag, thus achieving a proactive LVRT capability.

2. The extension and application of the modulation technique described in [14] and the design of effective PI-based regulators for the control of a 3L-T type qZS GFL inverter, achieving the necessary internal capacitor voltage balancing and CMV reduction, while maintaining the simplicity of the implementation.

Both simulation and experimental results are presented to demonstrate the aforementioned functionalities under normal grid conditions and under grid fault operation to demonstrate the satisfactory behavior of the converter following the LVRT requirements imposed by the Spanish grid code.

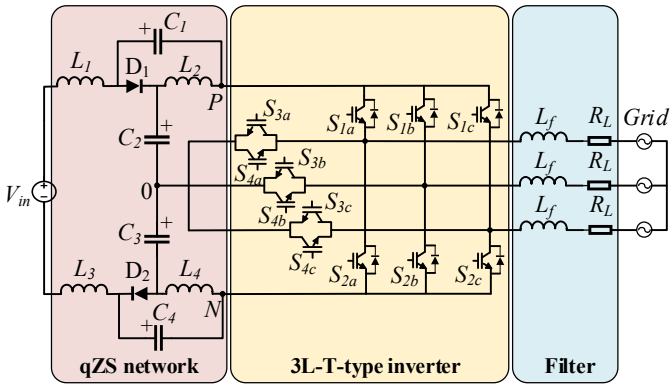


Fig. 1. Grid connected 3L-T-type qZSI scheme.

The rest of the paper is organized as follows: Section II presents a description of the overall system and the converter topology. Section III describes the SVPWM modulation technique. Section IV discusses the ac side and dc side controls design. Then, simulation and experimental results are presented in Section V and Section VI, respectively. Finally, conclusions are drawn in Section VII.

II. System Description

Fig. 1 shows the schematic circuit of the grid-connected 3L-T-type qZSI. An intermediate stage formed by two symmetric qZS networks is connected between the PV array input voltage source and the 3L-T-type inverter. Finally, an inductive output filter links the inverter to the electrical grid.

A representation of the complete closed-loop control system highlighting the implemented functionalities is depicted in Fig. 2. The instantaneous grid voltages v_{abc} and the grid currents i_{abc} are fed to the control strategy in order to perform the active and the reactive power control. The voltage v_{PV} and the current i_{PV} at the PV array are also measured to be fed to the controller when performing MPPT operation. Additionally, the measurements of the capacitor voltages v_{C2} and v_{C3} allow the implementation of the dc-link voltage (v_{DC}) control and the inner capacitors C_2 and C_3 imbalance mitigation. The control strategy block, highlighted in yellow, generates the pulse-width modulation (PWM) signals for the inverter power-switches. The converter PWM signals generation is determined by the different functionalities implemented in the presented strategy, marked in bold in Fig. 2. Additional functionalities regarding GFL converters such as temperature control, harmonic compensation or anti-islanding protection are shown in grey, denoting that they are not within the scope of this work. A detailed description of the control strategy is illustrated in Fig. 3. Grid Synchronization is achieved through a second-order generalized integrator-phase locked loop (SOGI-PLL), based on frequency adaptive quadrature-signals generation [32]. The use of PLL structures for synchronization is a distinctive characteristic in GFL converters, as opposed to GFM converters, which synchronize with the grid by the power-synchronization mechanism of SGs [33]. This aspect may reduce the stability margin of GFL converters in low short-circuit ratio (SCR) grids where GFM converters show better performance.

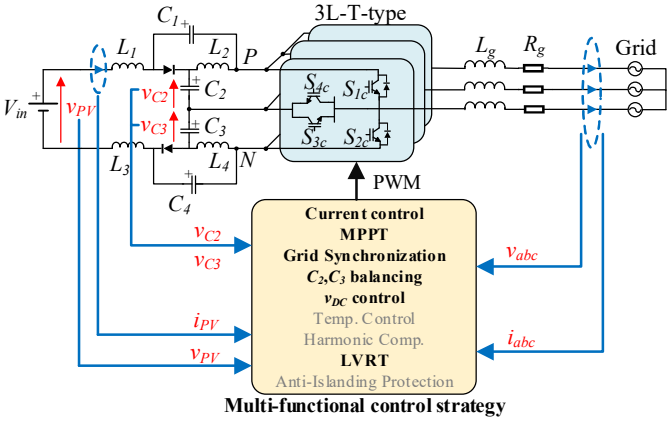


Fig. 2. Generalized system configuration.

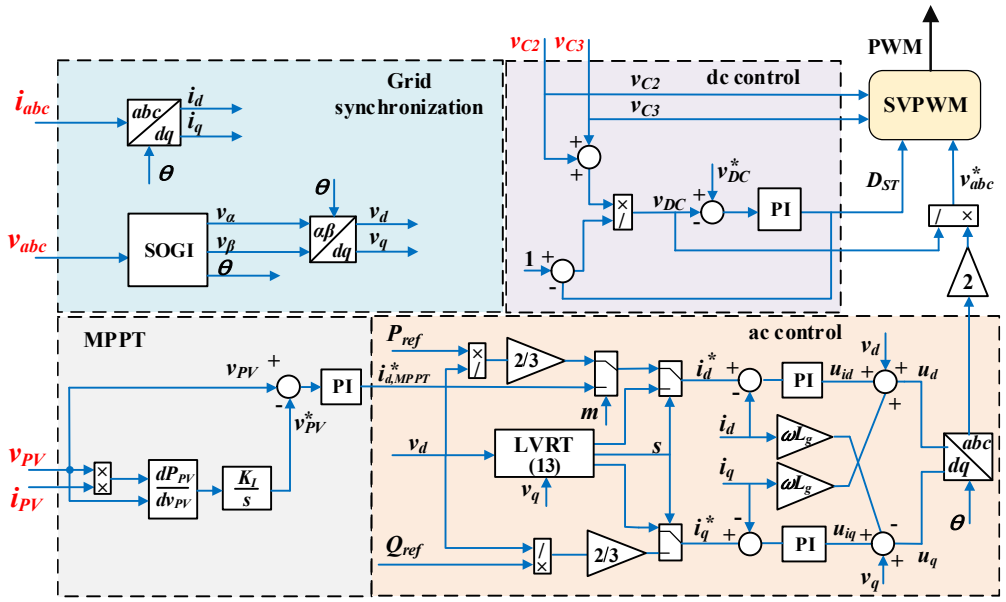


Fig. 3. Block diagram of the inverter control strategy.

However, GFL converters demonstrate more stable synchronization in stiff grids with high SCR. Once synchronization is accomplished, the ac control allows the active and the reactive power control by means of a decoupled PI-based *dq* current controller. By working in the *dq* reference frame, the control scheme can be simplified by using PI controllers to make line current components (i_d and i_q) to track the reference currents i_d^* and i_q^*. Furthermore, a decoupled PI-type scheme is used with decoupling paths $-\omega L i_d$ and $+\omega L i_q$ in order to cancel the cross-couplings between *d* and *q* quantities, which is known to improve the performance of the controller, achieving an accurate current tracking [34].

Current references i_d^* and i_q^* are calculated from the active and reactive power references, denoted as P_{ref} and Q_{ref}. P_{ref} can be set manually or determined by the MPPT control block highlighted in grey when signal *m* is activated, by means of the *d*-axis current component setpoint $i_{d,MPPT}^*$. The MPPT algorithm implemented is based on a cascade dual-loop. The outer loop involves the MPPT algorithm itself, which is based on the incremental conductance (IncCond) technique. The algorithm calculates the slope of the P-V curve and then integrates the result multiplied by an integral gain K_I. The output of the MPPT algorithm provides the reference PV voltage v_{PV}^* for a PI-based inner control loop. This PI controller outputs $i_{d,MPPT}^*$ for the ac controller.

In the case of LVRT operation of the converter, the signal *s* is activated, and the current references are calculated by the LVRT block, which is described in detail in Section V. The controller receives the measured grid current components i_d, i_q and calculates the error value by subtracting them from the current references. The PI controllers apply a correction to this error based on the proportional and integral terms by generating the input voltages references v_{abc}^* of the SVPWM block.

Finally, the dc control is fed with capacitor voltages v_{C2} and v_{C3} in order to perform an estimation of v_{DC}. A PI controller is used to track the reference value v_{DC}^* by acting on the shoot-through duty cycle (D_s). Additionally, measured v_{C2} and v_{C3} are used by the SVPWM block in order to perform the capacitors voltage imbalance compensation.

III. Space Vector Modulation Method

A simple SVPWM scheme addressing several functionalities is used in this work for the PWM signals generation. A detailed description can be found in [14]. Fig. 4 shows the space vector representation for a three-phase three-level inverter, indicating the employed sector division. The reference voltage vector (V_{ref}) is generated through a combination of the nearest three space vectors, for which the duty cycle and sequence of generation over a modulation period need to be calculated. The capacitors imbalance compensation is achieved by incorporating small vectors to the large, medium and zero (LMZ) vector sequence for a positive imbalance ($v_{C2} > v_{C3}$) in sectors highlighted in grey and a negative imbalance ($v_{C2} < v_{C3}$) in sectors highlighted in white. A PI controller is used to adjust the duty cycle of the small vector. Furthermore, CMV reduction is accomplished by only applying the non-crossed out small vectors in Fig. 4 as they are associated with the lower CMV values. A lower CMV reduces the leakage currents of the converter, contributing to prevent damage from indirect contacts.

Finally, the qZS network boosting ability is possible through the insertion of ST states, which consist in the short-circuit of the dc-link through the inverter branches. This ST states are inserted during the zero-vectors dwelling times in order to maintain the volt-second average of the converter.

During the ST states, the energy provided by the input power source is stored in the inductors of the qZS network to be transferred to the capacitors and the grid during the non-ST states. The boost factor (*B*) defined as the ratio between the peak value of v_{DC} and the input voltage V_{in} can be calculated from the analysis of the qZS network in steady state operation, assuming a continuous conduction mode [7]:

$$B = \frac{\hat{v}_{DC}}{V_{in}} = \frac{1}{1\text{-}2D_S}. \tag{1}$$

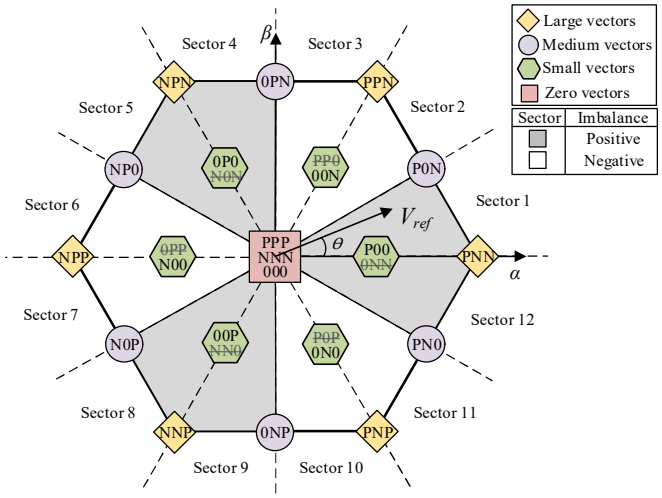


Fig. 4. Sector division of the SVPWM technique.

TABLE I
Operation Parameters and Design Values of the Converter

Parameters	Value
Input voltage V_{in}	250 V
dc-link voltage setpoint (v_{DC}^*)	300 V
Rated grid voltage ($V_{gn,rms}$)	230/3 V
Load current (I_0)	7 A
ac frequency	50 Hz
Maximum nominal current (I_N)	11 A
Switching frequency (f_{sw})	10 kHz
Shoot-through duty cycle (D_S)	0.08 p.u
Capacitors C_1, C_2, C_3, C_4	3.3 mF
Capacitors resistance (R_1, R_2, R_3, R_4)	0.1
Inductors resistance (r_1, r_2, r_3, r_4)	0.35
Inductors L_1, L_2, L_3, L_4	2 mH
Filter inductance (L_g)	5.88 mH
Filter resistance (R_g)	0.4 Ω

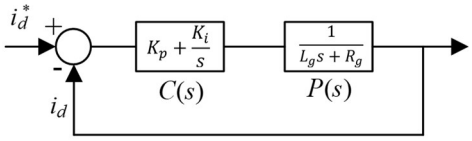


Fig. 5. Block diagram of the current controller in the *d*-axis.

IV. Controllers Design

Both the dc-side and the ac-side controllers have been designed according to the experimental design values of the power converter and the operation parameters, which are summarized in Table I. A scaling of the nominal conditions was employed in the experimental tests by setting the experimental grid voltage $V_{gn,rms}$ to one third of the rated grid voltage (230 V in Europe).

A. DQ Current Controller

The PI-based current controller has been designed in the *dq* synchronous reference frame, which causes the system dynamics given by (2) to be highly coupled. u_d, u_q, v_d and v_q are the inverter output voltages and the grid voltages in the *dq*-frame, respectively. The angle Θ used in the *dq* transformation is extracted from the SOGI-PLL. Although the dynamics of the SOGI-PLL can affect the response of the system due to perturbations in the grid voltage, they have been left out of consideration to simplify the stability analysis.

$$L\begin{bmatrix}\frac{di_d}{dt}\\ \frac{di_q}{dt}\end{bmatrix} = \begin{bmatrix}u_d\\ u_q\end{bmatrix} - \begin{bmatrix}R_g & -\omega L_g\\ -\omega L_g & R_g\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix} - \begin{bmatrix}v_d\\ v_q\end{bmatrix}. \tag{2}$$

Since the existing cross-coupling between the *d*-axis and *q*-axis can affect the dynamic performance of the controller, the decoupling control scheme illustrated in the ac block in Fig. 3 was implemented as follows:

$$\begin{bmatrix}u_d\\ u_q\end{bmatrix} = \begin{bmatrix}-\omega L_g & \omega L_g\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix} + \begin{bmatrix}v_d\\ v_q\end{bmatrix} + \begin{bmatrix}u_{id}\\ u_{iq}\end{bmatrix}, \tag{3}$$

where u_{id} and u_{iq} account for the control outputs of the PI control scheme. By substituting equation (3) in (2), the new decoupled system is:

$$L_g\begin{bmatrix}\frac{di_d}{dt}\\ \frac{di_q}{dt}\end{bmatrix} = -\begin{bmatrix}R_g & R_g\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix} + \begin{bmatrix}u_{id}\\ u_{iq}\end{bmatrix}. \tag{4}$$

From (4), the closed-loop diagram of the current controller in the *d*-axis is simplified as depicted in Fig. 5, where $P(s)$ accounts for the plant of the system and $C(s)$ for the PI controller with a proportional gain K_p and an integral gain K_i. The overall closed-loop transfer function of the negative feedback system $G_{cl}(s)$ is defined as:

$$G_{cl}(s) = \frac{K_p\, s + K_i}{L_g s^2 + (R_g + K_p)s + K_i}. \tag{5}$$

Re-arranging the second-order transfer function obtained in (5), the values of damping ratio δ and natural frequency ω_n are derived as follows:

$$s^2 + 2\delta\omega_n s + \omega_n^2 = s^2 + \frac{R_g + K_p}{L_g}s + \frac{K_i}{L_g}, \tag{6}$$

$$\begin{cases}\delta = \dfrac{R_g + K_p}{2L_g\omega_n}\\ \omega_n = \sqrt{\dfrac{K_i}{L_g}}\end{cases}. \tag{7}$$

From (7), the values of the proportional gain K_p and integral gain K_i can be obtained by using the following equation:

$$\begin{cases}K_p = 2\delta\omega_n L_g - R_g\\ K_i = L_g\omega_n^2\end{cases}. \tag{8}$$

By properly selecting δ and ω_n the bandwidth (BW) of the system can be fixed, which should be one or two decades lower than f_s. For $\delta = 0.707$ and $\omega_n = 1728$ rad/s the gains of the PI controller are $K_p = 14$ and $K_i = 17555$. However, the presence of a zero in (5) causes a unit step response with a 20% overshoot (M_p). Aiming for a M_p below 10%, the K_p of the controller can be increased to a value of 30 in order to achieve a slower response of the system. For $K_p = 30$ and $K_i = 17555$ the new overshoot and bandwidth are $M_p = 7\%$ and BW = 890 Hz. The Bode diagram and the step response of the closed-loop system is depicted in Fig. 6 (a) and (b), respectively. The same gains can be used in the *q*-axis controller for simplicity.

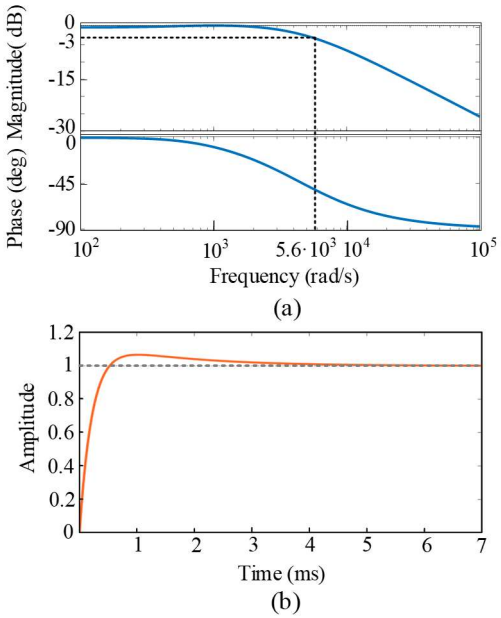


Fig. 6. Stability analysis of the ac control loop: (a) Bode diagram. (b) Unit step response.

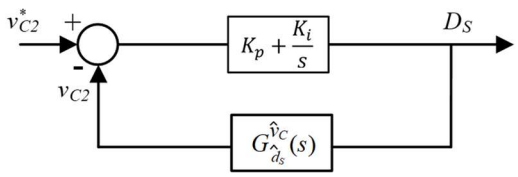


Fig. 7. Small-signal control model of capacitor voltage v_{C2}.

B. MPPT Controller

As stated previously, the error between the measured voltage at the PV array v_{PV} and the reference voltage provided by the MPPT algorithm v_{PV}^* is fed to a standard PI controller with the following transfer function:

$$PI_{MPPT}(s) = \frac{K_{I,MPPT}}{s} + K_{P,MPPT} \tag{9}$$

Due to the difference in voltage and power level between the simulation and experimental tests, slightly different values of the proportional and integral gains have been selected by trial and error for the simulation and experimental study. Additionally, the sample time T_{s_MPPT} and the integral gain K_I of the IncCond algorithm were selected to achieve a fast and smooth response. Table II summarizes the main parameters of the MPPT controller.

TABLE II
PARAMETERS OF THE MPPT CONTROLLER

	$K_{I,MPPT}$	$K_{P,MPPT}$	$T_{s,MPPT}$	K_I
Simulation	1	0.002	1/50 s	10
Experimental	4	0.005	1/50 s	10

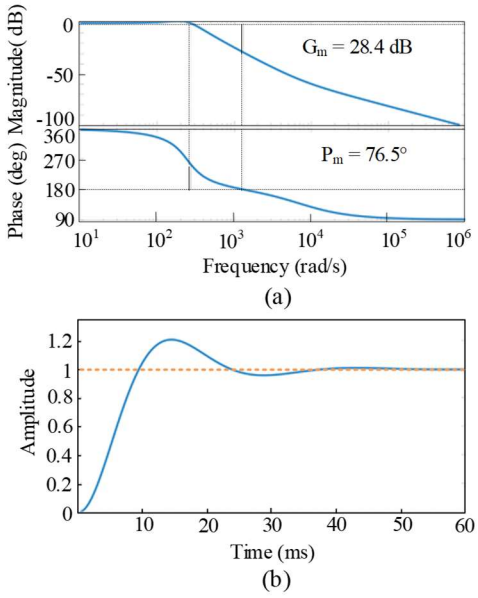


Fig. 8. Stability analysis of the dc control loop: (a) Bode diagram. (b) Unit step response.

C. DC-Link Voltage Controller

The value of v_{DC} is regulated by controlling D_s in order to track the desired reference value. For this purpose, a PI-based controller is used. The value of D_s is fed back for the estimation of v_{DC} from the voltages of the two internal capacitors (v_{C2} and v_{C3}), following equation (10) as represented in Fig. 3:

$$v_{DC} = \frac{v_{C2} + v_{C3}}{1 - D_s}. \tag{10}$$

The dynamic behavior of v_{DC} will therefore depend on the dynamic response of v_{C2} and v_{C3} to the small-signal variation of D_S. The small-signal model of the single qZS network derived in [18], [35] can be extended to the case of study involving two symmetric qZS networks, considering that each qZS network is affected by half of V_{in}. In order to obtain the small-signal model, perturbations $\hat{d}_S$, $\hat{v}_{in}$ and $\hat{i}_0$ are added to D_S, V_{in} and I_0, respectively, causing variations in the dynamic state variables of the qZS network. Assuming $\hat{V}_{in}$ and $\hat{I}_0$ to be zero and applying the principle of inductor volt-second and capacitor charge balance in steady state, the small-signal transfer function from the remaining variable $\hat{d}_S$ to the state variables can be obtained. For simplification, only the upper qZS network is considered for the controller design. According to the small-signal model, identical transfer functions from D_S to capacitor voltages v_{C1} and v_{C2} can be derived (11).

$$G_{\hat{d}_s}^{\hat{v}_c} = \frac{LI_{11}s + (R+r)I_{11} + (1-2D_S)V_{11}}{LCs^2 + (R+r)Cs + (1-2D_S)^2} \tag{11}$$

where $L = L_1 = L_2$, $C = C_1 = C_2$, $R = R_1 = R_2 = R_3 = R_4$, $r = r_1 = r_2 = r_3 = r_4$, $I_{11} = I_0 - 2I_L$, $I_L = \frac{1-D_s}{1-2D_s} I_0$, $v_{C1} = \frac{1-D_s}{2-4D_s} V_{in}$, $v_{C2} = \frac{D_s}{2-4D_s} V_{in}$ and $V_{11} = v_{C1} + v_{C2} - I_0 R$.

The controller and plant scheme of the control system regarding capacitor voltage v_{C2} is represented in Fig. 7. The parameters of the PI controller have been decided aiming for considerably slower dynamics in the dc-side than ac-side. This has been accomplished by having a relatively lower crossover frequency of the controller. For $K_p = 0.01$ and $K_i = 100$, the Bode diagram and the step response of the closed-loop system is illustrated in Fig. 8 (a) and (b) respectively, where a positive gain margin (G_m) and a positive phase margin (P_m) account for the stability of the system.

V. LOW VOLTAGE RIDE THROUGH

As discussed in Section I, the ability of PV systems to stay connected to the grid and avoid a high loss of power during a voltage sag is known as LVRT capability. Similar grid code connection requirements have been developed and imposed in many countries such as Spain, Germany, Italy and Japan, where PV systems account for a large proportion of electricity generation. In addition to the ability of the power inverter to remain connected to the grid during the fault, PV systems are required to inject reactive power into the grid in order to support the voltage recovery of the sag. In the presented control strategy, LVRT operation has been addressed according to the Spanish grid code requirements [36].

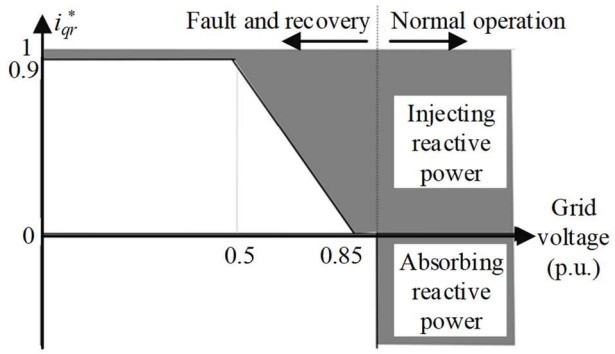


Fig. 9. PV system requirements during LVRT operation.

The code dictates that the system must provide the maximum possible current during both the fault and subsequent recovery period, considering that the operating point of the installation must be located within the shaded area in Fig. 9. In order to detect a voltage sag in the grid, the voltage amplitude v_{gp} is monitored according to (12). For this purpose, the components v_d and v_q obtained from the SOGI-PLL are used.

$$v_{gp} = \sqrt{v_d^2 + v_q^2}. \tag{12}$$

The percentage value of current reference in the q-axis, denoted as I_{qr}^*, is calculated as follows:

$$\begin{cases} I_{qr}^* = 0, & v_{gp} > 0.85\ V_{gn} \\ I_{qr}^* = -\dfrac{18}{7}\cdot\dfrac{v_{gp}}{V_{gn}} + \dfrac{18}{7}\cdot 0.85, & 0.9V_{gn} \geq v_{gp} > 0.5V_{gn} \\ I_{qr}^* = 0.9, & v_{gp} \leq 0.5\ V_{gn} \end{cases} \tag{13}$$

where V_{gn} is the rated peak voltage of the grid. Finally, the injected current references i_q^* and i_d^* are calculated from the maximum available current of the power converter (I_N), according to the following equations:

$$i_q^* = I_N \cdot I_{qr}^*, \tag{14}$$

$$i_d^* = \sqrt{1 - I_{qr}^{*\,2}} \cdot I_N. \tag{15}$$

VI. Results and Discussion

In this section, simulation and experimental results are presented to demonstrate the previously described functionalities implemented in the control strategy, as well as the proper dynamic and steady-state response of the grid connected 3L-T-type qZSI. The operation parameters detailed in Table I correspond to the chosen parameters for the experimental tests. However, simulation tests have been carried out for the nominal grid conditions ($V_{gn,rms}$ = 230 V) with V_{in} = 670 V, v_{DC}^* = 800 V and L_g = 10 mH. The rest of the parameters in Table I remain identical both in the simulation and in the experimental tests.

In order to illustrate the behavior of the system for several active and reactive power setpoints, four different operation time intervals have been defined in Table III, where the active power setpoint (P_{ref}), the reactive power setpoint (Q_{ref}) and the corresponding d-axis and q-axis reference current components ($i_d^*$and i_q^*) are shown for the simulation and experimental cases.

The inner capacitors voltages balancing and the v_{DC} control functionalities are activated during all the operation time intervals. The simulation and experimental results are discussed in subsection VI-A and subsection VI-B, respectively.

A. Simulation Results

The inverter system model and the control strategy have been simulated using PLECS (version 4.4.5, Plexim electrical engineering software) simulation tool.

Fig. 10 shows the three grid currents (i_a, i_b, i_c) injected to the grid during the four operation time intervals and the transient views for each active and reactive power steps. The power converter switching starts at the beginning of the 1st interval with zero active and reactive power reference. Ideally, the grid currents should be zero in this scenario. Active power is injected to the grid during the 2nd interval and the 3rd interval where the displayed transients show the dynamic performance of the current controller during a current reference step. Finally, reactive power is consumed in the 4th interval where the grid voltage of phase a is depicted in the transient view to illustrate the phase shift of the phase current with respect to the phase voltage. It is worth noting that the total harmonic distortion (THD) of i_a improves as the magnitudes of the active and the reactive power setpoints increase, as shown in Fig. 11, where the steady-state waveforms of the grid currents are presented for the 2nd, 3rd and 4th intervals.

To illustrate the proper performance of the current controller, the d-axis and q-axis measured current components and their corresponding setpoints for each operation time interval are shown in Fig. 12. The transient views of the reference current steps demonstrate the fast underdamped response of the system during both active and reactive power setpoints variation.

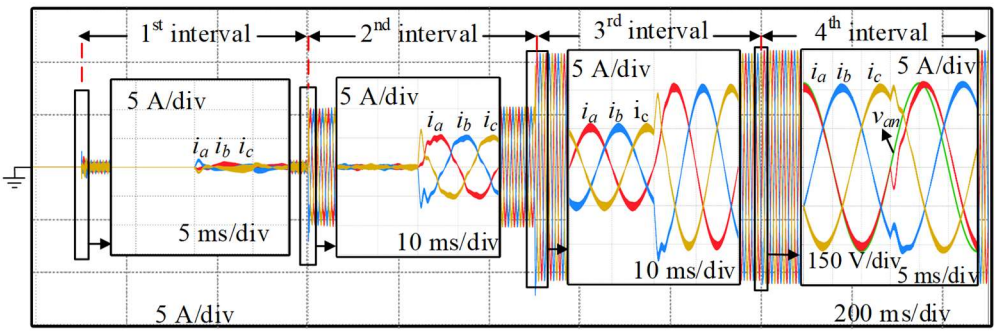


Fig. 10. Simulation results: grid currents i_a, i_b, i_c with transient details for each operation time interval with v_{DC} control and inner capacitor voltages balancing.

This article has been accepted for publication in IEEE Journal of Emerging and Selected Topics in Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2022.3193258

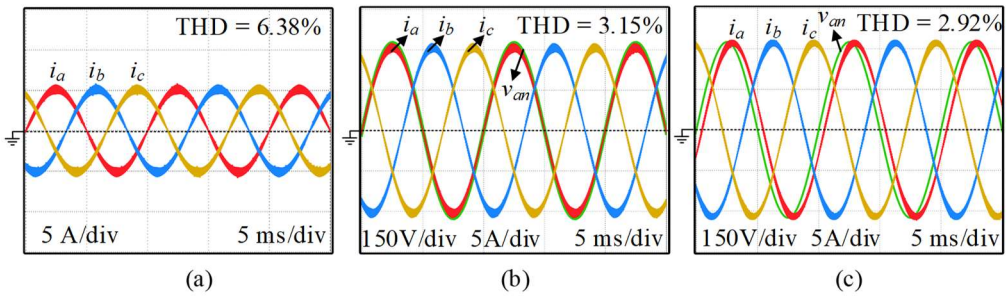


Fig. 11. Simulation results: (a) Grid currents i_a, i_b, i_c in the 2nd interval. (b) Grid currents i_a, i_b, i_c and phase voltage v_{an} in the 3rd interval. (c) Grid currents i_a, i_b, i_c and phase voltage v_{an} in the 4th interval.

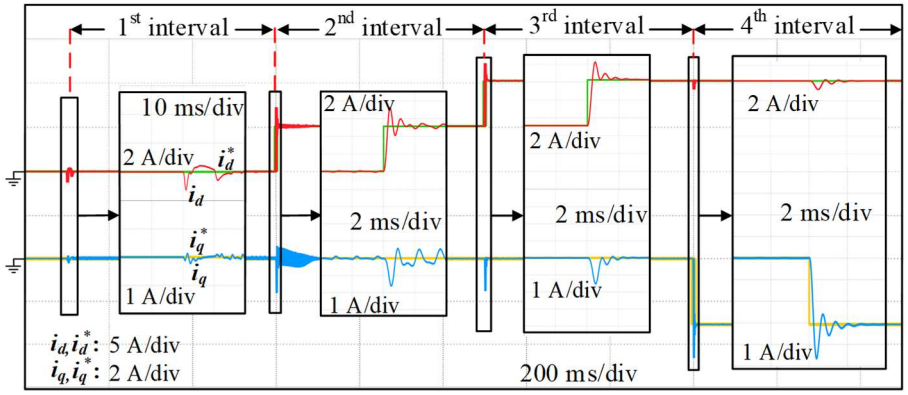


Fig. 12. Simulation results: *dq* components of the measured grid currents (i_d, i_q) and the grid current setpoints (i_d^*, i_q^*) with transient details for each operation time interval.

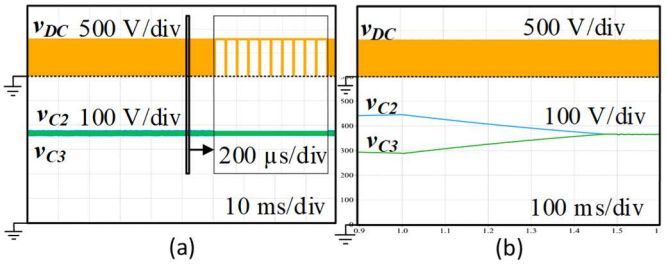


Fig. 13. Simulation results: (a) dc-link voltage v_{DC} and capacitor voltages v_{C2} and v_{C3} in the 4th interval. (b) dc-link voltage v_{DC} and inner capacitors voltages (v_{C2}, v_{C3}) evolution during imbalance control.

The capacitors voltages v_{C2} and v_{C3}, and the dc-link voltage v_{DC} in the 4th interval are shown in Fig. 13 (a). A detailed view of these waveforms shows the uniformly distributed ST states causing a drop of v_{DC} to zero during the short-circuits of the dc-link through the inverter branches. By effectively controlling the value of D_S, the tracking of the reference value (v_{DC}^* = 800 V) is achieved. Fig. 13 (b) shows a transient of the same waveforms during the capacitor voltages balancing after a positive imbalance scenario ($v_{C2} > v_{C3}$) in the 4th interval. For this purpose, a resistor of 470 Ω connected in parallel to capacitor C_3 has been used to produce the imbalance, while maintaining the corresponding controller inactive. This results in a voltage difference between C_2 and C_3 of approximately 150 V. Once the imbalance control is activated, the voltage difference between both capacitors is rapidly compensated without any undesired overcurrent or overvoltage.

The dc-side control performance is demonstrated in Fig. 14 (a) where a transient of variables V_{in}, v_{C2}, v_{C3} and D_S during an input voltage drop in the 4th interval is shown. This situation is intended to emulate a possible temporary change of the PV solar irradiance, where V_{in} drops from 670 V to 560 V. In order to maintain the reference value of v_{DC}, the controller responds by increasing the value of D_S during the voltage sag period. Figs. 14 (b) and 14 (c) show detailed views of variables v_{DC} and V_{in} before the voltage dip and during the voltage dip, respectively. As a result of a higher value of D_S during the voltage dip, the ST states exhibit larger time widths with respect to the nominal input voltage operation.

TABLE III
POWER AND CURRENT REFERENCES FOR EACH OPERATION TIME INTERVALS

	1st interval		2nd interval		3rd interval		4th interval	
	Sim.	**Exp.**	**Sim.**	**Exp.**	**Sim.**	**Exp.**	**Sim.**	**Exp.**
P_{ref} (W)	0	0	2500	850	5000	1700	5000	1700
Q_{ref} (var)	0	0	0	0	0	0	1500	500
i_d^* (A)	0	0	5.12	5.23	10.25	10.45	10.25	10.45
i_q^* (A)	0	0	0	0	0	0	-3.07	-3.07

The THD values for the nominal power conditions in the 3rd and 4th intervals are below the allowable limit of 5% as dictated by the standards IEEE 1574/IEC 61727 [37], [38].

In Fig. 15, the obtained CMV (Fig. 15 (a)) is compared with the one (Fig. 15 (b)) generated by the well-known approach that involves the alternating upper and lower shoot-through (UST-LST) states [39] during the 3rd interval. The CMV is limited to a value of $\pm v_{DC}/6$ in the SVPWM modulation employed in this study, whereas it takes a value of $\pm v_{DC}/3$ in the carrier-based UST-LST modulation, thus reducing the operational risk by decreasing the potential leakage current flowing between the PV array and the ground [40].

Fig. 16 shows the MPPT dynamic and steady-state performance, where the input voltage source was replaced by a solar PV array model composed by BP-365 modules in a configuration of 40 modules in serial and 2 strings in parallel. The evolution of v_{PV}, i_{PV}, v_{DC} and D_S is represented in Fig. 16 (a). v_{PV} evolves from the open-circuit voltage V_{oc} to the maximum power point voltage V_{mp}. Correspondingly, i_{PV} evolves from zero to the maximum power point current I_{mp}. It can be observed that D_S progressively increases simultaneously to the v_{PV} decreasing below 800 V in order to maintain v_{DC}^*. Fig. 16 (b) shows i_a, i_b, i_c and v_{an} at the point of maximum power. The current THD is 3.11%, which complies with the standards [37], [38]. The I-V and P-V characteristic curves are represented in Fig. 16 (c) and Fig. 16 (d), where P_{mp} accounts for the power at the point of maximum power and I_{sc} accounts for the short-circuit current.

Finally, the LVRT operation of the converter is illustrated in Fig. 17 (a). The evolution of the measured variables i_a, v_{an}, i_d and i_q are represented for a grid voltage sag of a value of $v_{gp} = 0.65V_{gn}$ and a duration of 55 ms in the 3rd interval. After the fault has occurred, the SOGI system takes a brief time to resynchronize with the grid until the new i_d and i_q setpoints are correctly calculated.

A detailed view of the grid fault is depicted in Fig. 17 (b). It can be observed that once synchronization is achieved, reactive power is injected to the grid following the code requirements described in Section V. In order to compensate for the increase of i_q, i_d is reduced to prevent the nominal injected current from exceeding the maximum current of the converter (I_N = 11 A).

B. Experimental Results

Identical experimental tests to those of the simulation study were conducted in order to validate experimentally the converter performance and the functionalities of the control strategy. Fig. 18 shows the experimental laboratory setup. The 12MB150VX-120-50IGBT module from FUJI has been used to implement the 3L-T-type inverter, composed of 12 RB-IGBTs and driven by the driver board AT-NP 3-level 12-in-1 from FUJI. The control strategy and the switching signal generation for the converter were programmed and obtained by using the rapid prototype controller RT Box 1 from Plexim, which is equipped with analogue and digital breakout boards. The USM-3IV sensor modules from Taraz TECHNOLOGIES were employed to measure the current and voltage variables to be fed back to the controller. The programmable grid emulator GE15 from CINERGIA is used as the electrical grid, generating the grid fault for the LVRT operation.

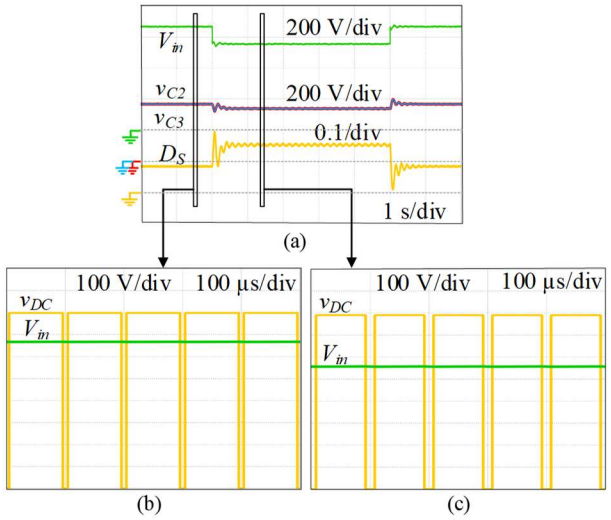


Fig. 14. Simulation results: (a) Evolution of capacitor voltages v_{C2}, v_{C3} and shoot-through duty cycle D_S during an input voltage (V_{in}) drop and subsequent recovery. (b) Detailed view of the dc-link voltage v_{DC} before input voltage (V_{in}) drop. (c) Detailed view of the DC-link voltage v_{DC} after an input voltage drop.

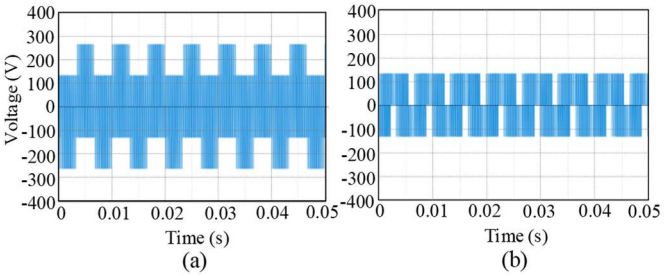


Fig. 15. CMV obtained in simulations. (a) By using the conventional UST-LST modulation strategy, limited to ±1/3 of the dc-link voltage. (b) By using the SVPWM proposed in [14] limited to ±1/6 of the dc-link voltage.

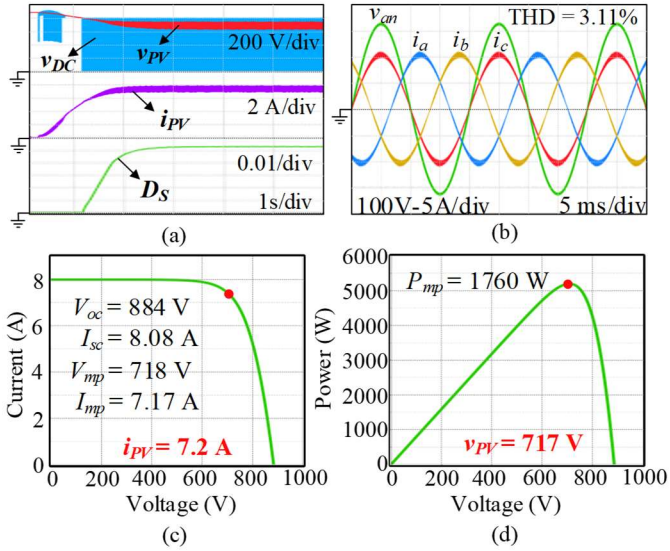


Fig. 16. Simulation results: (a) Evolution of v_{DC}, $v_{PV, iPV}$ and D_S during MPPT. (b) Grid currents i_a, i_b, i_c and phase voltage v_{an} in the point of maximum power. (c) I-V characteristic curve of the solar array. (d) P-V characteristic curve of the solar array.

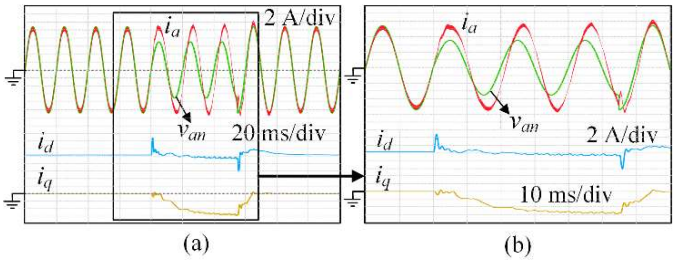


Fig. 17. Simulation results during LVRT operation with v_{gp} = 0.65V_{gn}: (a) Grid phase current i_a, phase-to-neutral grid voltage v_{an}, d-axis and q-axis components of the grid currents (i_d, i_q). (b) Detailed view of the same variables (i_a, v_{an}, i_d, i_q).

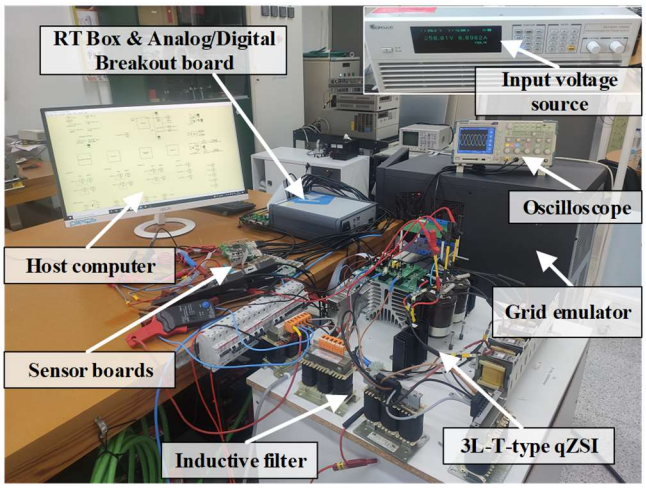


Fig. 18. Full laboratory setup.

The system is supplied with a dc input voltage source, the 62000H-S Solar array Simulator from Chroma. The experimental results were obtained by both the PLECS environment through the RT-box 1 and the Tektronix TPS2024B digital oscilloscope with Tektronix P5100A voltage probes and A622 current probes.

Fig. 19 shows the experimental results of the complete sweep involving the four operation time intervals described in Table II, where the grid currents i_a, i_b and i_c are represented. The system response to active and reactive power reference steps can be observed in the transients between intervals. The steady-state waveforms of these variables are shown in Fig. 20 for the 2nd, 3rd, and 4th intervals. A low THD value equal to 3.89% for the current of phase a is obtained for the nominal power in the 4th interval, and a value of 4.29% in an operational point below the nominal one in the 3rd interval. These values comply with the THD limit of 5% fulfilling the standards [37], [38].

In accordance with these results, a fast and stable response of the current controller is demonstrated in Fig. 21, where the d-axis and q-axis measured current components and their corresponding reference values are shown. Additionally, the transients displayed between intervals exhibit a proper overshoot and settling time of the system for each current reference step. It can be noted that slightly higher overshoot values during the transients with respect to the design value of M_p = 7% can be observed. This difference can be explained due to the implementation of low pass-filters to mitigate the noise when measuring i_d and i_q, and the perturbations caused by the SOGI-PLL dynamics.

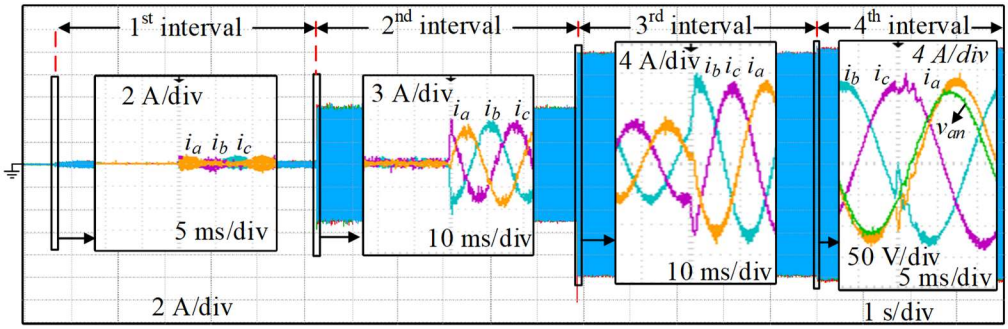


Fig. 19. Experimental results: grid currents i_a, i_b, i_c with transient details for each operation time interval with v_{DC} control and inner capacitor voltages balancing.

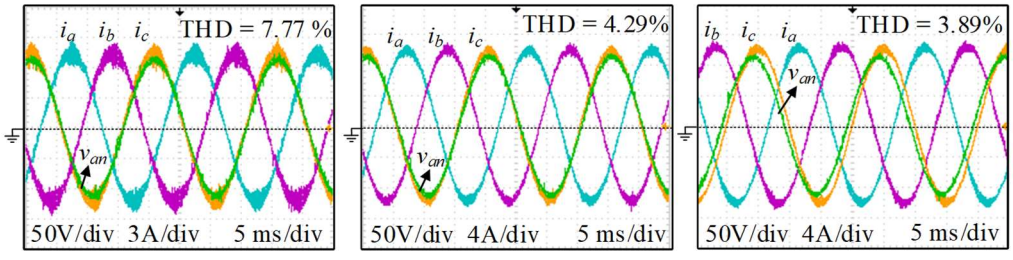


Fig. 20. Experimental results: (a) Grid currents i_a, i_b, i_c and v_{an} in the 2nd interval. (b) Grid currents i_a, i_b, i_c and v_{an} in the 3rd interval. (c) Grid currents i_a, i_b, i_c and v_{an} in the 4th interval.

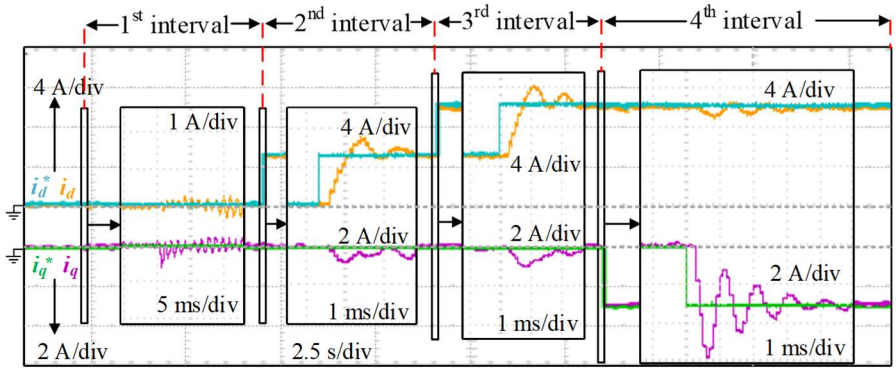
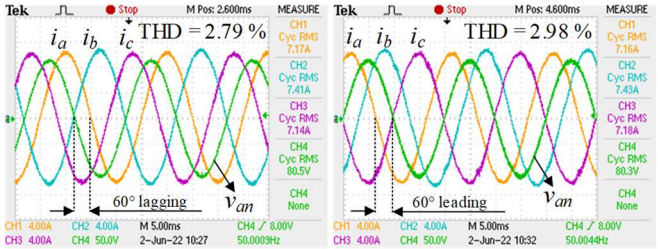
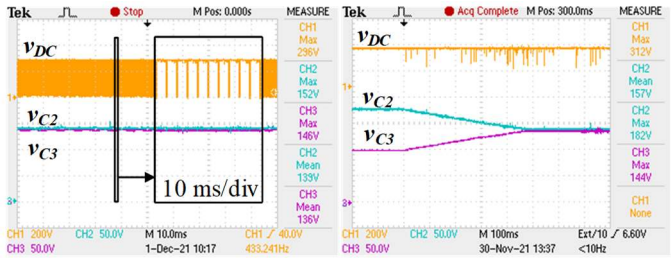


Fig. 21. Experimental results: *d*-axis and *q*-axis components of the measured grid currents (i_d, i_q) and the grid current setpoints (i_d^*, i_q^*) with transient details for each operation time interval.



(a) (b)

Fig. 22. Experimental results: (a) Grid currents i_a, i_b, i_c and v_{an} with FP equal to 0.5 lagging. (b) Grid currents i_a, i_b, i_c and v_{an} with FP equal 0.5 leading.



(a) (b)

Fig. 23. Experimental results: (a) dc-link voltage v_{DC} and capacitor voltages v_{C2} and v_{C3} in 4th interval. (b) dc-link voltage v_{DC} and inner capacitors voltages (v_{C2}, v_{C3}) evolution during imbalance control.

To demonstrate the ability of the converter to inject and to absorb reactive power allowing reactive power regulation, experimental tests with power factor PF equal to 0.5 lagging (Fig. 22 (a)) and PF equal to 0.5 leading (Fig. 22 (b)) around the rated power of the converter were conducted. These results fully comply with the German standard VDE-AR-N 4105 [41], which allows power factors from 0.95 leading to 0.95 lagging in the range of installed capacity of 3.68 kVA or less. Besides, the THD values obtained in these tests are below the 5% specified by [37], [38].

Fig. 23 (a) shows the experimental steady-state waveforms of v_{DC}, v_{C2} and v_{C3} in the 4th interval. A detailed view of the oscilloscope caption allows to observe the switching ST states, which cause v_{DC} to switch between zero and its peak value. This maximum value is determined by the DC controller which acts on D_S in order to track the reference value for the experiments of $v_{DC}^* = 300$ V. A similar approach to that of the simulation tests have been used to demonstrate the inner capacitor imbalance mitigation. A resistor of 470 Ω is connected in parallel to capacitor C_3 in order to generate a large positive imbalance of approximately 80 V. Once the imbalance control is activated, the evolution of capacitor voltages v_{C2}, v_{C3} and dc-link voltage v_{DC} is shown in Fig. 23 (b), where the voltage balancing is achieved in a time of roughly 500 ms.

A variation of the solar conditions of the PV generation system was simulated by programming the Chroma Solar array simulator in order to induce a voltage drop of V_{in}. The experimental response of the dc control is demonstrated in Fig. 24 (a). D_S increases from a value of approximately 0.084 to a value of 0.15 when V_{in} decreases from 250 V to 210 V. Detailed views of v_{DC} and V_{in} before and after the voltage drop are shown in Fig. 24 (b) and Fig. 24 (c) respectively, where a larger time width of the ST switching states can be observed when D_S takes a higher value.

In a similar way to the simulation study, the CMV is compared to another approach. Fig. 25 shows the obtained CMV (Fig. 25 (a), that is compared with the one (Fig. 25 (b)) generated by the UST-LST switching strategy [39] during the 3rd interval. As expected, the CMV is limited to a value of $\pm v_{DC}/6$ in the SVPWM modulation implemented in our work, whereas it takes a value of $\pm v_{DC}/3$ in the UST-LST case.

In order to validate experimentally the MPPT operation, the Chroma solar array simulator was configured to emulate the behavior of a solar array composed by BP-365 modules in a two-string configuration with 13 PV modules per string.

Fig. 26 (a) shows the evolution of v_{PV} from V_{oc} to V_{mp}. Accordingly, i_{PV} evolves from zero to the I_{mp} value. When v_{PV} decreases below 300 V, the dc-link control begins to increase D_S so that the value of v_{DC} does not fall below the setpoint of 300 V. Fig. 26 (b) shows i_a, i_b, i_c and v_{an} at the point of maximum power, where an active power of 1755 W is being injected to the grid and a THD below 5% is obtained. The I-V and P-V curves are represented in Fig. 26 (c) and Fig. 26 (d), where the main characteristic parameters of the PV array are shown. A red dot indicates the power point that the system reaches once the MPPT controller is in the steady-state regime.

Finally, LVRT operation was validated experimentally by programming in the grid emulator a voltage sag of magnitude $v_{gp} = 0.55V_{gn}$ and a duration of 60 ms in the 3rd interval. The experimental evolution of measured signals v_{an}, i_a, i_d and i_q during the LVRT operation is shown in Fig. 27 (a). Once the SOGI-PLL is synchronized, the current measured components i_d and i_q stabilize at their corresponding values, which are calculated following equations (8-11) so that the inverter provides the maximum possible current I_N. The lagging phase shift of the phase grid current with respect to the grid voltage during the fault can be observed in detail in Fig. 27 (b), which indicates that the converter is providing reactive power to support the grid recovery.

C. *Efficiency Study*

The power losses have been analyzed in order to estimate the efficiency of the overall system, both in simulation and experimentally. The simulation tool PLECS includes a domain for modeling thermal structures and accurately calculating switching and conduction losses based on the power module datasheet. The experimental estimation of the efficiency was conducted by using the equipment Newtons4th PPA5500 dedicated for this purpose.

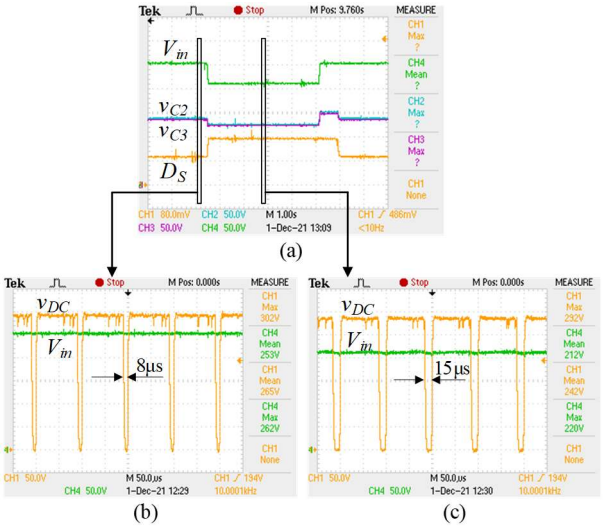


Fig. 24. Experimental results: (a) Evolution of capacitor voltages v_{C2}, v_{C3} and shoot-through duty cycle D_S during V_{in} drop and subsequent recovery. (b) Detailed view of the dc-link voltage v_{DC} before V_{in} drop. (c) Detailed view of the dc-link voltage v_{DC} after V_{in} drop.

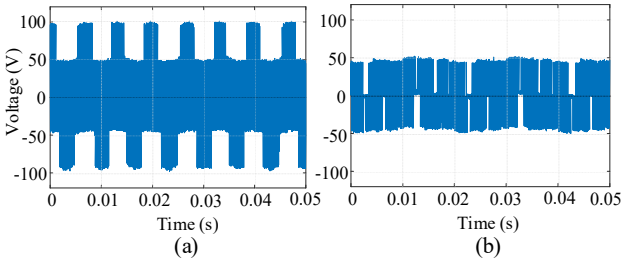


Fig. 25. CMV obtained in experiments. (a) By using the conventional UST-LST modulation strategy, limited to ±1/3 of the dc-link voltage. (b) By using the SVPWM proposed in [39] limited to ±1/6 of the dc-link voltage.

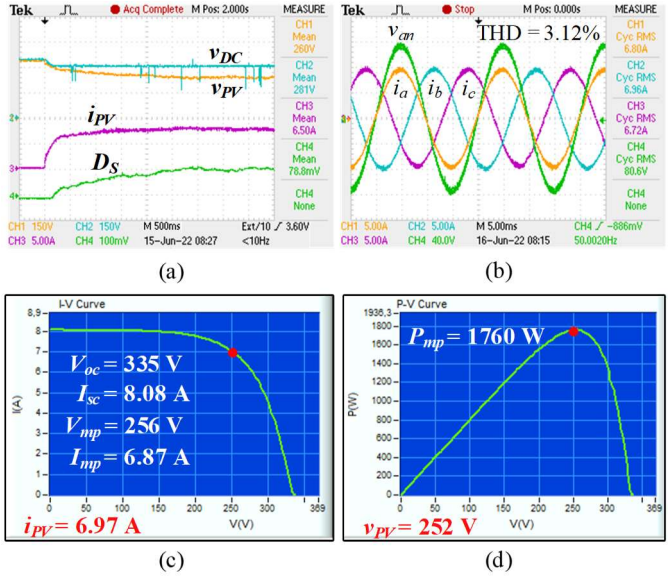


Fig. 26. Experimental results: (a) Evolution of v_{DC}, $v_{PV,\ iPV}$ and D_S during MPPT. (b) Grid currents i_a, i_b, i_c and phase voltage v_{an} in the point of maximum power. (c) I-V characteristic curve of the solar array. (d) P-V characteristic curve of the solar array.

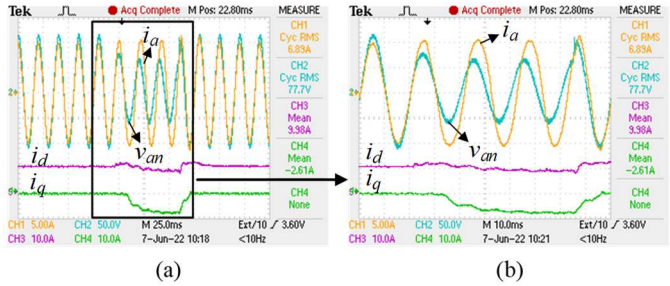


Fig. 27. Experimental results during LVRT operation with $v_{gp} = 0.55V_{gn}$: (a) Grid phase current i_a, phase-to-neutral grid voltage v_{an}, grid currents (i_d, i_q). (b) Detailed view of the LVRT operation.

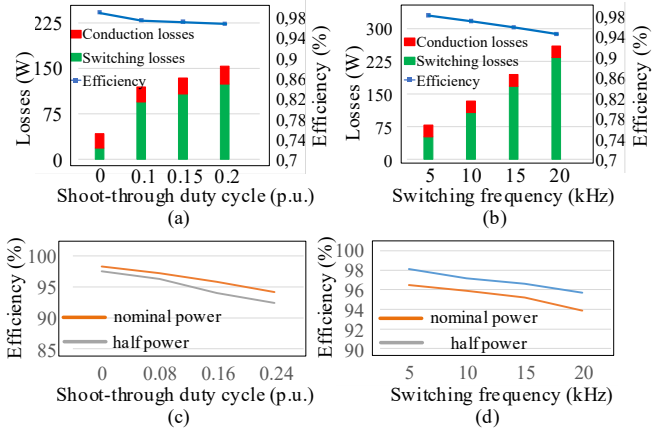


Fig. 28. Power losses and efficiency estimation in simulation under different (a) ST duty cycle and (b) switching frequency. Experimental estimation of the efficiency at nominal and half power under different (c) ST duty cycle and (d) switching frequency.

Both in simulation and experimentally, the power losses were measured for different values of D_S and f_{sw} in nominal and half power conditions. Fig. 28 illustrates the obtained results during the tests. Fig. 28 (a) and (b) show the power losses distribution and efficiency when varying D_S and f_{sw}, respectively, in simulation. The experimental results of the efficiency are also shown in Fig. 28 (c) and (d) versus D_S and f_{sw}, respectively, for nominal and half power conditions. It can be observed that an efficiency around 95% was achieved at the rated power of the converter. As expected, switching and conduction losses take higher values as both D_S and f_{sw} increase.

VII. Conclusion

The increasingly transformation of electricity generation systems towards decentralized DGs based on fluctuating renewable energies such as PV, require power conversion systems to have advanced and intelligent functionalities that improve the controllability of the systems. In this work, for the first time, a control strategy has been designed and experimentally validated implementing some of these essential functionalities, such as active and reactive power control, dc-link voltage control and LVRT operation, in a relatively novel and promising topology that brings together in a single power stage a qZS network with integrated boost capacity and a 3L-T-type inverter. In this work, the design and validation of effective ac-side and dc-side controllers, and the implementation of LVRT operation for the 3L-T-type qZSI were successfully addressed. It represents a novel contribution in the field of GFL inverters due to the scarcity of works in the literature analyzing the dynamic behavior of grid-tied Z-source-based inverter topologies.

References

[1] R. Rosso, X. Wang, M. Liserre, X. Lu, and S. Engelken, "Grid-Forming Converters: Control Approaches, Grid-Synchronization, and Future Trends—A Review," *IEEE Open Journal of Industry Applications*, vol. 2, pp. 93–109, Apr. 2021, doi: 10.1109/OJIA.2021.3074028.

[2] C. Qin, C. Zhang, X. Xing, X. Li, A. Chen, and G. Zhang, "Simultaneous Common-Mode Voltage Reduction and Neutral-Point Voltage Balance Scheme for the Quasi-Z-Source Three-Level T-Type Inverter," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 3, pp. 1956–1967, Mar. 2020, doi: 10.1109/TIE.2019.2907501.

[3] C. Qin, C. Zhang, A. Chen, X. Xing, and G. Zhang, "A Space Vector Modulation Scheme of the Quasi-Z-Source Three-Level T-Type Inverter for Common-Mode Voltage Reduction," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 8340–8350, Oct. 2018, doi: 10.1109/TIE.2018.2798611.

[4] J. Anderson and F. Z. Peng, "Four quasi-Z-Source inverters," *PESC Record - IEEE Annual Power Electronics Specialists Conference*, pp. 2743–2749, 2008, doi: 10.1109/PESC.2008.4592360.

[5] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, Mar. 2003, doi: 10.1109/TIA.2003.808920.

[6] O. Ellabban and H. Abu-Rub, "Z-Source Inverter: Topology Improvements Review," *IEEE Industrial Electronics Magazine*, vol. 10, no. 1, pp. 6–24, Mar. 2016, doi: 10.1109/MIE.2015.2475475.

[7] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electronics*, vol. 8, no. 1, pp. 1–10, Jan. 2015, doi: 10.1049/iet-pel.2013.0904.

[8] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and T. Jalakas, "Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application," *Electric Power Systems Research*, vol. 130, pp. 10–21, Jan. 2016, doi: 10.1016/j.epsr.2015.08.018.

[9] V. Ferñao Pires, A. Cordeiro, D. Foito, and J. F. Martins, "Quasi-Z-Source Inverter with a T-Type Converter in Normal and Failure Mode," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7462–7470, Nov. 2016, doi: 10.1109/TPEL.2016.2514979.

[10] A. Abdelhakim, F. Blaabjerg, and P. Mattavelli, "Modulation Schemes of the Three-Phase Impedance Source Inverters-Part I: Classification and Review," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8. Institute of Electrical and Electronics Engineers Inc., pp. 6309–6320, Aug. 01, 2018. doi: 10.1109/TIE.2018.2793255.

[11] A. Abdelhakim, F. Blaabjerg, and P. Mattavelli, "Modulation Schemes of the Three-Phase Impedance Source Inverters-Part II: Comparative Assessment," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6321–6332, Aug. 2018, doi: 10.1109/TIE.2018.2793205.

[12] C. Roncero-Clemente, E. Romero-Cadaval, M. Ruiz-Cortes, and O. Husev, "Carrier Level-Shifted Based Control Method for the PWM 3L-T-Type qZS Inverter with Capacitor Imbalance Compensation," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 8297–8306, Oct. 2018, doi: 10.1109/TIE.2018.2814020.

[13] H. Peng *et al.*, "Improved Space Vector Modulation for Neutral-Point Balancing Control in Hybrid-Switch-Based T-Type Neutral-Point-Clamped Inverters with Loss and Common-Mode Voltage Reduction," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, Dec. 2019, doi: 10.24295/CPSSTPEA.2019.00031.

[14] N. Mayorga, C. Roncero-Clemente, A. M. Llor, and O. Husev, "A Simple Space Vector Modulation Method with DC-Link Voltage Balancing and Reduced Common-Mode Voltage Strategy for a Three-Level T-Type Quasi-Z Source Inverter," *IEEE Access*, vol. 9, pp. 82747–82760, 2021, doi: 10.1109/ACCESS.2021.3087035.

[15] C. Roncero-Clemente, O. Husev, M. Ruiz-Cortes, E. Romero-Cadaval, F. Barrero-Gonzalez, and E. Gonzalez-Romera, "Grid-Connected Single-Phase 3L-T-type qZS Inverter for Renewable Energy," *IECON Proceedings (Industrial Electronics Conference)*, vol. 2019-October, pp. 5003–5007, Oct. 2019, doi: 10.1109/IECON.2019.8926888.

[16] J. Monteiro, V. F. Pires, and J. F. Silva, "A Model Predictive Control for the T-Type qZS Inverter with Capacitor Imbalance Compensation," *IECON Proceedings (Industrial Electronics Conference)*, vol. 2019-October, pp. 4715–4720, Oct. 2019, doi: 10.1109/IECON.2019.8927387.

[17] C. Roncero-Clemente, O. Husev, F. Barrero-Gonzalez, E. Gonzalez-Romera, M. I. Milanes-Montero, and E. Romero-Cadaval, "Grid-Connected Three-Phase 3L-T-type qZS Inverter for Renewable Energy," *Proceedings - 2020 IEEE 14th International Conference on Compatibility, Power Electronics and Power Engineering, CPE-POWERENG 2020*, pp. 114–119, Jul. 2020, doi: 10.1109/CPE-POWERENG48600.2020.9161512.

[18] Y. Li, S. Jiang, J. G. Cintron-Rivera, and F. Z. Peng, "Modeling and control of quasi-z-source inverter for distributed generation applications," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1532–1541, 2013, doi: 10.1109/TIE.2012.2213551.

[19] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 654–664, 2009, doi: 10.1109/TPEL.2009.2012527.

[20] X. Xing, C. Zhang, J. He, A. Chen, and Z. Zhang, "Model predictive control for parallel threelevel T-type grid-connected inverters in renewable power generations," *IET Renewable Power Generation*, vol. 11, no. 11, pp. 1353–1363, Sep. 2017, doi: 10.1049/IET-RPG.2016.0361/CITE/REFWORKS.

[21] X. Li, X. Xing, C. Zhang, A. Chen, C. Qin, and G. Zhang, "Simultaneous Common-Mode Resonance Circulating Current and Leakage Current Suppression for Transformerless Three-Level T-Type PV Inverter System," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 6, 2019, Accessed: Jan. 05, 2022. [Online]. Available: https://ieeexplore-ieee-org.ezproxy.unex.es/document/8424178/

[22] J. Hong and R. Cao, "Adaptive selective harmonic elimination model predictive control for three-level t-type inverter," *IEEE Access*, vol. 8, pp. 157983–157994, 2020, doi: 10.1109/ACCESS.2020.3020216.

[23] M. Lak, Y. T. Tsai, B. R. Chuang, T. L. Lee, and M. H. Moradi, "A Hybrid Method to Eliminate Leakage Current and Balance Neutral Point Voltage for Photovoltaic Three-Level T-Type Inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 12070–12089, Oct. 2021, doi: 10.1109/TPEL.2021.3073471.

[24] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. v. Timbus, "Overview of control and grid synchronization for distributed power generation

systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006, doi: 10.1109/TIE.2006.881997.

[25] W. Liang, Y. Liu, and J. Peng, "A Day and Night Operational Quasi-Z Source Multilevel Grid-Tied PV Power System to Achieve Active and Reactive Power Control," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 474–492, Jan. 2021, doi: 10.1109/TPEL.2020.3000818.

[26] Y. Shi, T. Kayiranga, Y. Li, and H. Li, "Exploring the LCL Characteristics in GaN-Based Single-L Quasi-Z-Source Grid-Tied Inverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 7758–7768, Oct. 2017, doi: 10.1109/TIE.2017.2694379.

[27] J. Joshi, A. K. Swami, V. Jately, and B. Azzopardi, "A Comprehensive Review of Control Strategies to Overcome Challenges during LVRT in PV Systems," *IEEE Access*, vol. 9, pp. 121804–121834, 2021, doi: 10.1109/ACCESS.2021.3109050.

[28] X. Zhao, J. M. Guerrero, M. Savaghebi, J. C. Vasquez, X. Wu, and K. Sun, "Low-Voltage Ride-Through Operation of Power Converters in Grid-Interactive Microgrids by Using Negative-Sequence Droop Control," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, 2017, Accessed: Jan. 04, 2022. [Online]. Available: https://ieeexplore-ieee-org.ezproxy.unex.es/document/7471501/

[29] Z. Shao, X. Zhang, F. Wang, R. Cao, and H. Ni, "Analysis and Control of Neutral-Point Voltage for Transformerless Three-Level PV Inverter in LVRT Operation," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2347–2359, Mar. 2017, doi: 10.1109/TPEL.2016.2565640.

[30] Y. Jiang, C. Qin, X. Xing, X. Li, and C. Zhang, "A Hybrid Passivity-Based Control Strategy for Three-Level T-Type Inverter in LVRT Operation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 4009–4024, Dec. 2020, doi: 10.1109/JESTPE.2019.2928571.

[31] M. Easley, S. Jain, M. Shadmand, and H. Abu-Rub, "Autonomous Model Predictive Controlled Smart Inverter with Proactive Grid Fault Ride-Through Capability," *IEEE Transactions on Energy Conversion*, vol. 35, no. 4, pp. 1825–1836, Dec. 2020, doi: 10.1109/TEC.2020.2998501.

[32] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," 2006. Accessed: Jan. 18, 2022. [Online]. Available: https://ieeexplore-ieee-org.ezproxy.unex.es/document/1711988/

[33] L. Zhang, L. Harnefors, and H. P. Nee, "Power-synchronization control of grid-connected voltage-source converters," *IEEE Transactions on Power Systems*, vol. 25, no. 2, pp. 809–820, May 2010, doi: 10.1109/TPWRS.2009.2032231.

[34] R. Brito, A. Carvalho, and M. Gericota, "A new three-phase voltage sourced converter laplace model," *Proceedings - 2015 9th International Conference on Compatibility and Power Electronics, CPE 2015*, pp. 160–166, Aug. 2015, doi: 10.1109/CPE.2015.7231066.

[35] Y. Liu, B. Ge, F. Z. Peng, A. R. Haitham, A. T. D. Almeida, and F. J. T. E. Ferreira, "Quasi-Z-Source inverter based PMSG wind power generation system," *IEEE Energy Conversion Congress and Exposition: Energy Conversion Innovation for a Clean Energy Future, ECCE 2011, Proceedings*, pp. 291–297, 2011, doi: 10.1109/ECCE.2011.6063782.

[36] "BOE.es - BOE-A-2006-18485 Resolución de 4 de octubre de 2006, de la Secretaría General de Energía, por la que se aprueba el procedimiento de operación 12.3 Requisitos de respuesta frente a huecos de tensión de las instalaciones eólicas." https://www.boe.es/diario_boe/txt.php?id=BOE-A-2006-18485 (accessed Jan. 19, 2022).

[37] IEEE, "IEEE STD 1547-2018," *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces*, pp. 1–138, 2018.

[38] "IEC 61727: Photovoltaic (PV) Systems - Characteristics of the Utility Interface."

[39] J. Gutiérrez-Escalona, C. Roncero-Clemente, F. Barrero-González, O. Husev, E. González-Romera, and M. I. Milanés-Montero, "Experimental evaluation of a new carrier-based modulation method for a three-level T-type quasi-impedance-source inverter," *IET Power Electronics*, vol. 15, no. 4, pp. 337–348, Mar. 2022, doi: 10.1049/PEL2.12234.

[40] L. Zhou, F. Gao, and T. Xu, "A Family of Neutral-Point-Clamped Circuits of Single-Phase PV Inverters: Generalized Principle and Implementation," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4307–4319, Jun. 2017, doi: 10.1109/TPEL.2016.2587660.

[41] *Power generation systems connected to the low-voltage distribution network: technical minimum requirements for the connection to and parallel operation with low-voltage distribution networks.* [Berlin]: VDE Verlag, 2011.

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