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Compact CMOS Wideband Instrumentation Amplifiers for Multi-Frequency Bioimpedance Measurement: A Design Procedure

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Abstract: The design of an instrumentation amplifier (IA), based on indirect current feedback and suited to electrical bioimpedance spectroscopy, is presented. The IA consists of two transconductors and a summing stage, featuring a single-stage configuration process that allows the maximum achievable bandwidth to be extended. The transconductors are linearized by means of resistive source degeneration, whereas the use of super source followers allows a reduction in the values of the source degeneration resistors. This fact leads to a decrease in the overall noise and the silicon area, thus resulting in a compact implementation. A thorough analysis of the proposed solution, accompanied by a design procedure and verified by means of electrical simulations, is also provided. Two versions of the IA, i.e., a single-ended (SE) and a pseudo-differential (PD) structure, were designed and fabricated using 180 nm CMOS technology to operate with a 1.8 V supply. The experimental results, including a BW of 5.2 MHz/8.0 MHz, a CMRR higher than 72 dB/80 dB, a DC current consumption of 139.0 µA/219.3 µA and a silicon area equal to 0.0173 mm^2/0.0291 mm^2 for the SE/PD implementation, validate the suitability of the approach.

Keywords: CMOS; indirect current feedback; instrumentation amplifier; low-voltage; resistive source degeneration; wide bandwidth

Citation: Corbacho, I.; Carrillo, J.M.; Ausín, J.L.; Domínguez, M.Á.; Pérez-Aloe, R.; Duque-Carrillo, J.F. Compact CMOS Wideband Instrumentation Amplifiers for Multi-Frequency Bioimpedance Measurement: A Design Procedure. *Electronics* **2022**, *11*, 1668. https://doi.org/10.3390/electronics11111668

Academic Editor: Yahya M. Meziani

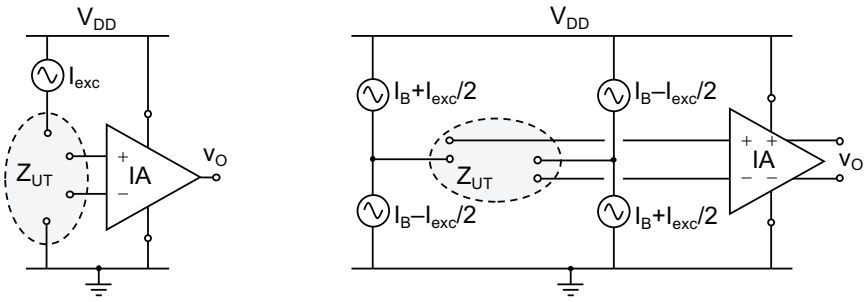
Received: 5 May 2022
Accepted: 21 May 2022
Published: 24 May 2022

1. Introduction

Electrical bioimpedance measurements allow for the characterization of biological media according to their electrical properties [1]. To this end, the biological impedance under study (Z_{UT}) is electrically excited by a sinusoidal signal, whereas the internal composition is determined in terms of the magnitude and phase angle of the corresponding response. The measurement of bioimpedance at a given single frequency is known as bioelectrical impedance analysis, whereas bioelectrical impedance spectroscopy refers to the determination of the impedance in a certain frequency range. Furthermore, the characterization of temporary alterations in the Z_{UT} and the detection of transient physiological events require the use of a multi-frequency bioimpedance analysis.

The conceptual scheme of a typical bioimpedance measurement system is illustrated in Figure 1, in single-output and differential-output versions. A sinusoidal voltage or current can be indistinctly used as an excitation signal, and it ismuch more common to base the bioimpedance analysis on an injected current signal, I_{exc}, to avoid any damage in the biological Z_{UT}. The amplitude of the excitation current signal is chosen with such a low intensity, in the range of the µAs and always lower than 1 mA, that the bioimpedance technique, in addition to being non-invasive, economic, slight, and easy-to-use, results in innocuous effects. The typical frequencies of electrical signals used in bioimpedance technology range from several hundreds of Hz to a few MHz, which is known as the β-dispersion

range. The phase angle, and therefore the reactive component of the bioimpedance in this frequency band, provides valuable information, for instance, on the state of the plasma membrane (cell membrane), which is in turn a good indicator of cellular health.



(**a**) (**b**)

Figure 1. Conceptual scheme of a bioimpedance measurement system: (**a**) single-output and (**b**) differential-output structure.

Once the Z_{UT} is properly excited, the corresponding voltage drop that is generated can be measured by means of an instrumentation amplifier (IA) [2–42], whereas signal conditioning [41,43] may be subsequently required prior to signal processing. Taking into account the characteristics of the measurement procedure described above, the features of the IA can be determined. On the one hand, the levels of the signals to be processed can be maintained within a certain range through the appropriate programming of the value of the excitation current. In this way, the voltage signal across the impedance under study will be in the mV range and, consequently, low amplification levels and a linear response over a determined input voltage range are required. On the other hand, a relatively wide bandwidth (BW) is mandatory, in order to properly operate over the entire frequency range considered in the bioelectrical impedance measurement application. It is worth pointing out that the IA, beyond providing a certain signal amplification, allows the buffering of the sample under study, as well as the adaptation of the DC levels of the signals at the Z_{UT} and at the input of the signal conditioning system. Furthermore, excessive amplification would impose a constraint on subsequent stages, as their operating voltage ranges would be correspondingly increased.

Current feedback (CF) is a suitable technique used to implement an integrated IA [2,5–7,10,15,18,22,26,33,35]. Indeed, this solution uses an input transconductor to process the input signal and an output (or feedback) transconductor to feed the output signal back in current form. By following this approach, the amplification factor of differential-mode (DM) signals can be set in a straightforward manner, whereas circuit stability can be easily ensured over a wide frequency range. Moreover, the solution leads to a circuit structure that is more compact and which has much lower power consumption as compared to the traditional three-op ampstructure [3,9]. Additionally, it is worth mentioning that the rejection of common-mode (CM) signals, evaluated by means of the CM rejection ratio (CMRR), is carried out at the input stage and can be enhanced by means of appropriate balancing and isolation techniques. Different approaches to implementing the CF in an IA have been proposed. The first IAs based on CF included a feedback loop around the input and/or the output transconductor in order to equalize the biasing currents as a function of the input signal level [2], which was later popularly known as local current feedback (LCF) [15,18,26]. In addition, direct current feedback (DCF) [4,5] was proposed to include the input and output transconductors in the same branches of the circuit implementation, in order to simultaneously reduce the power consumption and achieve higher compactness. Nevertheless, this configuration is not appropriate for operation under low supply voltages, due to the multiple stacking of devices. Alternatively, indirect current feedback (ICF) [6,33,35] was proposed for low-voltage operation, maintaining a similar operation principle as that of DCF.

An appealing characteristic of an ICF IA is that the input CM voltage range can be suited to the intended application, either by using an input voltage level shifter or by directly adjusting the aspect ratios of certain transistors. Indeed, in a single-output configuration, such as the one illustrated in Figure 1a, the Z_{UT} is usually connected to a voltage level close to ground. This imposes on the IA the capability to operate around this voltage region. On the other hand, if one is aiming at a differential structure, as is the case depicted in Figure 1b, a balanced excitation circuit must be used, which locates the input CM voltage range of the signal to be acquired by the IA around the midsupply. In both cases, the input CM voltage range of the IA must be adapted to the DC level of the signal.

In this contribution, the design of an IA based on the ICF technique that leads to a wide BW and is able to process relatively large input signals with a reduced power consumption is described. Two different realizations, namely, a single-ended (SE) and a pseudo-differential (PD) structure, are presented. Both of them have been implemented in 180 nm CMOS technology to operate with a supply voltage of 1.8 V. The experimental characterization of the silicon prototypes shows the suitability of the proposal to be used in a bioimpedance measurement system. The rest of the manuscript has been organized as follows. Section 2 deals with the structure of the ICF IA, considering both the block diagram and the transistor level implementation. A design procedure, which includes a theoretical analysis and the corresponding simulated design space, is proposed in Section 3. The experimental characterization of the two IAs is reported in Section 4 and conclusions are drawn in Section 5.

2. Principle of Operation

2.1. Block Diagram

A conceptual block diagram of an ICF IA is illustrated in Figure 2a, where G_{mI} and G_{mO} are the input and the output (or feedback) transconductors, respectively; Σ is a summing stage in which the output currents of G_{mI} and G_{mO} are added; $A(s)$ is an inverting gain stage; and β is the feedback network. The voltage-to-current (V-to-I) converter G_{mI} generates current i_I from the input voltage, $v_{I,DM}$, whereas an output current i_O is produced by the transconductor G_{mO} when a voltage $v_{SENSE} - V_{REF}$ is applied to their input terminals. The voltage v_{SENSE} is a scaled replica of the output voltage, v_O, and V_{REF} is a reference voltage used to set the DC component of v_O to the intended level. The $A(s)$ stage can be omitted, i.e., $A(s) = 1$, in order to obtain a single-stage IA, or may be implemented by means of a first-order section, so that the gain of the feedback loop can be further increased.

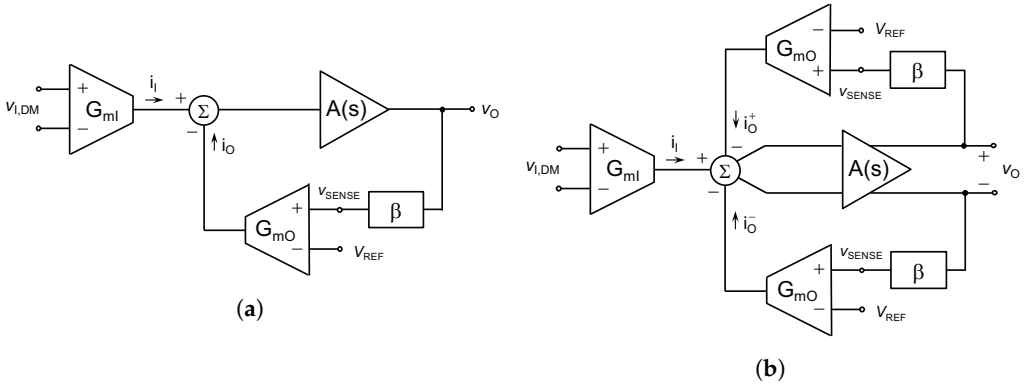


Figure 2. Block diagram of (**a**) a single-ended and (**b**) a differential ICF IA.

The transfer function of the system illustrated in Figure 2a can be expressed as:

$$H(s) \equiv \frac{v_o(s)}{v_i(s)} = \frac{G_{mI} \cdot \left(R_{out} \parallel \frac{1}{sC_{out}}\right) \cdot A(s)}{1 + \beta \cdot G_{mO}\left(R_{out} \parallel \frac{1}{sC_{out}}\right) \cdot A(s)} \quad (1)$$

where R_{out} and C_{out} are the output resistance and capacitance, respectively, of the summing stage. Provided that the loop gain around transconductor G_{mO} is sufficiently high, the voltage gain, A_v, and the BW of the IA can easily be deduced from (1) to be

$$A_v \equiv \frac{v_o}{v_{i,dm}} = \frac{1}{\beta} \cdot \frac{G_{mI}}{G_{mO}} \tag{2}$$

$$BW = \beta \cdot \frac{G_{mO}}{C_{BW}} \tag{3}$$

where C_{BW} is the capacitor used to make the feedback loop stable, i.e., a load capacitor, C_L, or a compensation capacitor, C_C, depending on whether the IA consists of one or two gain stages, respectively. The gain of the IA can be adjusted by means of the ratio of the input and output transconductances, with the latter also compromisedin the setting of the bandwidth.

In cases in which the bioimpedance measurement system follows the scheme illustrated in Figure 1b, the block diagram in Figure 2a can be easily translated into a differential structure, as depicted in Figure 2b. Even though two output transconductors are required in this case, the need for a specific block to control the CM output voltage is avoided, as detailed in Section 2.2.

2.2. Transistor Level Implementation

The transistor level implementation of a SE ICF IA, following a single-stage approach, i.e., $A(s) = 1$, and connected in a unity gain feedback configuration, that is, $\beta = 1$ and $v_O = v_{SENSE}$, is detailed in Figure 3. The principle of operation of the input and output transconductors is based on converting a voltage into a current on a resistor. Two voltage followers are used to isolate the input and output resistors, R_I and R_O, respectively, from preceding and subsequent stages. To this end, the block known as a super source follower (SSF) is used [33,35]. Indeed, the implicit feedback in an SSF, established by transistor MFI(O) around the signal driver transistor MDI(O), leads to lower output resistance of the buffer. This fact greatly reduces the impact of the source degeneration resistor on the gain of the voltage follower and allows one to decrease the value of $R_{I(O)}$. The effective transconductance generated by the input and output V-to-I cells is equal to:

$$G_{m,eff} \equiv \frac{i_{I(O)}}{v_{DM}} = \frac{2}{R_{I(O)}} \frac{1}{\left[1 + \left(1 + \frac{2}{R_{I(O)}} \frac{1}{g_{m,MDI(O)}}\right)\left(\frac{g_{o,MDI(O)} + g_{o,MSDI(O)}}{g_{mFI(O)}}\right)\right]} \approx \frac{2}{R_{I(O)}} \tag{4}$$

where $g_{m,MiI(O)}$ and $g_{o,MiI(O)}$ are the transconductance and output conductance, respectively, of transistor Mi at the input (I) or output (O) transconductor; $R_{I(O)}$ is the source degeneration resistor (R_I or R_O); and $g_m \gg g_o$ has been assumed. The first term in (4), which is inversely proportional to $R_{I(O)}$, represents the ideal transconductance of the V-to-I converter if the voltage followers were completely ideal, whereas the second contribution accounts for the loading effect of the source degeneration resistor on the voltage followers. As inferred from (4), the feedback loop implicit in the SSF greatly reduces the second-order dependence of the trasnconductance on $R_{I(O)}$, and the last term can be approximated to unity [35].

The input CM voltage range of the proposed IA can be flexibly adjusted. Indeed, the operation for input signals around the midsupply is intrinsically granted merely by setting the aspect ratio of the input devices correctly so that the MSUI transistors, working as current sources, can operate in saturation, i.e., $V_{SD,MSUI} \geq |V_{DSat,MSUI}|$. Moreover, the operation for input signals around ground, as in the case illustrated in Figure 1a, can be easily achieved through the proper sizing of the MFI transistors. Indeed, the voltage at the drain of MDI transistors, which could force their operation in the triode region, can be reduced to an appropriate level by increasing the aspect ratio of MFI transistors, thus ensuring the operation of the input drivers in saturation.

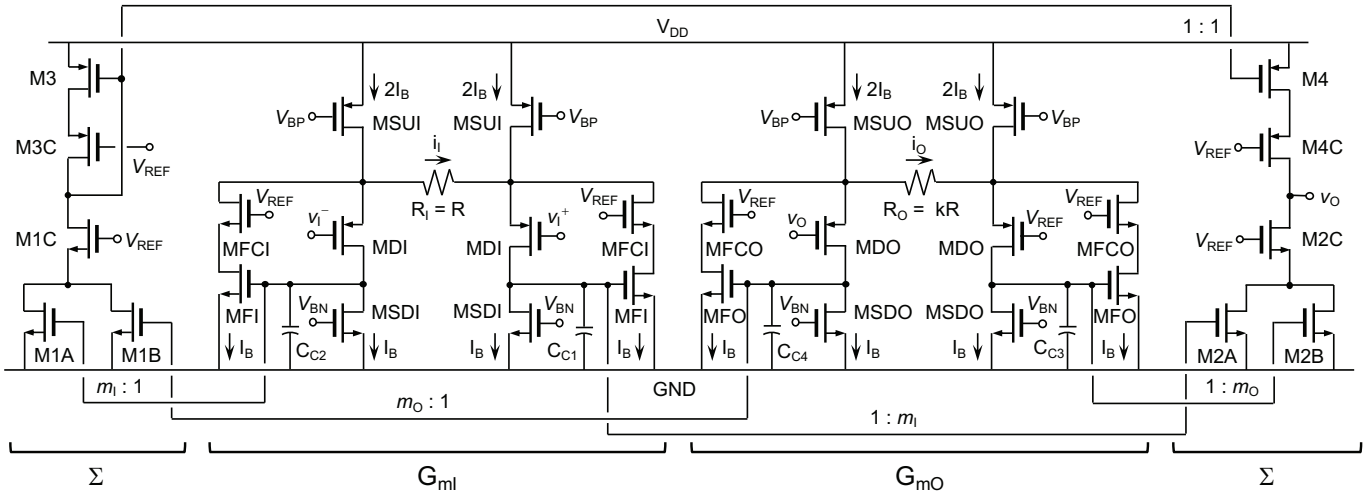


Figure 3. Transistor level implementation of the proposed single-ended ICF IA.

The current signals generated by G_{mI} and G_{mO} are conveyed to the output node of the IA by means of current mirrors with gains of $1 : m_I$ and $1 : m_O$, respectively. Furthermore, the transconductances obtained in the input and output V-to-I converters are inversely proportional to R_I and R_O, which are referred to here as $R_I = R$ and $R_O = k \cdot R$ for convenience. The current gains m_I and m_O and resistor ratio $k = R_O/R_I$ form a set of design parameters that provides the circuit with additional design flexibility in order to adjust the voltage gain and bandwidth of the IA to the intended values. Indeed, in view of the circuit implementation method proposed in Figure 3, the general transfer function in (1) for the ICF IA can be rewritten as:

$$H(s) = \frac{\frac{m_I G_{mI}}{m_O G_{mO}}}{1 + s\frac{C_L}{m_O G_{mO}}} \tag{5}$$

where C_L is the load capacitor connected to the output of the IA. Cascode MFCI(O) transistors, shown in Figure 3, allow the enhancement of the accuracy of the current mirrors with gains of m_I and m_O. In addition, capacitors C_{C1} to C_{C4} are used to optimize the phase margin of the feedback loop inherent in each SSF cell.

The differential implementation of the proposed ICF IA is shown in Figure 4. As observed, there are two output V-to-I converters, each of which is used to compare one of the two output voltages, v_O^+ and v_O^-, with the reference voltage V_{REF}. Unlike in the case of a fully-differential structure, no CM feedback (CMFB) circuit is required to control the CM component of the output voltage, as two feedback loops around the two output transconductors are established, thus stabilizing each output node individually. Therefore, the proposed differential structure can be classified as pseudo-differential. In any case, the differential structure of the input transconductor carries out the rejection of input CM signals, thus ensuring a high CMRR. As the PD ICF IA is intended to operate in the configuration illustrated in Figure 1b, operation for input CM signals around the midsupply can be ensured by using an aspect ratio for MFI transistors that are much smaller as compared to the SE approach.

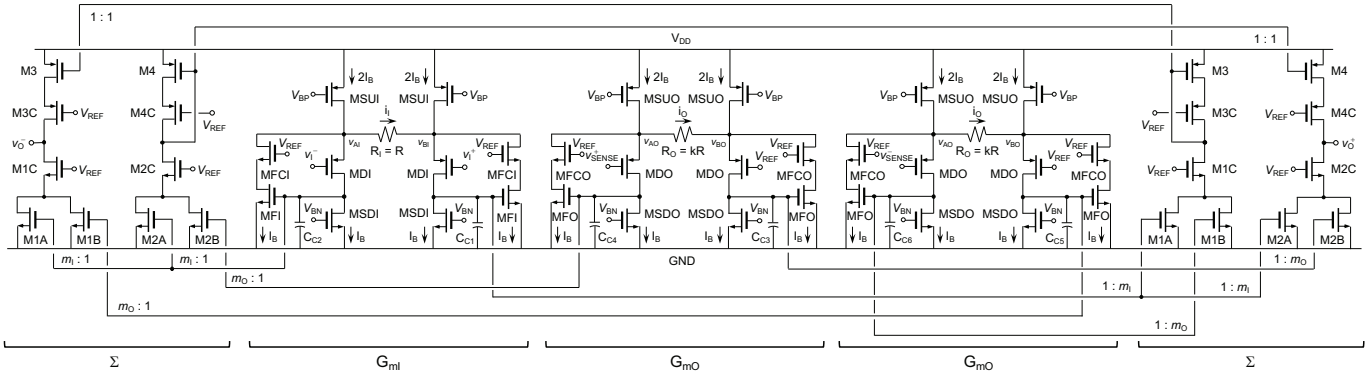


Figure 4. Circuit schematic of the proposed pseudo-differential ICF IA.

3. Design Guidelines

The main features of an ICF IA are analyzed here in order to determine the potential design space as a function of the design options available, in particular, of the parameters set [m_I,m_O,k]. The expressions obtained are validated by means of simulations and a design procedure is proposed.

3.1. Theoretical Analysis

Gain and bandwidth: Taking into account the transfer function of a single-stage ICF IA, given in (5), along with the expression of the effective transconductance in (4), the following expressions for the A_v and the BW are obtained:

$$A_v = \frac{m_I G_{mI}}{m_O G_{mO}} = \frac{k m_I}{m_O} \cdot \frac{\left[1 + \left(1 + \frac{2}{kR}\frac{1}{g_{m,MDO}}\right)\left(\frac{g_{o,MDO}+g_{o,MSDO}}{g_{m,MFO}}\right)\right]}{\left[1 + \left(1 + \frac{2}{R}\frac{1}{g_{m,MDI}}\right)\left(\frac{g_{o,MDI}+g_{o,MSDI}}{g_{m,MFI}}\right)\right]} \approx \frac{k m_I}{m_O} \tag{6}$$

$$BW = \frac{G_{mO}}{C_L} = \frac{m_O}{k} \cdot \frac{2}{C_L R} \cdot \frac{1}{\left[1 + \left(1 + \frac{2}{kR}\frac{1}{g_{m,MDO}}\right)\left(\frac{g_{o,MDO}+g_{o,MSDO}}{g_{m,MFO}}\right)\right]} \approx \frac{m_O}{k} \cdot \frac{2}{C_L R} \tag{7}$$

From these equations, interesting design guidelines may be inferred. First, the voltage gain of the IA in (6) is in the first order of approximation, according to the dominant term, proportional to k and m_I and inversely proportional to m_O. Secondly, the load regulation effect in the input and output V-to-I converters may be cancelled by making $k = 1$, that is, $R_I = R_O$. Otherwise, A_v deviates from the value given by the dominant term and the error increases as k is made larger. Finally, the BW in (7) is proportional to m_O and inversely proportional to k. Thus, a modification of the value of k may be counteracted by a change of m_O in the same sense without affecting the speed and stability conditions of the feedback loop. It is worth pointing out that if the voltage gain of the IA is set by means of parameter k, the saturation of transconductors G_{mI} and G_{mO} rises simultaneously, as v_O is k times larger than v_I, but R_O is also k times bigger than R_I. Nevertheless, if A_v is increased by raising the value of m_I with respect to m_O, whereas k is fixed equal to unity, the amplification of the output signal will force G_{mO} to saturate before G_{mI}.

CMRR: Ideally, only a fully-balanced DM signal can produce an output current in a transconductor. Nevertheless, in the presence of mismatches, CM signals can also lead to an output current in a real V-to-I converter. We can define the residual transconductance as follows:

$$\Delta G_m \equiv \frac{i}{v_{CM}} \tag{8}$$

where v_{CM} is the CM signal applied to the input of the transconductor. The small-signal equivalent model of the V-to-I converters used in the proposed ICF IA has been analyzed to determine the residual transconductance due to the presence of a CM input signal. To this end, for each pair of matched devices in the implementation, the small-signal parameter g_i

has been supposed to be $g_i + \Delta g_i/2$ and $g_i - \Delta g_i/2$, respectively. The main contributions to ΔG_m, after having analyzed and quantified all of them, were found to be due to MD transistors, i.e., $\Delta g_{m,MD}$ and $\Delta g_{o,MD}$, and may be expressed as follows:

$$\Delta G_m|_{\Delta g_{m,MD}} \approx \frac{2}{R} \cdot \frac{\Delta g_{m,MD} g_{o,MD}}{g_{m,MD}^2} \cdot \frac{1}{\left[1 + \frac{2}{R}\frac{1}{g_{m,MD}}\left(\frac{g_{o,MD}+g_{o,MSD}}{g_{m,MF}}\right)\right]} \tag{9a}$$

$$\Delta G_m|_{\Delta g_{o,MD}} \approx \frac{2}{R} \cdot \frac{\Delta g_{o,MD}}{g_{m,MF}} \cdot \frac{1}{\left[1 + \frac{2}{R}\frac{1}{g_{m,MD}}\left(\frac{g_{o,MD}+g_{o,MSD}}{g_{m,MF}}\right)\right]} \tag{9b}$$

The impact of the transconductance and output conductance mismatches of other transistors on ΔG_m is negligible and, hence, is not reported for the sake of conciseness. The contribution of the residual transcoductance can be disregarded in the output transconductor of the ICF IA, as it is much lower as compared to the effective transconductance. Nevertheless, this parameter plays a key role at the input V-to-I converter, since it gives an idea of the rejection to CM signals. In this respect, it is worth pointing out that the feedback loop inherent in an SSF also helps to reduce the load regulation effect of resistor R on the voltage followers, as may be inferred from the rightmost terms in (9a) and (9b).

The CMRR, defined as the ratio of the DM and CM gains of the IA, can be written as

$$CMRR \equiv \frac{A_v}{A_{cm}} = \frac{\frac{m_I G_{mI}}{m_O G_{mO}}}{\frac{m_I \Delta G_{mI}}{m_O G_{mO}}} = \frac{G_{mI}}{\Delta G_{mI}} = \frac{1}{\left(\frac{\Delta g_{m,MDI} g_{o,MDI}}{g_{m,MDI}^2} + \frac{\Delta g_{o,MDI}}{g_{m,MFI}}\right)} \cdot \frac{\left[1 + \frac{2}{R_I}\frac{1}{g_{m,MDI}}\left(\frac{g_{o,MDI}+g_{o,MSDI}}{g_{m,MFI}}\right)\right]}{\left[1 + \left(1 + \frac{2}{R_I}\frac{1}{g_{m,MDI}}\right)\left(\frac{g_{o,MDI}+g_{o,MSDI}}{g_{m,MFI}}\right)\right]} \tag{10}$$

The last fraction in the rightmost term of the previous equation represents the quotient between the load regulation effects of resistor R for the CM and the DM signals, respectively. The use of SSF cells allows it to approach unity if the value of the source degeneration resistor in the input transconductor is not excessively low, i.e., higher than 1 kΩ for practical purposes. Similar theoretical analyses can be carried out for the offset voltage and the power supply rejection ratio (PSRR), which are also influenced by device mismatches. Regarding the offset voltage, the response of the CMRR gives an idea of its behavior, as they are inversely proportional. As for the PSRR, most bioimpedance measurement applications are battery-operated and hence this is not a critical metric in our case.

Noise: Noise is another key metric to be considered in an IA. In those cases where the input signals are restricted to the low frequency range, different techniques for noise reduction, especially of the flicker component, have been considered [11,12,16,19–21,23,25,31,32]. Nevertheless, in bioimpedance spectroscopy, the frequency range that is typically considered is sufficiently wide to assume that thermal noise is dominant. In the ICF IA in Figure 3, the main contributions to the input's referred noiseare due to the devices in the input transconductor. In particular, the IA noise power spectral density can be approached as follows:

$$\frac{v_{iN,th}^2}{\Delta f} = \left[1 + \left(1 + \frac{2}{R_I}\frac{1}{g_{m,MDI}}\right)\left(\frac{g_{o,MDI} + g_{o,MSDI}}{g_{m,MFI}}\right)\right]^2 4kTR_I\left[1 + \frac{4}{3}(g_{m,MDI} + g_{m,MSUI})R_I\right] \tag{11}$$

where k is Boltzmann's constant and T is the absolute temperature. The first term in (11), which is the inverse of the load regulation effect of resistor R_I on the SSF sections, is the conversion factor for referring noise to the input; the second term is the thermal noise of resistor R_I; and the last term accounts for the noise contributions of the devices involved in the circuit implementation of the input V-to-I converter, G_{mI}. It becomes apparent from (11) that the noise of the IA can be reduced by decreasing the value of the source degeneration resistor R_I, which is possible thanks to the use of improved voltage followers, that is, of SSF cells.

Figures of merit: Some of the metrics considered in our analysis are included in a well-known parameter used to compare different IAs, the noise efficiency factor (NEF). This

figure of merit (FoM) describes how many times the noise of a system is higher as compared to the white noise of an MOS transistor with the same drain current and bandwidth [5] and is defined as:

$$NEF = V_{iN,rms}\sqrt{\frac{2I_{DD}}{\pi V_T 4kTBW}} \tag{12}$$

where I_{DD} and V_T are the total DC current flowing through the IA and the thermal voltage, respectively. This is a fair parameter for comparison when the amplitude of the signals to be processed is kept to a low extent. Nevertheless, when large input signals must be processed a high biasing current is required, which leads to a penalty in therms of NEF. Thus, an FoM that takes the signal amplitude into account, such as the dynamic range (DR), can be used in a complementary way. The DR is defined as:

$$DR = 20 \cdot \log\left(\frac{v_{I,DM_{max}}}{V_{iN,rms}}\right) \tag{13}$$

Moreover, in the particular implementations of the IA illustrated in Figures 3 and 4, the maximum input signal is given by

$$v_{I,DM_{max}} = A_{v,SSF} \cdot R \cdot I_B \tag{14}$$

where $A_{v,SSF}$ is the voltage gain of the SSF cells, which for practical purposes can be supposed to be equal to unity. Indeed, the condition for one of the MFI feedback transistors entering the cut-off region is that a maximum current equal to I_B flows through the source degeneration resistor. Different approaches to objectively determining the value of $v_{I,DM_{max}}$ can be established, with a widespread criterion involving the consideration of the amplitude of the input signal that leads to 1% of total harmonic distortion (THD).

3.2. Design Space

Based on the above analysis, it is clear that a same value of the voltage gain, A_v, can be obtained with different combinations of the design parameters m_I, m_O, and k. The most straightforward and common solution is to set the gain of the IA through the ratio k of the output and input degenerations resistors, R_O and R_I, respectively [15,35]. Nevertheless, as is evident from (6), this choice causes the theoretical value of A_v to deviate from the expected nominal value, with this deviation increasing for increasing values of k. Conversely, k can be made equal to unity and the gain of the IA can be set by means of the ratio m_I/m_O. In such a case, special care is required as the BW of the IA relies directly on m_O, and in particular, is directly proportional to the term m_O/k.

In order to determine the design space available for an ICF IA, in terms of A_v, BW, CMRR, and noise, and as a function on the combination of the design parameters [m_I,m_O,k], a case of study has been carried out. First, a nominal voltage gain $A_{v,nom}$ = 4 V/V has been selected, the value of which is in agreement with the relatively low values of the voltage gain required in bioimpedance measurement systems. Then, all the combinations of m_I, m_O, and k leading to the desired value of A_v have been determined, leading to the choices summarized in Table 1. Finally, the metrics A_v, BW, CMRR, and the input referred thermal noise haven been analytically calculated from their corresponding expressions in (6), (7), (10), and (11) when the resistor R is varied in the range [200 Ω−20 kΩ]. The theoretical results have been compared to simulations of the IA in Figure 3, designed using CMOS 180 nm technology to operate with a supply voltage equal to 1.8 V.

In Figure 5a the voltage gain A_v of the IA is represented, including both the results predicted by the analysis and the simulated response. For the case of $k = 1$ both types of results, theoretical and simulated, were extremely close to the nominal value of the voltage gain, i.e., 4 V/V, even for very low values of R. Indeed, the error of the theoretical response was exactly equal to zero, whereas the maximum error of the simulated behavior, not appreciable in Figure 5a, was only 0.1%. ln the other two cases, $k = 2$ and $k = 4$, there

was a noticeable dependence of A_v on R, with the most optimal results occurring around R = 5 kΩ. The higher the value of k, the larger the difference between the load regulation effects due to R_I and R_O and, hence, as predicted by (6), the larger the error in A_v with respect to the expected value $A_{v,nom}$.

Table 1. Combinations of [m_I,m_O,k] leading to A_v = 4 V/V with the same BW.

Option	k	m_I	m_O
#1	4	1	1
#2	2	1	1/2
#3	1	1	1/4

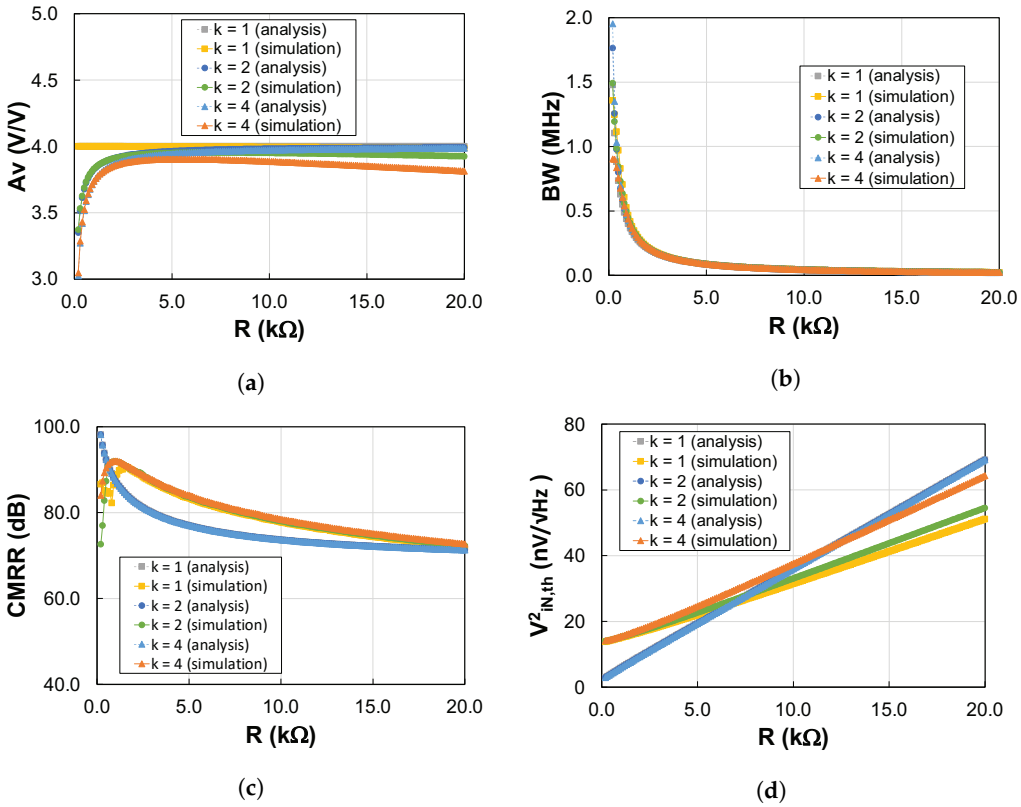


Figure 5. Analytical and simulated response of the ICF IA in terms of (**a**) A_v (**b**) BW, (**c**) CMRR, and (**d**) thermal noise vs. R.

The behavior of the BW of the IA is illustrated in Figure 5b, where again the analytical and simulated responses are represented against the value of resistor R. In both cases the value of the load capacitor, C_L, was set to 180 pF, a relatively high value that allows the splitting of the position of the dominant and the secondary pole of the feedback loop established around the output transconductor of the IA. As observed, the BW increases as the value of the source degeneration resistor R is reduced, which is consistent with (7). Thus, it can be concluded that the simulated value of the BW can be predicted by (7) with fairly high accuracym provided that the feedback loop around G_{mO} displays a response similar to a one-pole system. Otherwise, the impact of secondary poles on the BW should be taken into account in the analytical expression.

The CMRR at DC was also considered in our case study. On the one hand, it was theoretically estimated according to the $G_m/\Delta G_m$ ratio, as indicated in (10), selecting a mismatch for $g_{m,MDI}$ and $g_{o,MDI}$ equal to 0.1%. Moreover, the CMRR, defined as the quotient of the differential-to-differential gain over the common-to-differential gain, was obtained through a 500-run Montecarlo analysis, including mismatches and process varia-

tions. A comparison of the results obtained is illustrated in Figure 5c. It may be observed that the data calculated were the same for k values equal to 1, 2 and 4, as the value of k is not present in (10). Indeed, the CMRR essentially relies on the response of the input transconductor and, hence, the value of k has no impact on its value. It may be observed in Figure 5c that a reasonably good agreement was demonstrated between the theoretical and simulated values of the CMRR, even though the values of the mismatches assumed for the devices involved in (10) were found to be critical.

In view of the frequency range considered in our application, white noise would be dominant over flicker, or $1/f$, noise. For this reason, only thermal noise was taken into account in the theoretical analysis and, consequently, considered in (11). In Figure 5d the theoretical value of the input referred noise power spectral density is represented as a function of R, along with the simulated values of the same metric. In both cases, only the white noise component has been taken into account. As observed, the expression in (11) gives a rough idea of the thermal noise behavior, with noticeable differences arising due to the contributions of other devices that were not included, for the sake of simplicity, in the theoretical calculation of the noise. Therefore, there is an evident trade-off between the complexity of (11) and its accuracy.

Considering the design space created for the proposed ICF IA, illustrative conclusions can be drawn. First, the influence of the parameter k on the voltage gain can be partially counteracted by selecting a value that is not excessively low for R. Moreover, low values of the source degeneration resistor lead to a lower noise figure, thus imposing a design trade-off in the selection of the value of R. Finally, it is worth mentioning that the lower bound for the value of R is determined through the achievement of an appropriate phase margin for the feedback loop established around G_{mO}, which can be adjusted by properly selecting the value of the load capacitor. Indeed, the loading of the IA using only parasitic capacitances may not be sufficient to make the IA stable, and this can be easily overcome by connecting an on-chip load capacitor at the output terminal.

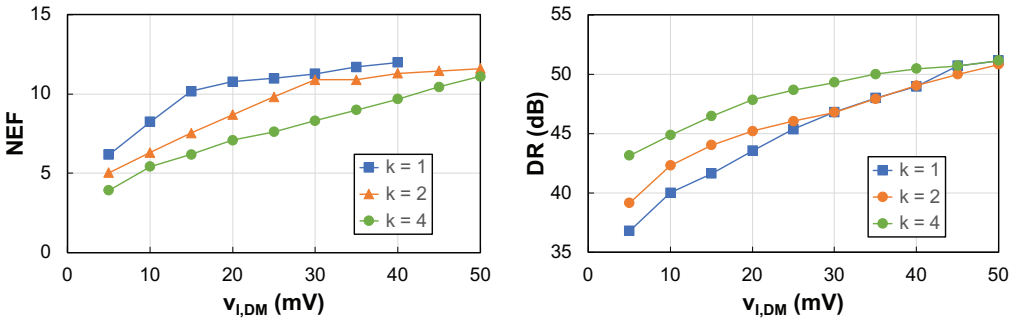
3.3. Design Procedure

To illustrate the analytical and simulated response of the IA described in the previous subsection, a very high value of the load capacitor C_L was assumed, whereas the value of the source degeneration resistor R was swept.Indeed, a high value of C_L allows for the overcompensation of the frequency response of the IA so that the dominant and the secondary poles are sufficiently far away from each other even for very low values of R, that is, for high values of the BW. Nevertheless, this approach is only useful for inspecting the possible design options, as an optimal methodology in the design of the ICF IA. In this respect, the following design procedure is proposed:

- Determine the combinations of the design parameters $[m_I, m_O, k]$ that lead to the desired value of A_v and provide the same BW.
- Select an option for $[m_I, m_O, k]$ and set the value of the source degeneration resistor R in view of the responses of A_v, BW, CMRR and the noise.
- Fix the value of the input DM signal range, $v_{I,DM_{max}}$.
- Find the value of the biasing current I_B that leads to $v_{I,DM_{max}}$ according to (14). This value can be refined by means of simulations establishing an objective criterion, such as obtaining 1% of THD when $v_{I,DM_{max}}$ is applied.
- Determine the value of C_L that leads to a phase margin of 60º for the feedback loop around G_{mO}.
- Calculate the NEF and the DR based on (12) and (13), respectively.

A summary of the simulated behavior of the ICF IA, in terms of the NEF and the DR as a function of $v_{I,DM}$, is depicted in Figure 6, considering the combinations for [m_I,m_O,k] indicated in Table 1. A source degeneration resistor R = 5 kΩ was chosen, representing a good design trade-off between selecting a moderately high value and avoiding an excessive loading effect on the SSF sections. Furthermore, values of I_B and C_L in the ranges [0.7, 7.8] μA and [14.3, 1.3] pF were selected for each value of $v_{I,DM}$ varying between 5 mV

and 50 mV of amplitude. The maximum value of the input DM voltage was limited by the requirement of having a THD below 1%. As a result, the BW and the input referred noise integrated from 1 Hz to the BW frequency were in the ranges of [0.7, 12.3] MHz and [24.6,98.1] μV_{rms}, respectively. The NEF, shown in Figure 6a, is minimized for the case $k = 4$, whereas the DR, represented in Figure 6b, displays the highest values for this same value of k. It may be observed in Figure 6a that for $k = 1$ the NEF is not shown for $v_{I,DM}$ values larger than 40 mV. Indeed, as indicated previously, an excessive level of the input voltage leads to the saturation of the output transconductor, G_{mO}, causing a corresponding drop in the BW and a huge increase in the NEF. In view of the results in Figure 6, it can be concluded that setting the voltage gain of the IA by means of the ratio $k = R_O/R_I$ leads to the lowest NEF and the highest DR, allowing the operating voltage range to be maximized.

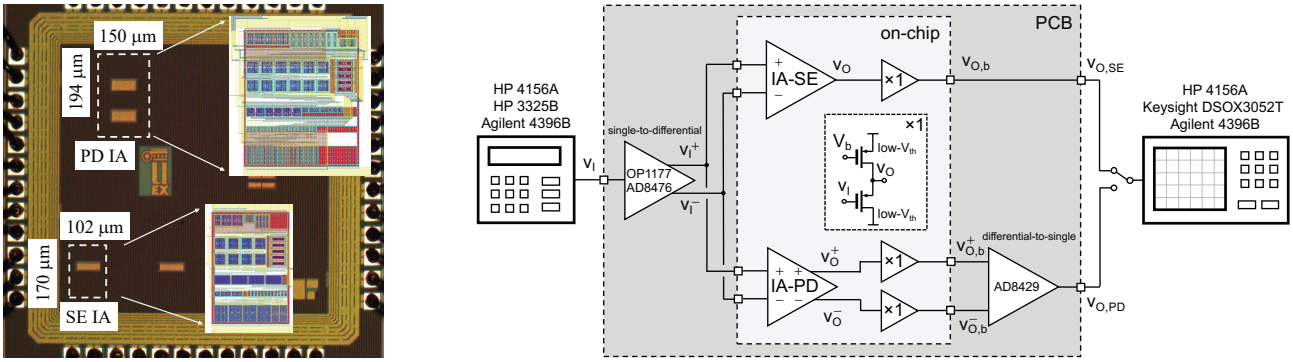


(**a**) (**b**)

Figure 6. Simulated (**a**) NEF and (**b**) DR as a function of the input DM voltage.

4. Experimental Results

The single-ended and pseudo-differential versions of an ICF IA including SSF cells, illustrated in Figures 3 and 4, respectively, were designed using UMC 180 nm CMOS technology to operate with a supply voltage of 1.8 V. Simulations were carried out with the Cadence® Tools Suite, Spectre simulator, and the BSIM3v3 models provided by the foundry, whereas Calibre® Design Suite assisted in the physical verification of the prototype. A microphotograph of the chip is depicted in Figure 7a, in which the layout of each IA is detailed, and the aspect ratios of the main transistors are reported in Table 2. The experimental characterization was carried out over seven samples of the silicon prototypes of every solution, i.e., the SE and the PD structure. The general testbench used for the measurements is illustrated in Figure 7b and included, among others, an HP 4156A precision semiconductor parameter analyzer, an Agilent 4396B spectrum analyzer, an HP 3325B function generator, and a Keysight DSOX3052T oscilloscope. As observed, an on-chip voltage buffer, labelled as $\times 1$, was used to isolate the output terminals of the IAs from low-resistive/high-capacitive loads. Each buffer consists of a PMOS source follower implemented with low-V_{th} transistors, so that operation with the general 1.8 V supply is feasible. The reference voltage, used to set the DC level of the output voltage and to bias the gate terminal of the cascode transistors, was 0.9 V, whereas the biasing current was set to be equal to $I_B = 10$ µA. Moreover, the circuits were optimized to operate at an input CM voltage level of 0.9 V, even though in the case of the SE solution MFI transistors were properly sized so that the IA can work properly with input voltages close to ground. The source degeneration resistors were implemented with non-silicidedhigh-resistance polysilicon, with values equal to $R_I = 5$ kΩ and $R_O = 20$ kΩ, which led to a nominal voltage gain of 4 V/V or 12.04 dB. The load capacitors, C_L, were implemented on-chip as metal-insulator-metal devices, with values of 2.5 pF and 4 pF for the SE and PD approach, respectively, with the goal of setting the phase margin of the feedback loop around G_{mO} as nominally equal to 60°. Furthermore, the overall capacitance connected to the output of the test buffers, due to the PCB used for measurements and to the test probe, was estimated to be around 30 pF.



(**a**) (**b**)

Figure 7. (**a**) Chip microphotograph and (**b**) measurement setup.

Table 2. Transistor aspect ratios (µm/µm) for the SE (Figure 3) and the PD (Figure 4) ICF IA.

Device	SE (µm/µm)	PD (µm/µm)	Device	SE (µm/µm)	PD (µm/µm)
MDI	200/1	200/1	MDO	200/1	200/1
MFI	320/0.5	80/0.5	MFO	80/0.5	80/0.5
MFCI	20/0.5	20/0.5	MFCO	20/0.5	20/0.5
MSDI	16/1	16/1	MSDO	16/1	16/1
MSUI	48/1	48/1	MSUO	48/1	48/1
M1A, M2A	320/0.5	80/0.5	M1B, M2B	80/0.5	80/0.5
M1C	20/0.5	20/0.5	M2C	20/0.5	20/0.5
M3, M4	30/0.5	30/0.5	M3C, M4C	60/0.5	60/0.5

The experimental DC characterization of the samples led to an average total DC supply current for the SE and the PD cases of 139.0 µA and 219.3 µA, respectively, whereas the standard deviation of the output voltage was equal to 5.7 mV and 5.6 mV, respectively. The output voltage of the IA, and hence the offset voltage, could not be measured due to the presence of the on-chip buffers, which introduce a DC voltage level shift with respect to the expected value around V_{REF}. The measured input/output DC transfer characteristics of the two proposed IAs are illustrated in Figure 8. In the case of the PD scheme, the overall output voltage was obtained from the individual outputs as $v_O = v_O^+ - v_O^-$, whereas the offset voltage with respect to the SE structure (of around 6 mV) was corrected to facilitate the graphical comparison. A DC linear input voltage range of around ±55 mV and ±60 mV was determined for the SE and the PD solutions, respectively. Despite the differential structure of the PD approach, both operating linear ranges were very similar, as the maximum signal that can be processed was limited by the saturation of the input transconductor, which was essentially the same in both approximations. Furthermore, the voltage gain and the bandwidth of the IAs are represented in Figure 9 (left axis and right axis, respectively) as a function of the input CM voltage. As observed, an important constraint of operating close to V_{DD} was observed, due to the PMOS implementation of the input and output transconductors. Moreover, the SE solution was able to operate from values of $v_{I,CM}$ very close to ground, whereas some limitations arose in this voltage region for the PD approach. The reason for these responses is that the input CM voltage range was intentionally widened in the case of the SE IA by increasing the size of the MFI transistors, as can be seen in Table 2, so that the measuring configuration illustrated in Figure 1a can be established.

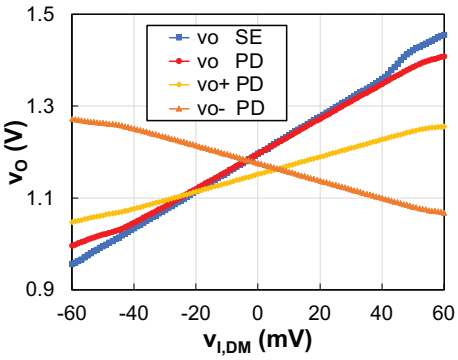


Figure 8. v_O vs. $v_{I,DM}$ DC transfer characteristics.

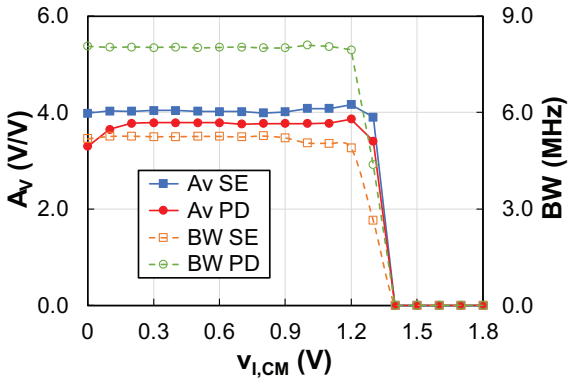


Figure 9. Measured A_v and BW vs. $v_{I,CM}$.

The AC response of the two IAs was also measured, obtaining a voltage gain in the low frequency band equal to 4.28 V/V (12.61 dB) and 3.70 V/V (11.36 dB) for the SE and the PD structure, respectively, whereas the BW was 5.2 MHz and 8.0 MHz, respectively. Regarding the DC gain, this is in agreement with respect to the nominal value, i.e., 4 V/V, with an error of 7% and −7.5% for the SE and the PD cases, respectively. As for the bandwidth, the measured values were lower than the simulated data obtained through a Montecarlo analysis (SE: 6.6 MHz, PD: 8.2 MHz), which led to errors of around −20% and −2.5% for the SE and the PD solutions, respectively. The large deviation in the first case can be ascribed to a higher effective value of the load capacitance due to the direct connection of the test probe to the output buffer, which did not happen in the PD solution, as observed in Figure 7b. Additionally, it was experimentally determined that the effective isolation provided by the voltage buffers was not as high as in the simulated case; thus, the parasitic capacitance is associated with the PCB and the test probe has a non-negligible influence on the experimental BW.In any case, the measured values for the BW of the SE IA were within the range determined by the extreme values found in a corners analysis. On the other hand, the CMRR was measured over the frequency and the results are illustrated in Figure 10. We obtained values at low frequency equal to 72.2 dB and 80.6 dB for the SE and the PD IAs, respectively. Even at the frequency corresponding to the BW, the CMRR was still higher than 33 dB and 41 dB for the SE and the PD solutions, respectively.

The noise was measured and integrated in a frequency band between 100 Hz and the frequency of the BW, resulting in values equal to 85.0 μV_{rms} and 92.0 μV_{rms} for the SE and PD approaches, respectively. These values were overestimated with respect to the actual value of the total measured noise by approximately 4%, due to the finite number of points considered for the integration of the noise. Furthermore, the linearity of the two IAs was characterized in terms of the THD, which is represented in Figure 11 as a function of the input signal amplitude, with frequencies of 1 kHz, 10 kHz, and 100 kHz. The SE IA reached a THD of 1% (−40 dB) for an input amplitude of 39 mV, whereas the same distortion level was obtained in the PD IA for an input amplitude of 53 mV.

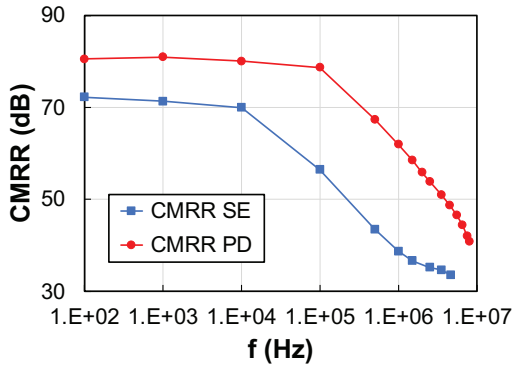


Figure 10. Experimental response of the CMRR as a function of the frequency.

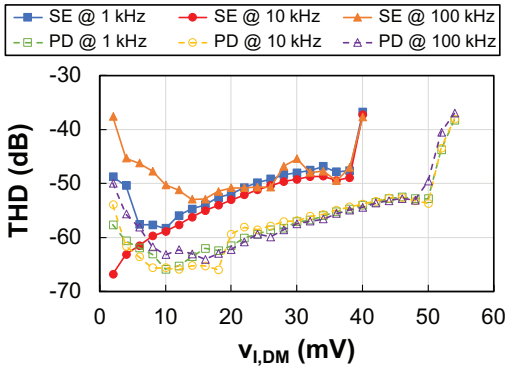


Figure 11. Measured THD as a function of $v_{I,DM}$ for different values of the frequency.

The performance of the two ICF IAs implemented is summarized in Table 3, including both simulated and measured results. It is worth pointing out that the data, expressed as the mean value plus/minus the standard deviation, were obtained through a 500 run Montecarlo analysis with mismatch and process variations in the case of simulations and from the measurements conducted on seven samples in the case of the experimental results. The deviations observed in the measured magnitudes as compared to the corresponding simulated metrics occurred due to process variations and it has been proven that they are within the ranges provided through a corners analysis. The increase in the measured noise with respect to the simulated magnitude was especially noticeable, a part of which can be ascribed to the measurement setup. This led to a corresponding rise in the experimental value of the NEF and a reduction in the measured DR.

Finally, in Table 4, the proposed IAs are compared to those of similar works that have previously been reported. In particular, IAs with a wide bandwidth or aimed at bioimpedance measurements were selected. The NEF is a widely accepted FoM in terms of noise performance, even though it does not take into account the maximum achievable level of the signals to be processed. For this reason, the DR was also considered for comparison. As observed in Table 4, the proposed IAs featured the largest BW among those solutions providing experimental results, were able to process the largest input differential signals for similar supply currents, and were the most compact solutions in terms of silicon area, even in the case of the PD approach, which requires more circuitry due to the differential structure.

Table 3. Simulated vs. experimental performance of the designed ICF IAs (Technology: 180 nm CMOS, V_{DD} = 1.8 V, $A_{v,nom}$ = 4 V/V).

Parameter	SE Simulated	SE Measured	PD Simulated	PD Measured
Voltage gain (V/V)	3.85 ± 0.35	4.28 ± 0.13	3.92 ± 0.05	3.70 ± 0.13
Voltage gain error (%)	−3.7	7.0	−1.9	−7.5
BW (MHz)	6.6	5.2	8.2	8.0
Output offset voltage (mV)	0.35 ± 80.76	±5.69	0.24 ± 80.61	±5.62
$v_I\|_{THD=-40\ \text{dB}}$ @ 1 kHz (mV)	53	39	54	53
$v_I\|_{THD=-40\ \text{dB}}$ @ 10 kHz (mV)	53	39	54	53
$v_I\|_{THD=-40\ \text{dB}}$ @ 100 kHz (mV)	52	39	54	53
SR^+/SR^- (V/µs)	6.0/13.6	6.7/13.4	10.3/10.3	10.9/9.4
CMRR @ DC (dB)	86.6 ± 14.7	72.2	85.5 ± 9.8	80.6
CMRR @ BW (dB)	63.4 ± 10.6	33.5	65.2 ± 6.2	41.2
$V_{iN,rms}$ [100 Hz-BW $^{(*)}$] (μV_{rms})	70.9	85.0	72.7	92.0
I_{DD} (µA)	137.4	139.0	216.1	219.3
NEF	12.5	23.5	14.4	26.3
DR (dB)	54.5	50.2	54.4	52.2

$^{(*)}$ BW_{SE} = 2.7 MHz and BW_{PD} = 4.0 MHz due to the noise measurement setup.

Table 4. Performance comparison of the proposed ICF IAs with other contributions in the literature.

Parameter	[13] JSSC'09	[15] TCAS-I'11	[18] IMCSSD'12	[35] IJEC'20	[40] TCAS-II'21	This Work SE	This Work PD
Technology	0.35-µm CMOS	0.35-µm CMOS	0.35-µm CMOS	0.35-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
Technique	V-to-I I-to-V	LCF	LCF	ICF	G_m-TI	ICF	ICF
Results	Meas.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.
V_{DD} (V)	36	3	2	3	1.8	1.8	1.8
I_{DD} (µA)	3000	285	240	250.6	162	139.0	219.3
Gain (dB)	−18/42	34	8	34	0/40	12.6	11.4
BW (MHz)	2.0	2.0	4.0	7.6	6.7×10^{-6}/87.0	5.2	8.0
CMRR (dB)	120	>90 @ DC	80 @ 1 MHz	99.5 @ DC	164.4 @ 100 kHz	72.2 @ DC	80.6 @ DC
THD (dB) @ v_I (mV_{pp})	N.A.	−56.2 @ 10	N.A.	−57.4 @ 10	N.A.	−52.0 @ 20	−61.6 @ 20
$v_{I,max}$ (mV)	N.A.	30	N.A.	8	N.A.	39	53
$V_{iN,rms}$ (μV_{rms})	283	16	36	32.4	N.A.	85.0	92.0
Area (mm^2)	8.64	0.068	0.037	—	0.0569	0.0173	0.0291
NEF	423.1	5.9	10.8	7.2	N.A.	23.5	26.3
DR (dB)	N.A.	65.5	N.A.	47.9	N.A.	50.2	52.2

5. Conclusions

The ICF technique has been proven to be a suitable technique to implement a wideband IA aimed at bioimpedance measurements. Furthermore, the use of SSF cells in the input and output transconductors required in the ICF approach leads to a general improvement in the overall performance, while also allowing the use of source degeneration resistors with relatively low values. This fact leads to an advantage in terms of silicon area occupation and noise, which in a broad-band application is dominated by the thermal component. The design space was determined by means of a complete analysis, which was confirmed by simulations, accompanied by a design procedure. Two instrumentation amplifiers, with SE and PD structures, were designed and fabricated using 180 nm CMOS technology to operate with a nominal voltage gain of 4 V/V and a supply voltage of 1.8 V. The experimental characterization of the prototypes, carried out using seven silicon samples, led to a wide bandwidth, a high CMRR, and a reduced power consumption, which demonstrates the suitability of the proposed solutions for bioimpedance measurements.

Author Contributions: Conceptualization, I.C., J.M.C., J.L.A. and J.F.D.-C.; methodology, I.C., J.M.C. and J.L.A.; software, I.C. and J.M.C.; formal analysis, J.M.C. and R.P.-A.; investigation, I.C., J.M.C. and J.L.A.; resources, I.C., J.M.C. and M.Á.D.; data curation, I.C., J.M.C., M.Á.D. and R.P.A.-V.; writing—original draft preparation, I.C., J.M.C., J.L.A. and J.F.D.-C.; writing—review and editing, I.C., J.M.C., J.L.A., M.Á.D., R.P.-A. and J.F.D.-C.; visualization, I.C. and J.M.C.; supervision, J.M.C., J.L.A. and J.F.D.-C.; project administration, J.F.D.-C.; funding acquisition, J.L.A. and J.F.D.-C. All authors have read and agreed to the published version of the manuscript.

Funding: Work funded by projects RTI2018-095994-B-I00, from MCIN/ AEI/10.13039/501100011033, and IB18079, from *Junta de Extremadura* R&D Plan, and by Fondo Europeo de Desarrollo Regional (FEDER) Una manera de hacer Europa. Silicon samples granted by EUROPRACTICE MPW and design tool support.

Conflicts of Interest: The authors declare no conflict of interest.

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