RESEARCH ARTICLE

Wide-Bandwidth Electronically Programmable CMOS Instrumentation Amplifier for Bioimpedance Spectroscopy

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ABSTRACT An instrumentation amplifier (IA) with continuous tuning of the voltage gain, suitable for operation over a wide frequency range, and aimed to electrical bioimpedance spectroscopy, is proposed. The operation principle of the IA is based on indirect current feedback (ICF), which leads to an almost-constant bandwidth regardless of the value of the programmed voltage gain. The use of improved voltage followers in the transconductors required in the ICF technique allows achieving a compact implementation with a bandwidth compatible with bioimpedance spectroscopy applications. The tuning strategy relies on a continuously programmable current mirror that can be electronically adjusted by means of a control current. The IA has been designed and fabricated in 180 nm CMOS technology to operate with a 1.8-V single supply. The experimental characterization of the silicon prototypes showed a gain programmability range higher than 45 dB, between -4.6 dB and 41.2 dB, a BW around 3 MHz, and a maximum CMRR at DC higher than 86 dB, all this with a minimum current consumption of 144.8 μA and an area occupation of 0.0196 mm^2.

I. INTRODUCTION

The electrical properties of a biological media can be characterized by determining its impedance, which is known as bioimpedance measurement technique [1]. The biological impedance (Z_{BIO}) is excited by an electrical sinusoidal signal, either a current or a voltage, the corresponding magnitude (a voltage or a current, respectively) is measured, and the internal composition of the Z_{BIO} is derived from the gain and phase angle of the response. In many applications, an excitation current, i_{exc}, is preferred, in order to avoid damaging the biological media, and a voltage is measured in response with the assistance of an instrumentation amplifier (IA) [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], as illustrated in Fig. 1. Indeed,

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i_{exc} can be kept in the range of the μA, and generally lower than a few mA, thus resulting innocuous for the sample under test. Nevertheless, if the value of the bioimpedance to be measured, which in principle can be completely unknown, is in the range of a few Ohm, the maximum excitation current dictated by medial safety regulations could result insufficient to generate a measurable voltage drop at Z_{BIO}. This constraint can be overcome by using an IA with electronically programmable voltage gain, which avoids any hardware reconfiguration of the system providing the application with flexibility of use. On the other hand, a complete electrical characterization of the Z_{BIO} requires measurements in a wide frequency range, from some hundred of Hz to a few MHz, which imposes additional requirements to the bandwidth (BW) of the IA.

The indirect current feedback (ICF) technique, represented by the block diagram within the dotted box in Fig. 1, is a suitable approach to implement a monolithic IA able to operate
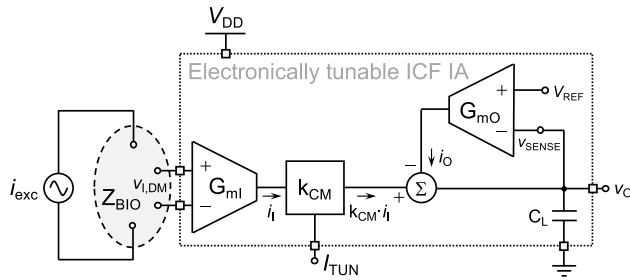
FIGURE 1. Conceptual block diagram of the proposed bioimpedance measurement system.

in a low-voltage supply environment [6], [27], [29], [31]. A single-stage ICF IA is basically made up of an input and an output (or feedback) transconductor, G_{mI} and G_{mO} in Fig. 1, respectively, and a summing stage. The gain of the IA relies on the ratio G_{mI}/G_{mO}. Besides, if G_{mO} is kept unchanged and the voltage gain of the IA, A_v, is adjusted by modifying G_{mI}, through the block k_{CM} in Fig. 1, the BW of the system remains approximately constant regardless of the value of the voltage gain.

The most popular strategy to program the gain of an IA is based on connecting an external resistor between two input ports of the circuit [3], [10]. Thus, to set the gain to a different value, the external component must be replaced. A straightforward solution to obtain a programmable IA is to incorporate a digitally configurable bank of components, thus achieving a discrete adjustment [4], [11], [17], [20]. Besides, different circuit techniques have been proposed to continuously tune the response of an analog section, some of which have been applied to program the voltage gain of an instrumentation amplifier [15], [19], [21], [22], [23], [24], [25], [28]. Among them, the most common approaches are based on the use of current mirrors [15], translinear loops [28], resistors implemented by means of active devices [21], [23], [25] or by modifying the biasing current [22], [24] or the transconductance [19] of some of the constituent blocks.

In this paper an electronically programmable ICF IA, designed and fabricated in 180 nm CMOS technology to operate with a 1.8-V supply, is presented. The single-stage structure of the IA, along with the use of improved voltage followers, leads to a compact, low power, and wide bandwidth implementation. The principle of operation of the tuning scheme is based on a continuously tunable current mirror, which offers multiple design options leading to a flexible design space. The rest of the manuscript has been organized as follows: the principle of operation of the ICF IA is described in Section II, the transistor level implementation of the circuit is detailed in Section III, experimental results are presented and discussed in Section IV and, finally, conclusions are drawn in Section V.

II. PRINCIPLE OF OPERATION

The proposed electronically programmable IA is based on a current feedback. Nevertheless, unlike direct current feedback [3], [4] and local current feedback [7], [14], in the

indirect current feedback technique [6], [29] the stacking of blocks is avoided and the feedback loop involves only the output transconductor, thus resulting more suitable for low-voltage wide-bandwidth applications.

A. CONCEPTUAL BLOCK DIAGRAM OF THE IA

The block diagram of the proposed IA is illustrated in the dotted box of Fig. 1. As observed, it consists of two transconductors, G_{mI} and G_{mO}, a current-mode gain block, k_{CM}, and a summing stage, Σ. The voltage-to-current (V-to-I) converter G_{mI} generates an output current, i_I, from the input differential-mode (DM) voltage, $v_{I,DM}$, whereas G_{mO} converts the voltage difference $V_{REF} - v_O$ into the current i_O. The signal V_{REF} is a reference voltage used set the DC level of the output signal. The current produced by the input transconductor is multiplied by the gain of a current mirror, k_{CM}, and the resulting signal, $k_{CM} \cdot i_I$, is compared in the summing stage with the current generated by the output V-to-I converter. The action of the feedback loop established around G_{mO} is twofold. On the one hand, the resulting current at the output of the summing stage is forced to be ideally zero, thus making currents $k_{CM} \cdot i_I$ and i_O equal. On the other hand, the virtual ground principle at the input of G_{mO} induces a DC voltage level equal to V_{REF} at the output of the IA.

The transfer function of the block diagram depicted in Fig. 1 can be expressed as:

$$H(s) \equiv \frac{v_o(s)}{v_{i,dm}(s)} = \frac{G_{mI} \cdot k_{CM} \cdot \left(R_{out} \parallel \frac{1}{sC_L}\right)}{1 + \beta \cdot G_{mO} \left(R_{out} \parallel \frac{1}{sC_L}\right)} \quad (1)$$

where R_{out} and C_L are the output resistance and the load capacitance, respectively. Assuming a sufficiently high gain in the loop around G_{mO}, the voltage gain, A_v, and the BW of the IA can easily be deduced from (1) to be:

$$A_v \equiv \frac{v_o}{v_{i,dm}} = k_{CM} \cdot \frac{G_{mI}}{G_{mO}} \quad (2)$$

$$BW = \frac{G_{mO}}{C_L} \quad (3)$$

The gain of the IA can be nominally adjusted by means of the ratio G_{mI}/G_{mO} and subsequently programmed by means of the current gain k_{CM}. Besides, the selection of an appropriate value of C_L is used to set the BW, also obtaining a suitable phase margin for the feedback loop. It is worth to note that the BW of the IA does not rely on the gain k_{CM}, which ensures a roughly constant frequency response over the entire gain programmability range.

B. CONTINUOUSLY TUNABLE CURRENT MIRROR

The electronic programmability of the voltage gain of the proposed IA is based on the continuously tunable current mirror illustrated in Fig. 2. In a conventional current mirror the same gate-to-source voltage is applied to the input and the output transistor, obtaining a fixed current gain that relies on the ratio of the geometries of both devices provided that they are biased in saturation. The principle of operation of
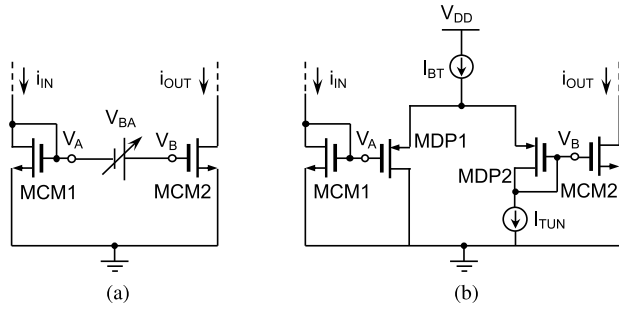
FIGURE 2. Continuously adjustable tuning section: (a) conceptual circuit schematic and (b) implementation of the floating voltage source.

the current mirror in Fig. 2a is based on including a floating voltage source between the gates of the input transistor, MCM1, and the output transistor, MCM2, so that the voltage level at each gate, V_A and V_B, respectively, can be varied and, hence, the current gain can be modified. The floating voltage source, with value $V_{BA} = V_B - V_A$, has been implemented in our proposal by means of a PMOS differential stage, MDP1 and MDP2, as depicted in Fig. 2b. The tail current of the differential section, I_{BT}, is shared between the two branches of the pair to cause a variable offset voltage. Indeed, the floating voltage V_{BA} depends on how this biasing current I_{BT} is distributed between the two branches of the differential pair. The diode connection in device MDP2 allows sourcing the required current by the current source I_{TUN} and driving the output transistor of the current mirror, MCM2. When the current I_{TUN} is made equal to $I_{BT}/2$ the same current flows through transistors MDP1 and MDP2, thus $V_A = V_B$ and the current gain of the current mirror is equal to one, provided that $(W/L)_{MCM1}=(W/L)_{MCM2}$. When $I_{TUN} < I_{BT}/2$ we have that $V_B > V_A$, thus leading to a current amplification. Conversely, if $I_{TUN} > I_{BT}/2$ it happens that $V_B < V_A$ and the output current is lower than the input current, which is equivalent to a current attenuation.

Three design aspects allow modifying the tunability range of the current mirror presented in Fig. 2. On the one hand, the input DM voltage range of the differential pair can be made wider, which allows obtaining a larger value for V_{BA} and, hence, a broader range for the current gain. This can be done by either increasing the value of the tail current of the differential pair, I_{BT}, or decreasing the aspect ratio of the driver transistors, $(W/L)_{MDP1-2}$. On the other hand, for a given voltage shift provided by the differential pair in the tuning section, V_{BA}, the current gain is made larger as the aspect ratio of transistors MCM1 and MCM2 is increased. These factors can be summarized in the following general analytical expression:

$$\frac{i_{OUT}}{i_{IN}} = \frac{(W/L)_{MCM2}}{(W/L)_{MCM1}} \cdot f(V_B, V_A) \qquad (4)$$

from which it becomes clear that the ratio of the sizes of the input and output devices stands for a nominal setting of the current mirror gain and the generic function of voltages V_B
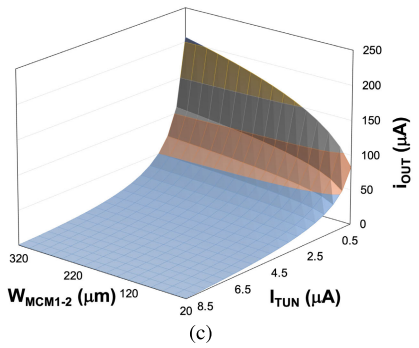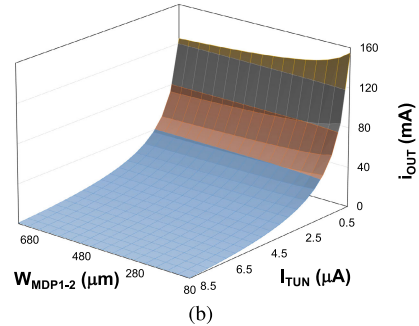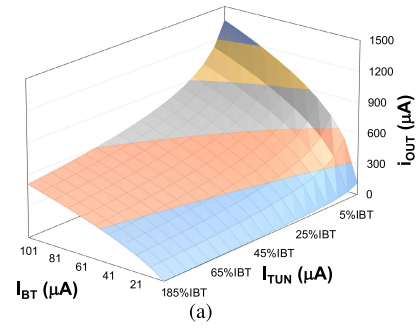
FIGURE 3. Design spaces of i_{out} vs (a) I_{BT} / I_{TUN}, (b) $(W/L)_{MDP1-2}$ / I_{TUN}, and (c) $(W/L)_{MCM1-2}$ / I_{TUN}.

and V_A enables the electronic programmability of the circuit section.

A particular expression can be easily derived for the current gain of the current mirror in (4). Nevertheless, to do so an inversion region, i.e., weak, moderate, or strong, has to be assumed. As the principle of operation of the proposed tunable current mirror is suitable for any inversion level, a design space has been built by means of simulations instead. The current gain of the programmable current mirror has been evaluated by modifying the biasing current of the differential pair, I_{BT}, the aspect ratio of the differential pair driver transistors, $(W/L)_{MDP1-2}$, and the aspect ratio of the devices in the current mirror, $(W/L)_{MCM1-2}$. The current I_{TUN}, which is considered the control variable to obtain electronic programmability, has also been swept in the three cases indicated. The corresponding design spaces are depicted in Figs. 3a, 3b, and 3c, where the input current was fixed to the value $i_{IN} = 10$ μA. In Fig. 3a the biasing current of the differential pair I_{BT} was swept in the range [1:101] μA, while the control current I_{TUN} was moved between 5% and 95% the value of I_{BT}. As observed, the output current of
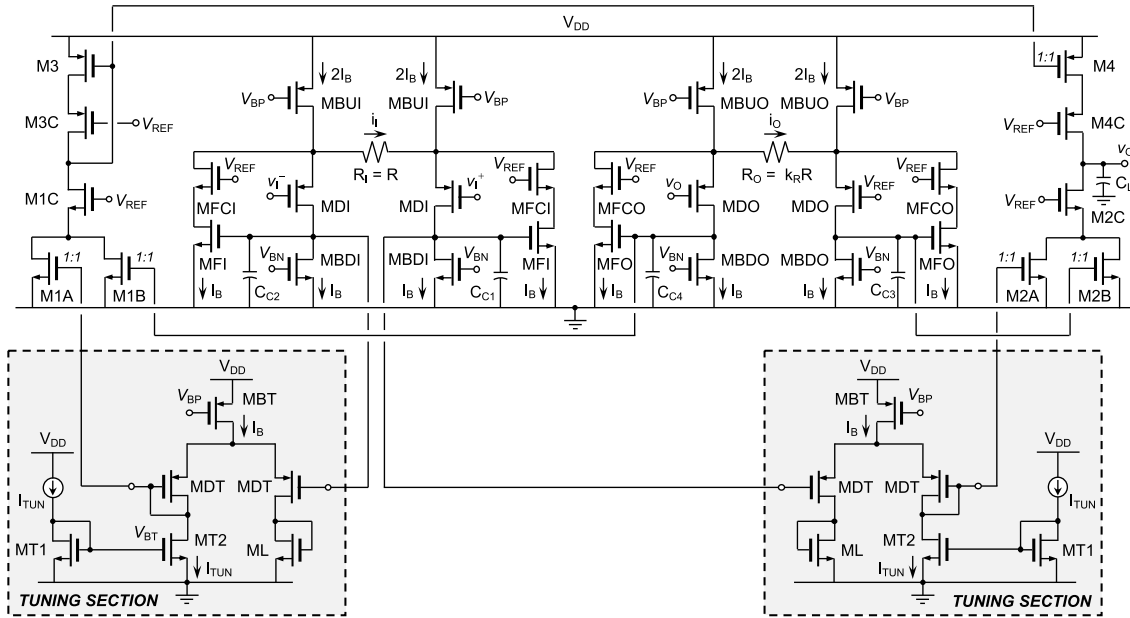
FIGURE 4. Transistor level implementation of the proposed electronically programmable ICF IA.

the current mirror can be increased at the cost of raising the power consumption of the circuit, since the current gain increases for larger values of I_{BT}. For the case illustrated in Fig. 3b the current I_{BT} was fixed to 10 μA, the aspect ratio of transistors MDP1 and MDP2, $(W/L)_{MDP1-2}$, was changed in the range [80/0.5:720/0.5] μm/μm and I_{TUN} was swept between 0.5 μA and 9.5 μA, i.e., from 5% to 95% the value of I_{BT}. It may be inferred from Fig. 3b that there is little influence of $(W/L)_{MDP1-2}$ on the output current of the current mirror, as for the considered aspect ratios it only moves in the range between 125 μA and 155 μA. Finally, Fig. 3c was obtained by fixing I_{BT} to 10 μA, sweeping $(W/L)_{MCM1-2}$ in the range [20/0.5:320/0.5] μm/μm and changing I_{TUN} between 0.5 μA and 9.5 μA. In this case it becomes clear that an increase in the aspect ratio of the transistors of the current mirror leads to ta noticeable increase of the output current and, hence, of the current gain.

In view of the data in Figs. 3a, 3b, and 3c, it may be concluded that a good design trade-off consists on fixing the biasing current of the differential pair to a value that does not increase excessively the power consumption of the circuit, minimizing the size of the transistors in the differential pair, as their impact on the current gain is not very high, and maximizing the aspect ratio of the transistors in the current mirrors in order to increase the programmability range. In addition to these design considerations, it is worth noting that the current I_{TUN} is a suitable control variable, which allows the electronic programmability of the tuning section and facilitates its inclusion in an automatic control loop.

III. PROPOSED PROGRAMMABLE ICF IA

The transistor level implementation of the proposed IA is illustrated in Fig. 4. The input and the output transductor, G_{mI} and G_{mO}, respectively, consist each of a resistor,

R_I and R_O, also respectively, where the *V*-to-*I* conversion takes place, and two voltage buffers, to isolate the resistor from the preceding stages. In particular, super source followers (SSFs), made up of a driver transistor, MDI(O), and a feedback device, MFI(O), are used in order to achieve a voltage gain very close to unity and to allow using small resistor values. Transistors MBUI(O) and MBDI(O) are current sources providing biasing currents equal to $2I_B$ and I_B, respectively, and devices MFCI(O) are used to ideally cancel systematic offset, as detailed below. Under these assumptions, the voltage gain of the super source followers has been found to be:

$$A_{v,SSF} = \cfrac{1}{1 + \left(1 + \frac{2}{R}\frac{1}{g_{m,MD}}\right)\left(\frac{g_{o,MD}+g_{o,MBD}}{g_{m,MF}}\right)} \quad (5)$$

where R, MD, MBD, and MF are the linearization resistor and the driver, current source, and feedback transistor, respectively, at the input and output transconductors. As observed in the most right term in the denominator of (5), the load regulation effect is highly reduced by the gain of the feedback loop implicit in the SSF, i.e., by the term $g_{m,MF}/(g_{o,MD} + g_{o,MBD})$, thus leading to a voltage gain very close to unity. As a consequence, the effective transconductance of the input and the output *V*-to-*I* converter can be expressed as:

$$G_{m,eff} \equiv \frac{i}{v_{DM}} \approx \frac{2}{R} \quad (6)$$

where R represents resistors R_I and R_O in G_{mI} and G_{mO}, respectively. As observed in Fig. 4, the current signal produced in the output transconductor, i_O, is conveyed to the summing stage by means of current mirrors with a fixed current gain *1:1*. Alternatively, the two tuning sections enclosed in dashed boxes in Fig. 4 have been incorporated in order to amplify the current signal generated by G_{mI}, i.e., i_I, which

appears at the summing stage as $k_{CM} \cdot i_I$. Considering the expression in (6) and taking into account that the linearization resistors at the input and the output V-to-I converter are named in Fig. 4 as R and $k_R R$, respectively, the voltage gain and BW of the proposed IA can be written as:

$$A_v = k_{CM} k_R \qquad (7)$$

$$BW = \frac{2}{k_R R C_L} \qquad (8)$$

The gain of the IA can be adjusted by means of the ratio $G_{mI}/G_{mO} = k_R$ and subsequently programmed by the current gain k_{CM}. As detailed in Section II-B, the value of k_{CM} can be lower or higher than unity, depending on the relative value of the control current I_{TUN} with respect to the bias current I_{BT}. Nevertheless, amplification is required in most cases in an IA. Thus, the maximum attenuation provided by the minimum achievable value of k_{CM} can be counteracted by means of the amplification factor k_R, thus expanding the entire programmability range provided by the tunable current mirror towards values of the voltage gain of the IA higher than 1 V/V. Besides, it is worth to note that the BW of the IA is set by adjusting the value of the on-chip physical capacitor C_L, which is only slightly influenced by the parasitic effects associated to the output node.

The ability of the IA to reject input common-mode (CM) signals is usually evaluated by means of the CM rejection ratio (CMRR), defined as the quotient of the gains when a DM and a CM signal are applied to the input of the IA. Mismatches between ideally equal devices give rise to a differential current even in the presence of an input CM signal, which is equivalent to have an undesired transconductance that can be expressed as:

$$\Delta G_{m,eff} \equiv \frac{i}{v_{CM}} \qquad (9)$$

Thus, matching must be enhanced in order to improve the CMRR. An outstanding feature of a current feedback IA is that the CMRR relies fundamentally on the input transconductor [31]. Indeed, all the devices in the input V-to-I converter, G_{mI}, take part in the generation of the residual transconductance in (9). It has been verified by simulations that the main contribution to $\Delta G_{m,eff}$ is associated to the input transistors, MDI in Fig. 4. A hand analysis of the small-signal equivalent circuit, assuming mismatches in the transconductance, $\Delta g_{m,MDI}$, and output conductance, $\Delta g_{o,MDI}$, of transistors MDI led to the following equations:

$$\Delta G_{m,eff}|_{\Delta g_{m,MDI}} \approx \frac{2}{R} \cdot \frac{\Delta g_{m,MDI} \, g_{o,MDI}}{g_{m,MDI}^2} \cdot LR \qquad (10a)$$

$$\Delta G_{m,eff}|_{\Delta g_{o,MDI}} \approx \frac{2}{R} \cdot \frac{\Delta g_{o,MDI}}{g_{m,MFI}} \cdot LR \qquad (10b)$$

where the term LR is equal to

$$LR = \frac{1}{\left[1 + \frac{2}{R} \frac{1}{g_{m,MDI}} \left(\frac{g_{o,MDI} + g_{o,MBDI}}{g_{m,MFI}} \right) \right]} \qquad (11)$$
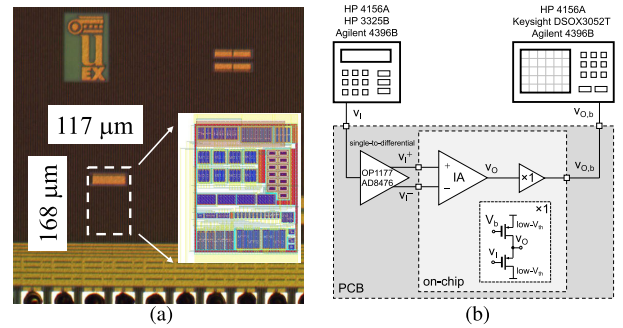

FIGURE 5. (a) Chip microphotograph (b) and experimental setup.

TABLE 1. Transistor aspect ratios (μm/μm) of the proposed IA in Fig. 4.

| Device	(W/L)	Device	(W/L)
MDI, MDO	200/1	MFI, MFO	80/0.5
MFCI, MFCO	20/0.5	MBDI, MBDO	16/1
MBUI, MBUO	48/1	M1A-B, M2A-B	80/0.5
M1C, M2C	20/0.5	M3, M4, MDT	240/0.5
M3C, M4C	60/0.5	MBT	24/1
MT1, MT2	16/1	ML	40/1

and stands for the load regulation effect of resistor R on the input voltage followers. Similar equations can be obtained for the other devices in G_{mI}. It can be inferred from (10) that to obtain a high CMRR in the proposed IA a good matching between the devices in the input V-to-I converter must be achieved, whereas it can be further improved by increasing the transconductance of transistors MDI and MFI.

It is worth to mention that the systematic offset of the single-ended structure proposed has been reduced by including cascode transistors in each SSF cell, devices MFCI and MFCO, and by properly sizing the PMOS current mirror, transistors M3-M4, used to carry out the differential-to-single conversion. Besides, capacitors C_{C1} to C_{C4} have been included to stabilize the frequency response of the four SSF cells used in the input and the output V-to-I converter.

IV. EXPERIMENTAL RESULTS

The proposed IA has been designed and fabricated in 180 nm CMOS technology to operate with a single supply voltage of 1.8 V. A microphotograph of the circuit, which occupies a silicon area of 0.0196 mm^2, is shown in Fig. 5a, where the layout is also detailed. Besides, the transistor aspect ratios of the IA are given in Table 1. The experimental characterization of the electronically programmable IA has been carried out over 7 different samples of the silicon prototype and the general testbench used in the different measurements is represented in Fig. 5b. The on-chip voltage buffer prevents an excessive loading of the output node of the IA and helps to keep a nearly constant BW regardless the value of the off-chip load capacitance.

The biasing current, I_B, was adjusted to be 10 μA, which led to a tail current of 20 μA for the SSF blocks and 10 μA for the tuning sections. The reference voltage, V_{REF}, used to establish the DC output level and to bias the gate terminal of the cascode transistors, was set equal to 0.9 V, i.e., to midsupply. The minimum gain of the tunable current mirrors
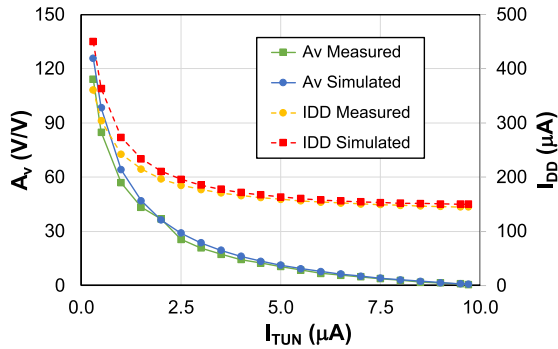
FIGURE 6. Voltage gain (left axis) and supply current (right axis) of the proposed IA as a function of I_{TUN}.

FIGURE 7. Measured and simulated BW *vs* I_{TUN}.

FIGURE 8. Measured and simulated CMRR *vs* I_{TUN}.

was determined by simulations to be approximately equal to 0.042 A/A. Consequently, the resistors at G_{mI} and G_{mO}, implemented with non-salicided high-resistance polysilicon, where sized with values $R_I = 2\,\text{k}\Omega$ and $R_O = 24\,\text{k}\Omega$ in order to counteract such an attenuation of approximately $12\times$. An on-chip metal-insulator-metal capacitor $C_L = 2.5$ pF was connected at the output terminal of the IA, just before the test buffer, in order to set the BW. The design criterion followed to size the integrated capacitor was to obtain a phase margin slightly higher than 60° in the feedback loop established around G_{mO}. It is worth to point out that the effective value of C_L is increased by the input capacitance of the test buffer, which slightly varies with the value of the external load capacitance, due to the PCB connections and to the test probe. In any case, the stability of the IA in such a configuration has been demonstrated by corner and Montecarlo simulations. Capacitors C_{C1} to C_{C4} were implemented by MOS-cap devices to minimize silicon area, having a nominal value of 1.45 pF.

AC measurements were carried out in the frequency range from 10 Hz to 10 MHz, so that both the voltage gain at low frequency and the bandwidth of the IA could be determined. The voltage gain of the IA was measured as a function of the tuning current and is represented in Fig. 6. The values of A_v varied between 0.59 V/V (-4.6 dB) and 114.29 V/V (41.2 dB) when I_{TUN} was swept between 0.3 μA and 9.7 μA, that is, 3% and 97% the value of tail current I_{BT}. The measured plot is in close agreement with the simulated results, which are also represented in Fig. 6. The price to be paid by the proposed programmability mechanism is the variation of the supply current, I_{DD}, which is also a function of I_{TUN}, as illustrated in Fig. 6. The current consumption of the SSF cells and the tuning sections is fixed and equal to $2I_B$ and I_{BT}, respectively. Nevertheless, signal amplification, which takes place for low values of the tuning current, requires an increase of the current mirrored to the outer branches of the IA, thus increasing the current consumption. A corresponding reduction of the supply current does not take place for high values of I_{TUN}, due to the minimum bound imposed by the fixed current consumption of certain circuit sections indicated before. A good agreement between simulations and measurements is also achieved for the case of I_{DD}, as observed in Fig. 6.
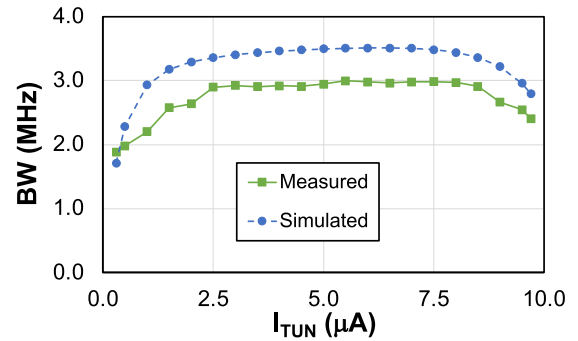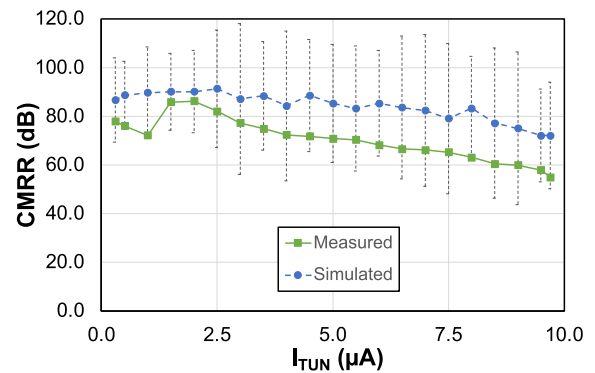
The AC characterization of the IA allowed also determining the BW, which is depicted in Fig. 7 as a function of I_{TUN}. It remains roughly constant over the entire programmability range with an approximate measured value of around 3 MHz. When the level of the tuning variable I_{TUN} is adjusted to values close to the extremes, i.e., zero and I_{BT}, the DC current through one of the two branches of the tuning section decreases. As a result, the position of the corresponding non-dominant pole is reduced, thus resulting in a drop of the BW of the IA. The difference between experimental and simulated values of the BW, also illustrated in Fig. 7, is ascribed to the impact of the test buffer on the capacitance at the output node of the IA, which is higher than expected from simulations.

Frequency measurements gave rise too to the experimental values of the CMRR, which is represented in Fig. 8 as a function of I_{TUN} in the range [0.3:9.7] μA and compared to the simulated response. The simulated CMRR was obtained from a set of 1000-run process and mismatch Montecarlo analyses, in which all the parameters of the devices were randomly varied with a value of sigma equal to 3. The error bars (standard deviation) associated to the each simulated value of the CMRR (mean value) comprise the measured data in all the cases. The minimum values of the experimental CMRR, around 55 dB, take place for the lowest values of the DM voltage gain, that is, for high values of I_{TUN}, whereas the maximum measured value of the CMRR is higher than 86 dB. The CMRR was also measured at the frequency of the

TABLE 2. Performance comparison of the proposed electronically programmable IA with similar contributions in the literature.

Parameter	[17] BioCAS'15	[19] ICTPS'16	[20] TCAS-I'17	[21] IJEC'17	[22] IJEC'18	[24] IJEC'18	[25] IJEC'18	[28] IJEC'20	This work
Technology	180 nm CMOS	180 nm CMOS	130 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	$0.35\mu m$ CMOS	180 nm CMOS
Programming	Discrete	Continuous	Discrete	Continuous	Continuous	Continuous	Continuous	Continuous	Continuous
Technique	Bank of resistors	G_m tuning	Bank of capacitors	Pseudo resistor	I_B tuning	I_B tuning	Pseudo resistor	Translinear loop	Current mirror
Results	Simulated	Simulated	Measured	Simulated	Simulated	Simulated	Simulated	Simulated	Measured
V_{DD} (V)	3.3	3.3	1.255	± 0.9	± 1.25	± 0.9	± 0.9	± 0.75	1.8
I_{DD} (μA)	211.5 / 1809	261	33.14	422.2	200.8	638.9 / 722.2	470	0.048 / 0.257	144.8 / 361.2
Gain (dB)	0.5 / 39.0	Max. 47	66 / 93	6.9 / 25.0	6.1 / 20.5	31.0 / 33.6	4.7 / 18.0	20.0 / 40.0	-4.6 / 41.2
BW (MHz)	6.0	$\sim 10^{-4}$	48×10^{-6}	1.8 / 19.3	52.7 / 233.0	73.0 / 100.0	3.0 / 14.8	$\sim 7\cdot 10^{-3}$	3.0
CMRR (dB)	>70 @ 100 kHz	117	77.6 @ 10 Hz	36.0 / 54.2	53.0	52.8 / 64.7	51.2	44.4 / 48.9	54.9 / 86.2 @ DC 27.6 / 58.9 @ BW
THD (dB)	N.A.	<-125	-47.9	-35.4 @ 4 μA_{pp} 5 kHz	-37.3	-41.0 @ 8 μA_{pp}	-45.7 @ 4 μA_{pp} 5 kHz	-34.0 @ 550 pA	-48.6 @ 40 mV_{pp} 1 kHz
Noise	N.A.	<1.2 μV/$\sqrt{\text{Hz}}$	3.75 μV_{rms}	12 / 18 pA/$\sqrt{\text{Hz}}$	7.5 pA/$\sqrt{\text{Hz}}$	5.8 pA/$\sqrt{\text{Hz}}$	N.A.	11.2 pA$_{rms}$	48.2 μV_{rms}
Area (mm^2)	N.A.	N.A.	0.183	N.A.	N.A.	N.A.	N.A.	N.A.	0.0196
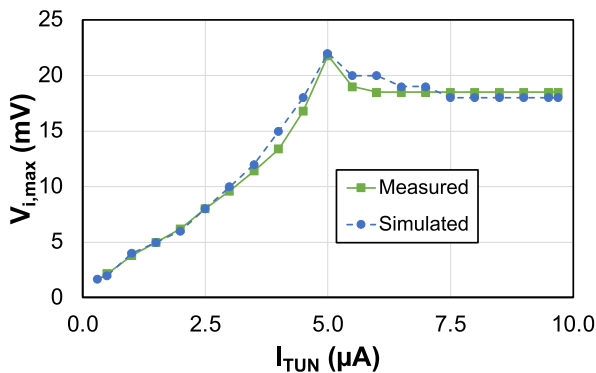
FIGURE 9. Maximum input voltage for a -40 dB THD as a function of I_{TUN}.

FIGURE 10. Input-referred spectral density of noise *vs* I_{TUN} at 1 MHz.

bandwidth, obtaining values around 25 dB lower in average with respect to the values obtained at low frequency.

The linearity of the IA was determined by measuring the total harmonic distortion (THD). In particular, the maximum input signal leading to a -40 dB THD is represented in Fig. 9 over the tuning variable, I_{TUN}. As observed, the peak of $v_{I,max}$ takes place in the central range of I_{TUN}, due to the operation of the differential pairs of the tuning sections in their linear region. When I_{TUN} is increased, the value of $v_{I,max}$ remains constant regardless of the voltage gain, as the main source of nonlinearity for low values of the voltage gain is due to the input stage. Conversely, for low values of the tuning current the voltage gain is highly increased and, hence, the saturation of the output transconductor and of the output branch limit the maximum input signal that can be applied, which is also very small due to the high values of the voltage gain.

The noise of the proposed IA was measured and simulated with the goal of determining the spectral density of noise as well as the integrated noise over a given frequency band. The input-referred spectral density of noise is illustrated in Fig. 10

as a function of I_{TUN} at a frequency of 1 MHz. As observed in the plots, experimental and simulated data show a similar trend, even though the minimum measurable noise is limited by the test setup. For high levels of I_{TUN}, that is, for low values of the voltage gain, the noise of the input and the output V-to-I converter have a similar contribution to the total noise. As the gain of the instrumentation amplifier is increased the input-referred noise of the output transconductor becomes negligible, thus leading to a lower overall input-referred noise. Besides, the noise was measured for $I_{TUN} = 5$ μA and integrated in the frequency band between 100 Hz and the BW and the corresponding value is reported in Table 2.

The experimental performance of the proposed electronically programmable IA is summarized in Table 2, where it is also compared to other similar solutions previously reported. As observed in Table 2, the proposed solution leads to the widest programmability range of the IA gain, featuring a BW suitable for bioimpedance spectroscopy applications and presenting a current consumption similar to that of the other proposals. In general, current mode techniques [21], [22],

[24], [25], [28] provide a wider operating frequency range, even though the CMRR in these cases is, also in general, much lower as compared to that of the voltage-mode approaches proposed in [17], [19], and [20], and in the present work. The noise of the proposed IA was measured in a frequency range between 100 Hz and 2.1 MHz, due to BW reduction suffered by the IA in this particular test configuration. In order to carry out an objective comparison, the noise efficiency factor (NEF) and the dynamic range (DR) can be used as figures of merit (FoMs). Indeed, the NEF gives an idea of the noise efficiency of each solution, even though it does not take into account the maximum level of the input signal that can be processed, which is, however, considered by the DR. The measured NEF achieved by the proposed approach, equal to 16.0, can be considered as appropriate for the intended application, taking into account that, on the one hand, in a wide bandwidth IA it is not usual to use circuit techniques for noise reduction, such as chopping, and, on the other hand, an experimental DR of 50.1 dB is simultaneously achieved. The NEF and the DR have not been included in Table 2 because they are not available for the other solutions. Only in [28] a simulated DR equal to 30.8 dB is reported. Therefore, the experimental performance of the proposed IA results suitable for its use in bioimpedance spectroscopy applications.

V. CONCLUSION

The accuracy of a bioimpedance measurement system can be increased by raising the level of the excitation current. Nevertheless, safety considerations lead to a limitation of the maximum value of this signal. An alternative solution is based on increasing, when required, the voltage gain of the instrumentation amplifier used to acquire the corresponding voltage response at the bioimpedance under test. An electronically programmable instrumentation amplifier, suitable to be used in an automatic gain control loop, has been proposed. The approach exploits a continuously tunable current mirror that allows programming the voltage gain of the IA. The circuit implementation makes use of improved voltage followers, i.e., super source followers, which allow reducing the value of the linearization resistors. As a consequence, the overall noise can be reduced and a compact structure can be achieved. The proposed IA has been designed and fabricated in 180 nm CMOS technology to operate with a 1.8-V supply. Experimental results showed an extensive programmability range, beyond 45 dB, a wide bandwidth, over 3 MHz, and a high CMRR, above 86 dB, with relatively low power consumption and a reduced silicon area occupation.

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