# Carrier Level-Shifted Based Control Method for PWM 3L-T-type qZS Inverter with Capacitor Imbalance Compensation

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***Abstract*—This paper presents a modified carrier level-shifted based control method for a pulse width modulation controlled three-phase three-level T-type quasi-impedance-source inverter. The benefits of proposed strategy are a uniform distribution of shoot-through states of constant width throughout the fundamental period, and the mitigation of the inner capacitors' voltages imbalance. The latter is achieved by means of a proportional-integral controller, which adjusts the relative time application of redundant states. The improved performance is demonstrated in terms of reliability, as the capacitors do not suffer from neutral-point imbalance. The control method can also be implemented in a different multilevel inverter configuration with an impedance-source network. A comprehensive simulation study and several experiments were performed in order to validate the adopted method in situations of imbalanced capacitor voltages.**

***Index Terms*— Impedance-source converters, multilevel, pulse width modulation (PWM) inverters, three-level T-type quasi-impedance-source inverter (3L-T-type qZSI), T-type inverter, voltage imbalance.**

## I. Introduction

An increasing energy demand, lack of conventional energy resources, growing concern over environmental pollution, and concept of on-site energy generation have led to the rapid rise in renewable energy generators. Most of these generators are inverter-based, both in connection to the low-voltage distribution network and in islanded operation. As of 2015, many of them interact with photovoltaic (PV) modules [1], considered one of the most promising technologies, with a cumulative installation capacity of 227 GW [2]. Some studies have identified benefits in PV systems without galvanic isolation [3], as well as in the use of three-level inverter (TLI) topologies within the residential sector [4], [5]. The main advantages of the former include higher performance, higher power density, and lower cost – due to the absence of the transformer. In comparison with their two-level counterparts, TLIs show advantages in lower power switching losses from commutating only half of the DC link voltage, better harmonic performance at the output, and a reduced AC output filter [4].

A relatively recent multilevel topology is that of the T-type inverter [6], [7], causing several manufacturers to compete for a lead in the market. In comparison with the more mature neutral-point-clamped (NPC) [8], the T-type inverter only needs a single power switch to clamp the middle point to the positive or negative DC rail. This reduces conduction losses, consequently lowering power switching losses at lower switching frequencies [5]. However, because the outer switches of the T-type inverter have to block the full DC link voltage, the NPC inverter may be a better solution at higher switching frequencies, when switching losses become more significant [5]. Though the T-type is also constrained by performing just voltage-buck operations, recent solutions based on impedance-source (IS) networks [9]-[12] are able to overcome this limitation. IS based inverters do not suffer from shoot-through (ST) states, and most of them have continuous input current. This family of converters increases the input voltage range regulation [13], a typical requirement in PV installations, avoiding an intermediary DC-DC boost converter.

The three-level T-type quasi-impedance-source inverter (3L-T-type qZSI) has been proposed and analyzed in only a few pieces of literature [14], [15] but is considered a potential and competitive design in the field of PV inverters. Fig. 1(a) represents the considered topology and Fig. 1(b) shows its simplified switching circuit. The control and switching signal generation for this configuration must be carefully analyzed, and the balance of the neutral-point assured. There are several pulse width modulation (PWM) techniques that can be applied to IS based inverters, such as simple boost control (SBC) [16], maximum boost control (MBC) [17] and maximum constant

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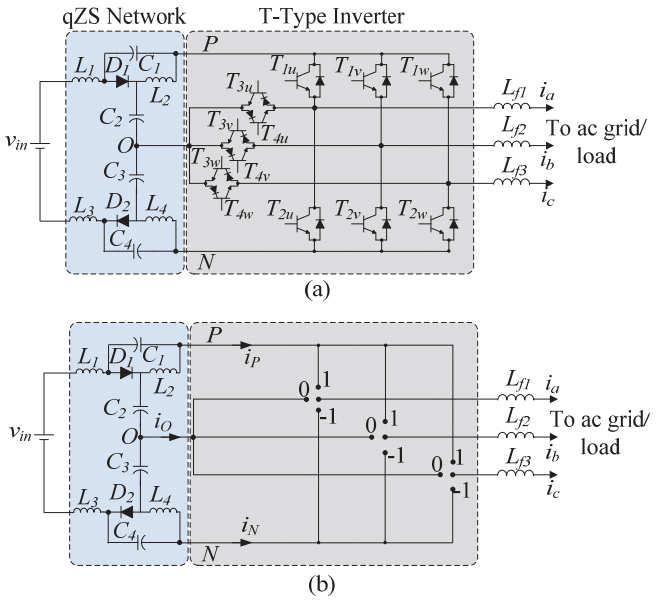


Fig. 1. Schematic circuit of 3L-T-type qZSI: (a) topology under study, and (b) switching model.

boost control (MCBC) [18]. These were later extended to control other IS multilevel inverters [19]-[21], but have not undergone analysis regarding mitigation of possible neutral-point voltage imbalances. Similarly, though control methods based on space-vector modulation (SVM) of the two-level counterpart have been modified for this family of IS multilevel inverters [22]-[24], the issue of imbalanced capacitor voltages has not been considered. Despite the increased popularity of IS multilevel inverters over classical multilevel inverters, there is a relative lack of research papers regarding the balance of neutral points [15], [25], [26]. This imbalance can be produced by incorrect control pulse generation, imbalanced loading conditions, and/or non-ideal capacitance values. Various modulation methods have been discussed for classical multilevel inverters facing this problem. Reference [27] proposes a PWM method with optimal switching frequency and [28] analyzes the stability of the neutral point by means of the dynamic model of the circuit. SVM approaches have demonstrated high effectiveness in reducing the neutral point imbalance [29] by implementing a selective harmonic elimination, since low frequency harmonics appear in this situation [30]. Other possible solutions to avoiding neutral-point voltage imbalance are predictive control and more robust DC-link capacitor designs [31]. Balancing neutral-point voltage is a very important issue in inverter reliability, as capacitors are considered key components of potential faults [32], [33].

This paper proposes a modified carrier level-shifted modulation technique for a 3L-T-type qZSI that is able to provide both uniformly distributed ST states and capacitor voltage imbalance compensation. The control technique can be easily extended to single-phase application, as well as to other IS or multilevel based topologies. The core idea was initiated in [26] and applied in a single-phase three-level neutral-point-clamped quasi-impedance-source inverter (3L-NPC qZSI) by simulation. The strategy is carefully and progressively explained and discussed (Section II). Then, the theoretical ideas are confirmed by simulations and experiments (Section III and IV).

## II. New Carrier Based Modulation Method for PWM Controlled 3L- T-Type qZS Inverter

This section progressively explains the operation principle of a 3L-T-type qZSI based on the proposed carrier level-shifted control strategy. The proposed method is conducted with the help of the 2-D vectorial representation depicted in Fig. 2. Here three-level switching states can be viewed as a two-level modulation system after an "origin-shifting" transformation is performed [19]-[21]. In Fig. 2, the considered reference phasor is shifted to the effective reference phasor with the "origin-shifting" process from ({-1,-1,-1}, {0,0,0}, {-1,-1,-1} to {1,0,0}, {0,-1,-1}). Then, the inverter modulation has equivalent active and zero states located in the vertices and center of the bolded two-level hexagon. By symmetry, six distinct shifted origins can be obtained, depending on the reference phasor angular position. Uniform distribution of ST states with constant width during the whole fundamental period (50 Hz) and the ability to mitigate the inner capacitor voltage imbalance are the main features of the new PWM methodology achieved. The former reduces the passive component rating of the IS network [33], and the latter improves reliability due to neutral point balance.

### A. ST Insertion and Differential Compensation

Three modulating signals $v^*_a$, $v^*_b$, $v^*_c$ ($\epsilon$ [-1,1] and per phase) and two triangular carriers (*carrier*$_1$, upper $\epsilon$ [0,1] and

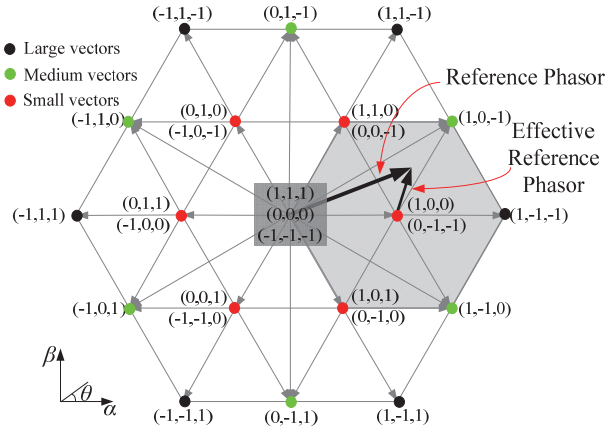


Fig. 2. Space vector representation of three-level inverter switching states.

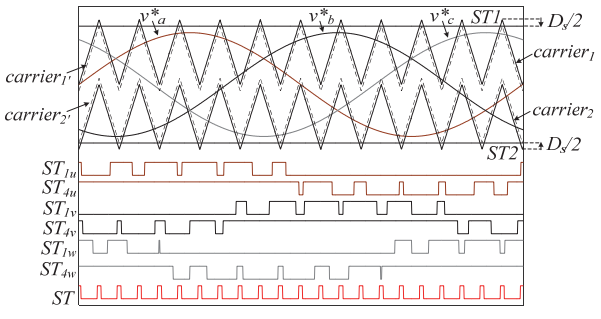


Fig. 3. New modulation for 3L-T-type qZSI with ST states.

*carrier*$_2$, lower ϵ [-1,0]) are compared to trigger different conventional states (see Fig. 3). Generation of the gate signals for switches $T_{1x}$ and $T_{4x}$ ($x$ = $u$, $v$ and $w$) are demonstrated in Fig. 3. $T_{3x}$ and $T_{2x}$ have complementary states to $T_{1x}$ and $T_{4x}$, respectively. Through this operation, the different voltage levels: 0, ± $v_{in}$/2, and ± $v_{in}$ are obtained, where $v_{in}$ is the input voltage. References *ST1* and *ST2* are used to produce the ST states. Operating in this way, uniformly distributed ST states of constant width are achieved throughout the output voltage period. Due to the insertion of the ST states, the output average phase-to-neutral voltage is modified, and the volt-second average is skewed, since they are not inserted during natural zero states. In order to maintain the volt-second average and assure the reference value, active and zero states are reconfigured by shifting upper and lower carriers by half of the ST duty cycle ($D_s$) [13]. This action makes that each inverter leg apply the half of the D-link voltage ($v_{dc\text{-}link}$/2) and -$v_{dc\text{-}link}$/2 more times during the positive and negative half-cycle respectively, in order to restore the normalized voltage. The certain amount of the half of the $D_s$ is because the symmetry of the triangular carrier wave.

A detailed switching period for when the reference phasor is located in the same position indicated in Fig. 2 is represented in Fig. 4. The corresponding state sequence is as follows: A {0,-1,-1} → B {0,0,-1} → C {1,0,-1} → D {1,0,0}. The initial state sequence is altered by the insertion of ST states into some original states. To respect the volt-second average, *carrier*$_1$ and *carrier*$_2$ are shifted to *carrier*$_{1'}$ and *carrier*$_{2'}$, respectively, by a value of $D_s$/2. This makes it possible to reconfigure a new state sequence with different state time widths (A′, B′, C′ and D′). This action is called “differential compensation”, because *carrier*$_1$ and *carrier*$_2$ are shifted by opposite signs (see Fig. 4), assuring the volt-second average.

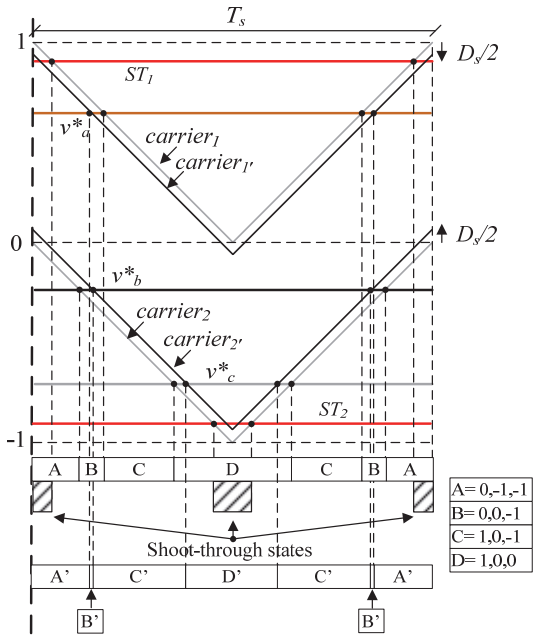


Fig. 4. Detail of switching period and action of differential compensation when the voltage reference phasor is in the triangle highlighted in Fig. 2.

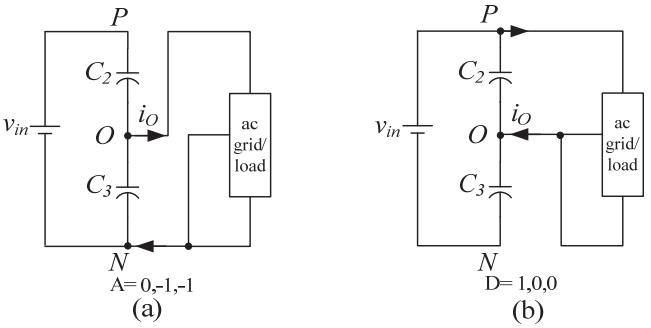


Fig. 5. Equivalent switching states in 3L-T-type qZSI: (a) small vector A, and (b) small vector D.

### *B. Neutral Point Imbalance and Common Compensation*

In Fig. 2, vectors with module length equal to $V_{dc}$ are called large vectors (e.g. {1,1,-1}), vectors with module length equal to $\sqrt{3}V_{dc}$/2 are medium vectors (e.g. {1,0,-1}), and the small vectors have module length equal to $V_{dc}$/2 (e.g. {1,0,0}) [29], [30]. The small vectors come in pairs (redundant states), with each vector in a pair generating the same line-to-line voltages. These pairs of redundant states connect a phase to the neutral-point, changing the sign of the current flowing in that direction. Fig. 5(a) and Fig. 5(b) represent the equivalent circuits of a pair of small vectors (A and D) involved in the state sequence where the reference phasor is located in Fig. 2. The task of the proposed neutral-point voltage balance control is to modulate the relative duration of the positive (A) and negative (D) small vectors within each switching cycle in order to maintain the balance of the neutral-point.

Fig. 6 has the same switching period as Fig. 4, and the reference vector is located at the same position as Fig. 2.

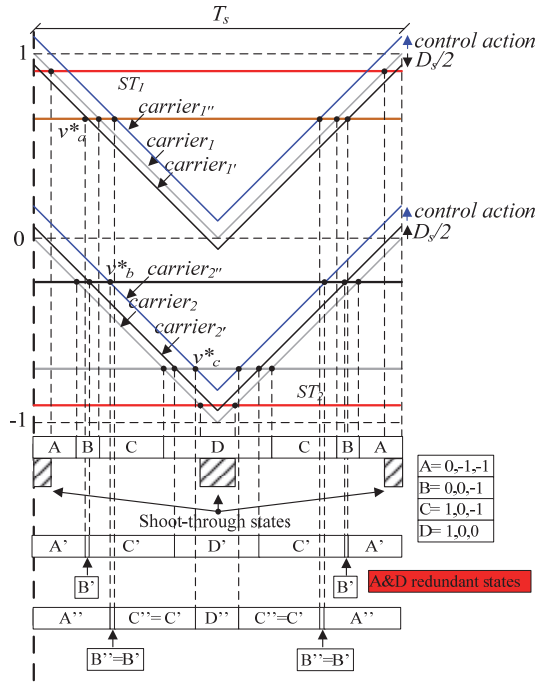


Fig. 6. Detail of switching period and action of common compensation when the voltage reference phasor is in the triangle highlighted in Fig. 2.

Because states A and D are small vectors and configure a pair of redundant states, they can be exchanged in order to charge or discharge capacitors $C_2$ and $C_3$ as necessary. By adding a common shift to $carrier_{1'}$ and $carrier_{2'}$, the relative duration of states A′ and D′ (already modified due to the differential compensation) is changed while the medium or large vectors remain the same. This figure represents the case in which $C_3$ presents a higher voltage than $C_2$, reducing the time duration of state D′ and consequently increasing the time duration of state A. The new state sequence (A′′, B′′, C′′ and D′′) just modifies the state time widths of redundant states.

Our proposal to generate this common shift (called "common compensation") to $carrier_{1'}$ and to $carrier_{2'}$ is based on the use of a proportional-integral (PI) controller. Depending on the error between voltage in the capacitor $C_2$ ($v_{C2}$) and in the capacitor $C_3$ ($v_{C3}$), the control action will be subtracted from the carrier signal levels. For example, when $C_3$ presents higher voltage than $C_2$, as in Fig. 6, both the error signal ($v_{C2}$-$v_{C3}$) and the control signal have negative values. When the control action (represented in blue) is subtracted from the carrier levels, both $carrier_{1'}$ and $carrier_{2'}$ "go up" ($carrier_{1'} \rightarrow carrier_{1''}$ and $carrier_{2'} \rightarrow carrier_{2''}$), increasing the relative time duration between A′′ and D′′, and producing the discharge of $C_3$.

## III. Simulation Results

To verify the above analytically described modulation method, simulations by help of MATLAB/Simulink were performed. Parameters of passive components as well as the ones of the conducted tests are represented in Table I. Passive elements of IS network were estimated according to the guidelines in [34] and [35] with the following equations:

$$L_{1,\dots,4} \geq \frac{v_{in}\,(1-D_s)\,D_s}{2\,i_{in}\,f_{sw}\,K_L\,(1-2D_s)}, \tag{1}$$

$$C_{1,4} \geq \frac{2\,P_{out}\,(1-2D_s)}{v_{in}^2\,K_C\,f_{sw}} \text{ and} \tag{2}$$

$$C_{2,3} \geq \frac{2\,P_{out}\,(1-2D_s)\,D_s}{v_{in}^2\,K_C\,f_{sw}\,(1-D_s)}, \tag{3}$$

where $L_{1,\dots,4}$ – quasi-impedance-source network (qZSN) inductance values, $v_{in}$ – input voltage, $i_{in}$ – input current, $f_{sw}$ – switching frequency, $K_L$ – assumed ripple in $i_{in}$, $P_{out}$ – output power, and $K_C$ – maximum voltage ripple across the capacitors.

For simplicity, an ordinary inductive filter was used with

TABLE I
Values Used in the Converter Design and Simulation Parameters

| Parameter | Unit | Value |
|---|---|---|
| Inductors $L_1, \dots, L_4$ | (mH) | 1.6 |
| Capacitors $C_1, \dots, C_4$ | (mF) | 1.1 |
| Switching frequency | (kHz) | 15 |
| Input voltage | (V) | 250 |
| $K_L$ and $K_C$ | (P.U) | 0.05 |
| $D_s$ | (P.U) | 0.12 |
| Output power | (W) | 500 |
| Output filter $L_{fi}$ ($i = a, b, c$) | (mH) | 3.6 |
| Load RMS voltage | (V) | 115 |
| $v_i(h_{SW})$ | (P.U) | 0.05 |
| $THD_I$ | (P.U) | 0.05 |
| Simulation step | (μS) | 0.5 |

an inductance calculated by following equation [36]:

$$L_f \geq \frac{v_i(h_{SW})\cdot V_g}{\omega_1 \cdot h_{SW} \cdot P \cdot THD_I}, \tag{4}$$

where $v_i(h_{SW})$ – harmonic component of the converter output voltage at the switching frequency, $V_g$ – RMS grid voltage, $\omega_1$– fundamental pulsation, $h_{SW}$ – switching harmonic order, and $THD_I$ – assumed total harmonic distortion of output current.

### A. Operation with ST and Differential Compensation

First test aims to validate the proper operation with ST states and the differential compensation action. Input voltage was set to 250 V with a balanced three-phase pure resistive load (3x100 Ω). $D_s$ equal to 0.12 was also considered. Simulation results of input voltage and input current ($v_{in}$ and $i_{in}$), DC-link voltage ($v_{dc\text{-}link}$), line-to-line voltages ($v_{ab}$, $v_{bc}$ and $v_{ca}$) before filtering and output phase currents ($i_a$, $i_b$ and $i_c$) with the $THD_I$ are shown in Fig. 7. Fig. 7(a) shows both $v_{in}$ and $i_{in}$. The converter is operating in continuous conduction mode (CCM). Fig. 7(b) represents $v_{dc\text{-}link}$, which drops to zero uniformly. This fact demonstrates the uniform distribution of ST states with constant width during the fundamental period. Fig. 7(c) depicts the line-to-line voltages before filtering, composed with the boosting levels of 0, ± $B$ $v_{in}$/2, and ± $B$ $v_{in}$, where $B$ represents the boost factor. The maximum value obtained (329 V) is in good agreement with the theoretical value ($v_{dc\text{-}link}$ = $v_{in}$ /(1-2 $D_s$)). The RMS values of output currents (Fig. 7(d)) prove the proper volt-second average.

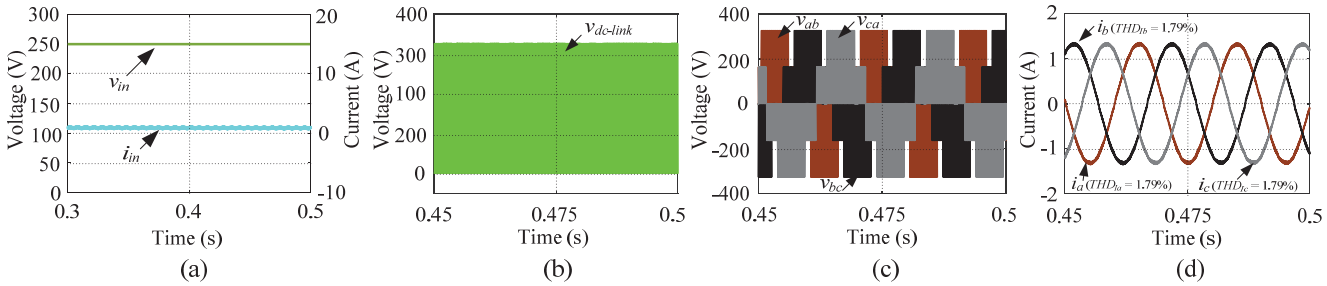


Fig. 7. Simulation results with modulation index equal to 0.8 and $D_s$ = 0.12: (a) input voltage and input current ($v_{in}$ and $i_{in}$), (b) DC-link voltage ($v_{dc\text{-}link}$), (c) line-to-line voltages ($v_{ab}$, $v_{bc}$ and $v_{ca}$) before filtering and (d) output phase currents ($i_a$, $i_b$ and $i_c$).

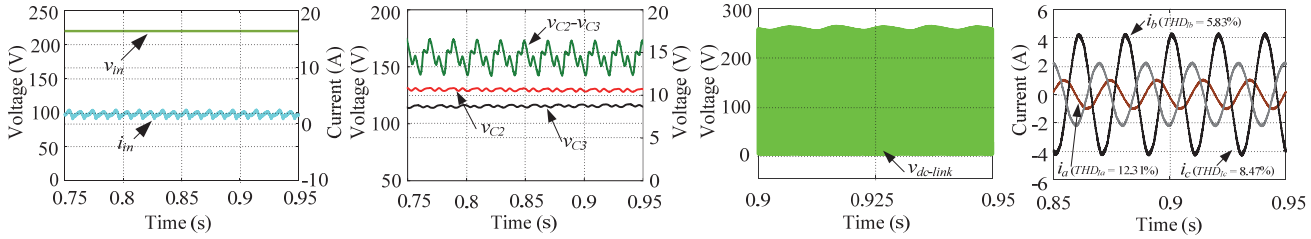


Fig. 8. Simulation results with modulation index equal to 0.8 and $D_s$ = 0.12 in unbalanced case, without common compensation: (a) input voltage and input current ($v_{in}$ and $i_{in}$), (b) voltages in capacitors $C_2$,$C_3$ and their difference ($v_{c2}$, $v_{c3}$ and $v_{c2}$-$v_{c3}$), (c) DC-link voltage ($v_{dc\text{-}link}$) and (d) output phase currents ($i_a$, $i_b$ and $i_c$).

### B. Operation with Unbalanced Conditions

Second simulation test is conducted to analyze the operation of the inverter in situations of imbalanced capacitor voltages. Different load and output filter values per phase are connected to the system in order to generate intentionally unbalanced voltages ($v_{C2}$ and $v_{C3}$). At the same time, to produce a greater imbalance, capacitors $C_2$ and $C_3$ have slightly different capacitance values. Table II summarizes these modified values, as well as the estimated constant values of the proposed PI controller, which will be further discussed in details. The rest of the parameters remain the same as in Table I.

In this simulation case, input voltage is set to 220 V and the same $D_s$ was also considered. The main simulated waveforms are represented in Fig. 8. Fig. 8(a) shows the input current and voltage, where a low frequency pulsation is appreciated. The low frequency pulsation, resulting from imbalanced conditions, is also seen in the DC-link voltage, depicted in Fig. 8(c). Fig. 8(b) shows the voltages across inner capacitors ($v_{c2}$ and $v_{c3}$) and their difference. As expected, $C_2$ exhibits a higher voltage, while $C_3$ has a higher ripple. The difference between them represents the voltage imbalance of the neutral-point. If this situation is not controlled, the converter may be damaged. The output current per phase (Fig. 8(d)) demonstrates the high degree of imbalance.

### C. Performance of the Common Compensation with Neutral-Point Unbalanced Conditions

The stability of our system with the proposed closed loop control scheme based on a PI controller, for mitigating the capacitor voltage imbalance is discussed in this section. The equivalent circuit for this situation is represented in Fig. 9(a),

TABLE II
NEW VALUES USED IN UNBALANCED CONDITIONS

| Parameter | Unit | Value | | |
|---|---|---|---|---|
| Capacitors $C_2$ and $C_3$ | (mF) | 1.1 | | 0.9 |
| Output filter $L_{fi}$ ($i = a, b, c$) | (mH) | 7.3 | 3.6 | 7.3 |
| Resistive load per phase | (Ω) | 100 | 23 | 47 |
| $K_p$ and $K_i$ (of PI controller) | | 0.2 | | 0.4 |

which allows different charge/discharge ratings of inner capacitors. The block diagram of the proposed PI based control is depicted in Fig. 9(b), where $\Delta v_c$ is the measured variable, $C(s)$ and $G(s)$ represent the transfer functions of the controller and plant, respectively, and γ is the common compensation control action. If $\Delta v_c$ has a positive value ($v_{c2} > v_{c3}$), then the control action γ will be positive, as demonstrated in Section II.B. Thus, the circuit can be more particularly represented by Fig. 9(c). In this case, the currents are calculated as:

$$\begin{cases} i_{C2} = i_{L1} - i_{load} \\ i_{C3} = i_{L4} = i_{L1} \end{cases}, \tag{5}$$

and the voltages across the inner capacitors:

$$\begin{cases} \Delta v_{C2} = \dfrac{1}{C_2}\int_0^{\gamma T} (i_{L1} - i_{load})\, dt \\ \Delta v_{C3} = \dfrac{1}{C_3}\int_0^{\gamma T} i_{L1}\, dt \end{cases}, \tag{6}$$

where $i_{Ci}$ and $i_{Li}$ – current across capacitor and inductance $i$, $i_{load}$ – current demanded from the load, and $T$ – switching period.

$\Delta v_c$ can be calculated as:

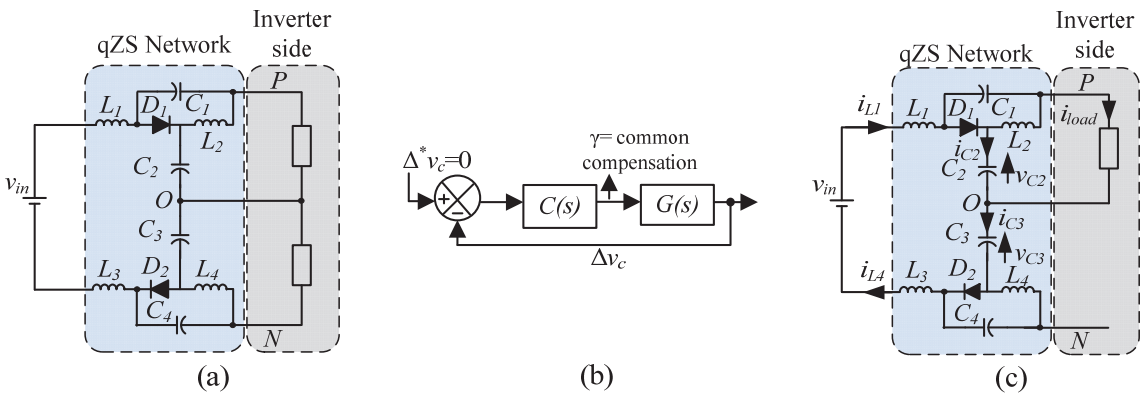


Fig. 9.(a). Equivalent circuit for unbalanced condition, (b) block diagram of proposed control and (c) circuit when $v_{c2}$>$v_{c3}$.

$$\Delta v_C = \Delta v_{C2} - \Delta v_{C3} = \frac{1}{C_2}\int_0^{\gamma T}(i_{L1} - i_{load})\,dt - \frac{1}{C_3}\int_0^{\gamma T} i_{L1}\,dt = \\ = \frac{C_2 - C_3}{C_2 C_3}\int_0^{\gamma T} i_{L1}\,dt - \frac{C_3}{C_2 C_3}\int_0^{\gamma T} i_{load}\,dt. \quad (7)$$

Assuming that $C_2 \approx C_3$ the expression can be simplified and solved as:

$$\left|\frac{\Delta v_C}{\gamma T}\right| = \frac{1}{C_2} i_{load} = K', \quad (8)$$

where $K'$ is a static gain that represents the transfer function of $G(s)$. The resulting closed-loop transfer function $G_{cl}(s)$ of the system is:

$$G_{cl}(s) = \frac{(K_p + K_i/s)K'}{1 + K'K_p + K_i K'/s}. \quad (9)$$

With the selected values of $K_p$ and $K_i$ (showed in Table II), and the rated values for $i_{load}$ and $C_2$, the stability of the system is guaranteed. This is further validated by plotting the closed loop transfer function (Fig. 10) because the zeros and poles of the closed-loop system are located on the left-hand side of the complex plane. It is important to note that these parameters must be carefully selected because they will affect the quality of output currents. The parameters used are considered to be a trade-off solution between imbalance mitigation capability and acceptable output quality.

The following simulation results are obtained once the PI controller dedicated to mitigate the voltage imbalance is enabled, at the same condition than the test of the previous section. In this case, the difference ($v_{c2}$-$v_{c3}$) (Fig. 11 (a)) is mitigated, at the expense of a slightly distorted output current (Fig. 11(b)). This reinforces the idea that control parameters should be carefully selected for their particular application. Finally, Fig. 11(c) shows the transient process of the PI control action. The reduction of the voltage difference ($v_{c2}$-$v_{c3}$) is achieved successfully. In this case, where $C_2$ has higher voltage than $C_3$, the control action has positive value and both carriers "go down". This means that small vectors or redundant states which discharge $C_2$ instead of $C_3$ have higher time durations.

## IV. Experimental Verification

An experimental prototype was built to further validate the proposed modulation method with imbalance compensation.

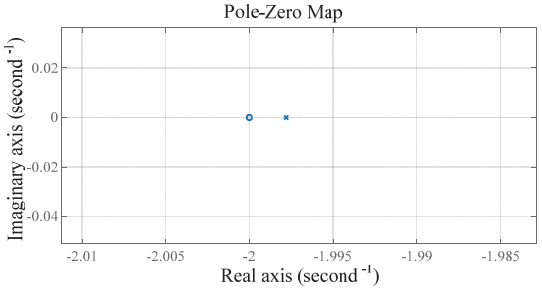


Fig. 10. Location of zeros and poles of the closed loop transfer function for selected $K_p$ and $K_i$.

This section summarizes the assembling procedure of the 3L-T-type qZSI, and describes the main components for experimental verification.

The 3L-T-type inverter assembly is based on the 12MB150VX-120-50 IGBT module from Fuji Electric (Fig. 12(a)). It is configured to have 1200V and 50 A 12 RB-IGBT in one package with highlighted advantages as size reduction and significant low power loss. The values of the passive elements (qZSN and output filter) are the same than the ones calculated for the simulation study. Diodes for the qZSN are based on the silicon carbide Schottky diode C3D10060G from CREE.

A driver board (Fig. 12(b)) for the AT-NPC 3-level 12in1 IGBT module is used to drive the power module, provided by Fuji Electric as well. Gate peripheral circuits are based on the ACPL-333J driver from Avago Technologies with a built-in function for short-circuit protection. The control unit is the dSPACE MicroLabBox (Fig. 12(c)) with a 2GHz dual-core real-time processor, programmable FPGA, and analogical/digital channels. The proposed carrier level-shifted modulation technique was programmed on a host PC in MATLAB/Simulink to run on ControlDesk software in real time at a sampling rate of 10 kHz. In order to embed the ST states into the conventional ones, another board with 74AC11032 chips (or gates) from Texas Instruments was designed. Finally, the measurement board (with the aim of implementing the common compensation to mitigate the neutral-point imbalance) includes two LEM LV 25-P voltage sensors. A general schematic of implementation of the proposed modulation technique and its different stages are represented in Fig. 13.

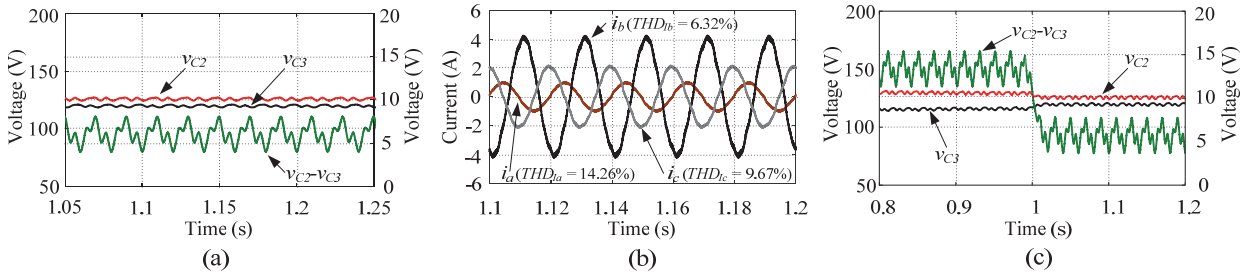


Fig. 11.(a). Simulation results with modulation index equal to 0.8 and $D_s$ = 0.12 in unbalanced case, with common compensation: (a) voltages in capacitors $C_2$,$C_3$ and their difference ($v_{c2}$, $v_{c3}$ and $v_{c2}$-$v_{c3}$), (b) output phase currents ($i_a$, $i_b$ and $i_c$) and (c) transient in inner capacitor voltages.

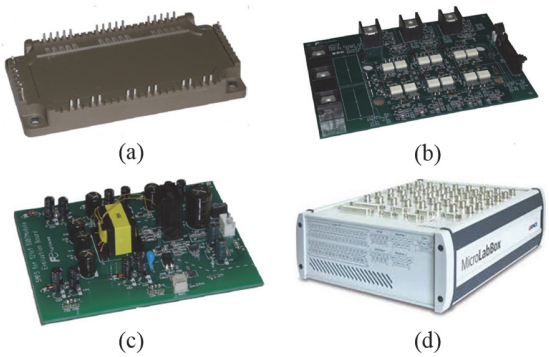


Fig. 12. Main hardware components for the prototype: (a) 12MB150VX-120-50 IGBT module, (b) driver board for AT-NPC 3-level 12in1 IGBT module, (c) auxiliary power supply driver board, and (d) dSPACE MicroLabBox.

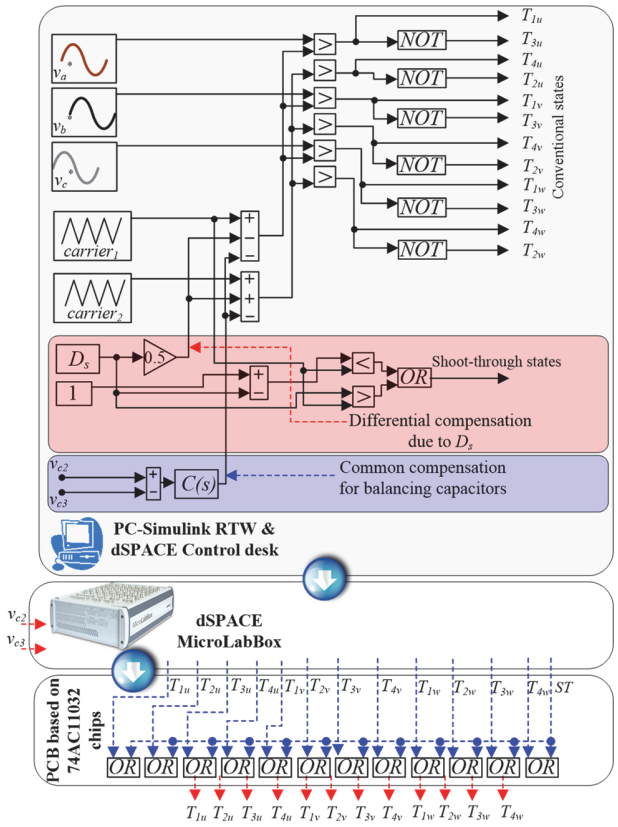


Fig. 13. Implementation of modulation method proposed and different stages for generating switching signals.

All measurements were made by a Yokogawa ScopeCorder DL850V digital oscilloscope, Chauvin Arnoux E3N current probes, and Tektronix TPP0051 voltage probes; Fig. 14(a) shows the full laboratory setup. The first test aims to validate the experimental setup with the proper switching of the 3L-T-type inverter. The same parameters in the real experiment than in the first simulation case are used ($v_{in}$ = 250 V and load (3x100 Ω)). Fig. 14(b) and Fig. 14(c) represent the main waveforms with modulation index equal to 0.8 and $D_s$ = 0. Fig. 14(b) shows the line-to-line voltages ($v_{ab}$, $v_{bc}$ and $v_{ca}$) before filtering, and Fig. 14(c) the output phase currents ($i_a$, $i_b$ and $i_c$). The different voltage levels of 0, ± $v_{in}$/2, and ± $v_{in}$ and sinusoidal currents with quite low $THD_I$ were obtained.

### A. Experimental test with ST and Differential Compensation

Fig. 15 shows the main experimental waveforms for validating the operation with ST sates and the differential compensation. $D_s$ = 0.12 is applied again. Fig. 15(a) shows both input voltage and current (the converter works in CCM), while Fig. 15(b) represents the DC-link voltage, that drops to zero uniformly during the fundamental period. Fig. 15(c) depicts the line-to-line voltages before filtering with the boosting levels of 0, ± $B$ $v_{in}$/2, and ± $B$ $v_{in}$. In this case, the maximum value obtained (326 V) matches quite well with the one obtained by simulation. Finally, in Fig. 15(d) we can see the output currents with a slight higher $THD_I$ (2.38%) in comparison with previous experimental case (without ST states, $THD_I$ was 1.85%), but still with very good quality.

### B. Experimental Results with Unbalanced Neutral-Point Conditions

This test analyzes the unbalanced situation without the PI controller for common compensation. Input voltage is set to 220 V, and the intentional imbalance is produced as in the corresponding simulation case (parameters were given in Table II). The main waveforms are depicted in Fig. 16. Fig. 16(a) shows the input current and voltage, with the expected low frequency pulsation resulting from imbalanced conditions. This effect is also transferred to the DC-link voltage, depicted in Fig. 16(c). Fig. 16(b) shows the voltages across inner capacitors ($v_{c2}$ and $v_{c3}$) and their difference. This neutral-point imbalance may be the cause of potential fault on the converter performance. The different output current per phase are represented in Fig. 16(d).

Fig. 17 shows the experimental results obtained after PI controller operation. The ripples of input current and DC-link voltage are quite similar to those in the situation without the controller (see Fig. 17(a) and Fig. 17(c)), but the difference ($v_{c2}$-$v_{c3}$) (Fig. 17 (b)) has been reduced adequately. The output current shown in Fig. 17(d) has a little bit more distortion than in the previous case without the common compensation. The $THD_I$ of each measured current was calculated and presented in Table III. It is worthy to notice the good agreement between simulation and experimental studies. Finally, the transient process of the PI controller action is represented in Fig. 18. The reduction of the voltage difference ($v_{c2}$-$v_{c3}$) is achieved very fast.

TABLE III
THD OBTAINED AND FUNDAMENTAL COMPONENT IN OUTPUT CURRENTS WITH AND WITHOUT COMMON COMPENSATION

| Case | $i_a$ | | $i_b$ | | $i_c$ | |
|---|---|---|---|---|---|---|
| | ***Fund. (A)*** | ***$THD_{Ia}$*** | ***Fund. (A)*** | ***$THD_{Ib}$*** | ***Fund. (A)*** | ***$THD_{Ic}$*** |
| Without Compensation | 0.7571 | 13.86% | 4.19 | 6.13% | 2.051 | 9.31% |
| With compensation | 0.7837 | 15.12% | 4.228 | 6.88% | 1.955 | 10.44% |

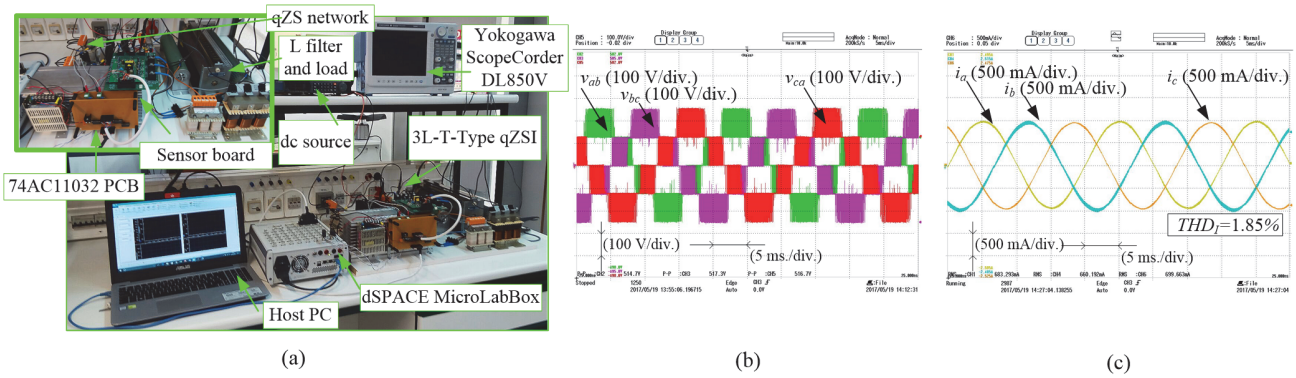


Fig. 14.(a) Full laboratory setup. Main experimental waveforms with modulation index equal to 0.8 and $D_s$ = 0: (b) line-to-line voltages ($v_{ab}$, $v_{bc}$ and $v_{ca}$) before filtering and (c) output phase currents ($i_a$, $i_b$ and $i_c$).

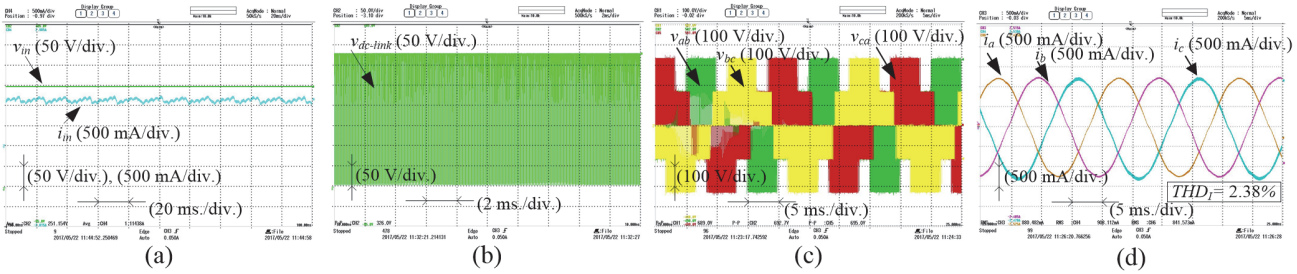


Fig. 15. Main real experimental waveforms with modulation index equal to 0.8 and $D_s$ = 0.12: (a) input voltage and input current ($v_{in}$ and $i_{in}$), (b) DC-link voltage ($v_{dc\text{-}link}$), (c) line-to-line voltages ($v_{ab}$, $v_{bc}$ and $v_{ca}$) before filtering and (d) output phase currents ($i_a$, $i_b$ and $i_c$).

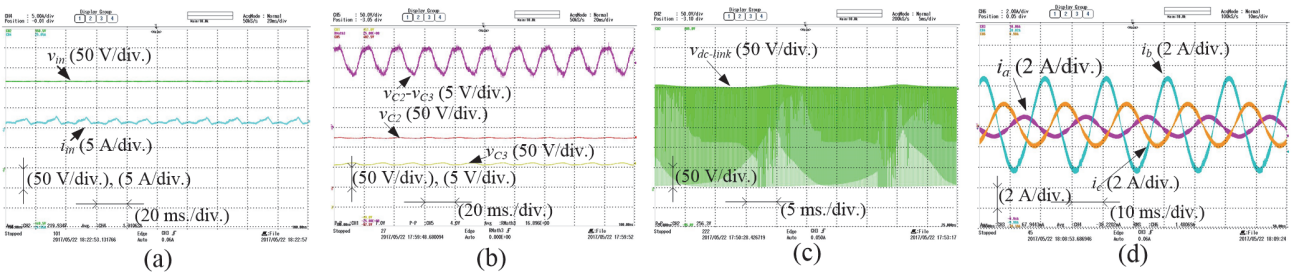


Fig. 16. Main real waveforms with modulation index equal to 0.8 and $D_s$ = 0.12 in unbalanced case, without common compensation: (a) input voltage and input current ($v_{in}$ and $i_{in}$), (b) voltages in capacitors $C_2$,$C_3$ and their difference ($v_{c2}$, $v_{c3}$ and $v_{c2}$-$v_{c3}$), (c) DC-link voltage ($v_{dc\text{-}link}$) and (d) output phase currents ($i_a$, $i_b$ and $i_c$).

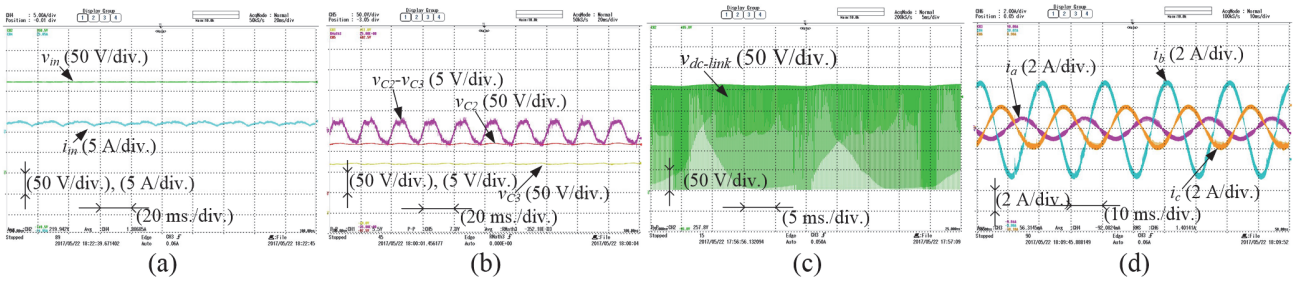


Fig. 17. Main real waveforms with modulation index equal to 0.8 and $D_s$ = 0.12 in unbalanced case with common compensation: (a) input voltage and input current ($v_{in}$ and $i_{in}$), (b) voltages in capacitors $C_2$,$C_3$ and their difference ($v_{c2}$, $v_{c3}$ and $v_{c2}$-$v_{c3}$), (c) DC-link voltage ($v_{dc\text{-}link}$) and (d) output phase currents ($i_a$, $i_b$ and $i_c$).

## V. Conclusion

This study has proposed a new modulation technique that can be applied to any IS based multilevel inverter. Its main capabilities include generating ST states of constant width throughout the entire fundamental period, and balancing the neutral-point voltage altogether. These advantages allow the reduction of the passive component rating, and increased reliability in comparison with previously reported methods. The proposed idea is successfully validated by simulations and by a prototype based on the 3L-T-type qZSI topology. The selection of the controller parameters directly affects the quality of the output current. The method also presents a high level of simplicity in its implementation.

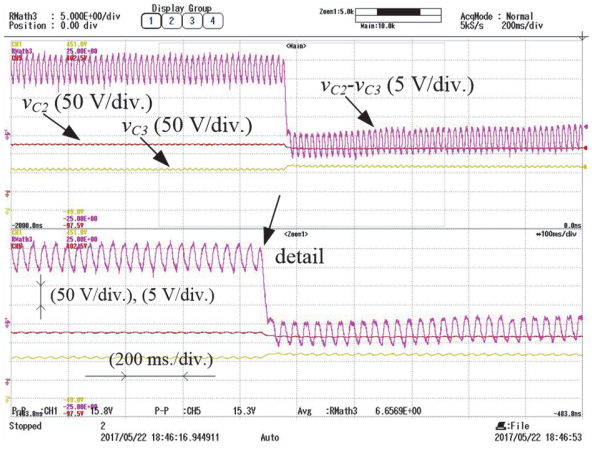


Fig. 18. Transient in inner capacitor voltages.

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