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Inversor Tipo String Basado en Red Cuasi-Z para Aplicación en Fotovoltaica Residencial

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Quasi-Z-Source Based String Inverter For Residential Photovoltaic Application

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Declaration

I hereby declare that this submission is my own work and achievement for the doctoral degree at University of Extremadura, and it does not contain material which has been accepted for the award of any other academic degree or diploma of the university or other institute of higher learning.

Elena Santasheva

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Abstract

Nowadays the industrial PEC for residential PV application is based on the well-known dc-dc boost converter and dc-ac inverter. In such topologies, the power goes through two conversion steps (dc-dc and dc-ac), therefore it is necessary to prevent the ST state by introducing the dead-time between the switching of the inverter switches that complicates the control system.

The solar PEC has the PV system in the input side, which leads to the following: the PEC should be able to regulate the input voltage in a wide range, provide CIC and have battery storage especially for residential application. The main task of the battery is to provide the power balance between the input and the output power in case of power misbalance that can occur between them. It can be caused by changing of the operation point of the PV system that could be affected by different reasons (solar irradiance/temperature variation) or load variation. Also, the battery storage should be able to provide the power when the input power is absent, for instance, during dark periods.

High DFR of the input power in single-phase inverters deteriorates the efficiency of the MPPT. In order to reduce the DFR of the input power, usually the E-cap with high value of capacitance in the input side is used. This solution has some drawbacks, the E-cap is the weakest part of the whole system; it is very sensitive to the current ripple and the capacity of the E-cap is reducing with time. As a result, generally it should be replaced every five years. In order to use other types of the capacitor such as film or ceramic, it is necessary (based on the market supply capabilities) to reduce the required value of capacitance of the decoupling capacitor. In order to achieve this goal, different approaches of the power decoupling (which in general can be divided into two types: the PPD and the APD approaches) have been proposed in the literature.

All the points above allow us to improve the efficiency, the reliability of the system, but the main task of the solar PEC is to provide the required quality of the power at the PCC with all discussed features.

This work was dedicated to the novel concept of the PEC based on the ISN. The PEC has benefited from qZSN through such positive properties as ST immunity, CIC. To provide the required power to the grid the BIC was proposed, which is able to provide the power even without the input source. To achieve the required quality of the grid current, the dPR controller with the HC circuit was selected; to avoid the current spike

during the start-up period, which may cause the current trigger protection, the optimization process of the dPR controller was proposed. To stabilize the dc-link voltage during the boost mode, the PID controller was used. To compensate the additional power losses caused by BIC, the APD approach realized by means of the specific control strategy of the BIC was proposed.

The theoretical results were confirmed by experimental results that were achieved by building up the qZSI with a BIC prototype. The tests showed that the designed qZSI with BIC can be applied for residential PV application.

Resumen

Actualmente el PEC usado en las instalaciones fotovoltaicas del ámbito residencial, está basado en el convertidor DC-DC y el inversor DC-AC. En estas topologías la potencia pasa por dos etapas de conversión (DC-DC y DC-AC) y existe la necesidad de prevenir el estado ST, introduciendo un tiempo muerto entre la conmutación de los interruptores,

El hecho de que el PEC en cuestión esté conectado a un sistema fotovoltaico conduce a lo siguiente: el PEC debe ser capaz de regular la tensión de entrada en un amplio abanico de posibilidades, proporcionar CIC y tener almacenamiento de baterías, especialmente en su aplicación en el ámbito residencial. La tarea principal de la batería es subsanar el problema de desequilibrio de potencia entre la entrada y la salida. El desequilibrio suele producirse debido al cambio del punto de funcionamiento del sistema fotovoltaico o debido a variaciones de carga. El punto de funcionamiento puede variar por diferentes razones: irradiancia solar o variación de la temperatura. En cuanto, a la batería debe ser capaz de proporcionar la potencia necesaria cuando el sistema fotovoltaico no pueda por si solo, por ejemplo, durante la noche o durante el transcurso de las inclemencias meteorológicas.

El alto DFR en la potencia de entrada en inversores monofásicos empeora la eficiencia del MPPT. Para reducir el DFR de la potencia de entrada se utilizan generalmente E-cap con alto valor de capacidad en el lado de entrada. La solución basada en E-cap presenta ciertos inconvenientes que lo convierten en la parte más débil del sistema, ya que es muy sensible a las pulsaciones y además su capacidad se reduce con el tiempo (con un tiempo de reemplazo de unos 5 años). Existe una necesidad del mercado de reducir la capacidad del condensador de desacoplamiento, por lo que se está sustituyendo por otro tipo de condensadores como pueden ser los films o los cerámicos. Para lograr este objetivo en la literatura se propusieron diferentes enfoques de desacoplamiento de potencia (que en general se pueden dividir en dos tipos: los enfoques PPD y APD).

Todos los puntos mencionados anteriormente permiten mejorar la eficiencia y la fiabilidad del sistema, pero la principal tarea del PEC fotovoltaico es proporcionar una potencia en el PCC con niveles adecuados de calidad.

Este trabajo presenta un novedoso concepto de PEC basado en ISN o qZSN, que permite introducir mejoras en cuanto a la inmunidad en ST y CIC. Para proporcionar la energía necesaria a la red se propuso el BIC, que es capaz de proporcionar energía incluso sin fuente de entrada. Para lograr la calidad requerida en la corriente de red se elige el

controlador dPR con circuito HC, el cual permite además evitar los picos de corriente producidos durante el período de arranque, evitando así la actuación de la protección de corriente. A la hora de abordar el problema de estabilizar el pico de la tensión del bus de continua durante el proceso de arranque, se propone un controlador PID, mientras que para compensar las pérdidas de energía adicionales causadas por el BIC se propone el enfoque de APD.

Los resultados teóricos han sidos confirmados por los resultados experimentales obtenidos mediante la construcción del prototipo qZSI con BIC. La realización de los ensayos experimentales demostró que el qZSI diseñado con BIC se puede aplicar en instalaciones PV residencial.

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Nomenclature

VSI	Voltage - Source Inverter
CSI	Current - Source Inverter
PV	Photovoltaic
PVS	Photovoltaic System
PEC	Power Electronic Converter
NPC	Neutral - Point Clamped
qZSI	quasi - Z Source Inverter
RES	Renewable Energy Source
DFR	Double Frequency Ripple
LPF	Low Frequency Ripple
APD	Active Power Decoupling
PPD	Passive Power Decoupling
DDFR	Double Damped Frequency Ripple
PDN	Passive Distribution Network
ADN	Active Distribution Network
CCM	Continuous Current Mode
OSFET	Metal emiconductor Field Effect Transistor
PWM	Pulse Width Modulation
AC	Alternative Current
DC	Direct Current
EMI	Electromagnetic Interference
DGS	Distribution Generation System
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electrotechnical Commission
IS	Impedance Source
ISN	Impedance Source Network
MPPT	Maximum Power Point Tracking
qZSN	quasi – Z - Source Network
ST	Shoot - Through
CIC	Continuous Input Current
DIC	Discontinuous Input Current
PF	Power Factor
FOC	Field Oriented Control
VOC	Voltage Oriented Control
DTC	Direct Torque Control

DPC	Direct Power Control
SVM	Space Vector Modulation
SPVWM	Space Vector Pulse Width Modulation
PI	Proportional Integer
PR	Proportional Resonant
dPR	damped Proportional Resonant
HC	Harmonic Compensation
MPC	Model Predictive Control
qZS	quasi - Z - Source
RESS	Renewable Energy Source System
PID	Proportional Integer Derivative
E-cap	Electrolytic capacitor
ESRs	Equivalent Series Resistors
dPR	damped Proportional Resonant
MPP	Maximum Power Point
AD	Analog Digital
FPGA	Field-Programmable Gate Array
DSP	Digital Signal Processor
PLL	Phase Locked Loop
SOGI	Second Order Generalized Integrator
LPF	Low Pass Filter
BIC	Battery Interface Converter
SPI	Serial Peripheral Interface
C1- C4	capacitors of the qZSN
L1- L4	Inductors of the qZSN
C_B	buffer capacitor
L_B	buffer inductor
Bat	battery of the battery interface converter
D_{01}-D_{04}	blocking diodes
D_1, D_2	diodes of the qZSN
Li	inductor of the inverter side filter
Lg	inductor of the grid side filter
Cf	filter capacitor
Rfi, Rfg, Rd	parasitic resistances
Ds	shoot-through duty cycle
Da	active state duty cycle
S1-S8	inverter switches
T1, T2	switches of the battery interface converter
Cout	output capacitor in unfolding circuit
Lout	output inductor in unfolding circuit
Rout	output resistor in unfolding circuit
Pin	input power
Pg	grid power
Vin	input voltage
Vg	grid voltage

Iin	input current
Ig	grid current
Ibat	battery current
Ib	current across active power decoupling circuit
Ds	shoot - through duty cycle
Da	active duty cycle
Vdc	dc-link voltage
Vc	voltage across capacitors C2+C3
T	line period
tsw	switching period
ton	ON - state time duration
toff	OFF - state time duration
fsw	switching frequency
T_{sw}	switching period
E_{LW}	energy stored in the inductors
E_{CW}	energy stored in the capacitors
T_W	total voltage stress on the switching devices
Vmax	maximum voltage across capacitors
Iave	average current across inductors
v_L	instantaneous voltage across inductor
v_C	instantaneous voltage across capacitor
V_T	reverse voltage on the semiconductor devices
i_L	instantaneous current across inductor
i_C	instantaneous current across capacitor
i_{S0}	instantaneous current across intermediate switch
i_{out}	instantaneous output current
v_{out}	instantaneous output voltage
K_{C1}, K_{C2}, K_{CB}	ripple coefficient of voltage across capacitors C_1, C_2, C_B
K_{L1}, K_{L2}, K_{LB}	ripple coefficient of current across inductors L_1, L_2, L_B
Cu	capacitor in an equivalent unit
Lu	inductance in an equivalent unit
L	output inductor
C	output capacitor
R	load resistance
ω	line frequency
ωc	cut-off frequency
φ	phase shift
TrF	transfer function
G	transfer function
Isc	shoot-through current
Immp	current at the MPP
Voc	open circuit voltage
Vmpp	voltage at the MPP
Empp	efficiency of the MPPT block
Econv	efficiency of the converter

E%	solar irradiance in percentage from nominal value

Chapter 1
Introduction

1.1 Definitions of the residential PV Inverter

Today we can observe how the power plants are shifting from being centralized power grid to becoming decentralized power grid/micro-grid due to the rising interest in the Renewable Energy Sources (RES), where the Photovoltaic Systems (PVs) are the most promising among Renewable Energy Sources Systems (RESs). A typical centralized power grid consists of:

- centralized generator (powerful synchronous generator) that sets the frequency of the grid and equals 50 Hz or 60 Hz, and the voltage of the grid, rms value equals 230 V. It is characterized as steady and dispatchable, including inertia, speed governing, excitation control [1],[2];
- transmission network that transfers the electricity from the centralized generator to a substation where the voltage of the electricity is decreased;
- distribution network delivers the electricity to the consumers/load;
- distribution generator is an additional power plant that produces power; it is usually located near the consumers/load. It can be connected to the distribution network or to the load in stand-alone mode. It could be the synchronous generator of smaller in size than the centralized generator or RES. The RES is characterized as variable, non-dispatchable, inverter-based, distributed;
- consumers/load.

The shift from being centralized to becoming a decentralized power grid is motivated by the fact that the electricity power socket is overloaded with too many plugs and in order

to sustain the power supply, making just some upgrades could be more expensive than the creation of a new, independent from the fuel cell, a decentralized power grid, which can also be more cost effective [3].

The string technology is a demanded solution where high power/voltage of the PVs is required, such as residential application. But since the PVs are characterized as a time-varying source due to their intermittent nature of the power production, this common Photovoltaic (PV) issue is crucial, because it depends on the temperature, solar irradiance, and the PVs do not produce the power during the night period. One of the major drawbacks of the string technology lies in its poor energy utilization at partial shadowing, where it can lead to the power fluctuation in the Distributed Generation System (DGS). Earlier when the penetration level of the RES into the DGS was not so high, its effect on the stability of the parameters of the grid was not critical because their capacities were significantly lower than the capacity of the central generator. So the shift is motivated also by the fact that the increasing level of the penetration of the RESs into DGS was starting to cause the instability of the grid, and the centralized generator was incapable of providing the stability of the system anymore. The decentralized power grid can consist of:

- distribution generator (micro turbine generator and RES);
- distribution network;
- energy storage;
- consumers/load.

The residential micro-grid may consist of one house, where the power produced by the PVs would be spent for its own needs, or of few houses in which case the community may share the produced power between each other or transfer the surplus of power to the main grid. One of the examples of such grids was built in the Netherlands, “The Aardehuizen: a neighbourhood microgrid” [3].
In order to connect the dc power produced by PVs and the ac sources or ac load, it is necessary to use a Power Electronic Converter (PEC), a residential PV inverter, as an interface inverter in a residential micro-grid. Earlier the PEC operated as a Passive Distributor Network (PDN) that could not provide the support of the grid. It only could inject the current into the grid with THD lower than 5%, which had to be synchronized with the grid voltage. However, high penetration level of the RES into DGS in the centralized power grid and the creation of the decentralized power grid led to the necessity to expand the functions of the PEC. In 2013, the Institute of Electrical and Electronics Engineering (IEEE) 1547 and International Electrotechnical Commission (IEC) 50438 were revised and the interface inverter was considered as an Active Distributor Network (AND). The ADN with a wider function can provide the frequency/voltage support of the grid. The review of the updated standards is presented in Chapter 2.

As stated earlier, the PVs produce unstable voltage, which forces to use the boost stage. In the industry, the traditional dc-dc boost converter was used. The Voltage Source Inverter (VSI) or Current Source Inverter (CSI) with a boost dc-dc converter cannot provide more than twice higher input voltage regulation ratio and this solution is topologically more complex and harder to control, because of the two-stage power conversion. One of the alternative approaches is based on an intermediate Impedance-Source Network (ISN) [1]-[3]. The ISN provides Shoot-Through (ST) immunity that makes the control strategy simpler, since there is no need to introduce dead-time and it can operate in a buck, and in a boost mode. These inverters based on the ISN are capable of performing Maximum Power Point Tracking (MPPT) with no need for using an auxiliary or extra dc-dc converter. Different types of the ISN have been proposed, such as the Trans-source[4],[5], Y-source [6],[7], EZ-source containing the coupled inductors within[8], [9] and the LCCT-Z-source[10]-[12], Γ-Z-source that contains the transformer within[13],[14] in the literature so far. In [15] authors present the brief review of the different configurations of the impedance networks. Not all of the proposed ISN are suitable for PV application because they provide Discontinuous Input Current (DIC) such as: Z –source [16], Trans-Z –source, LCCT-Z - source, Y-source, Γ-Z-source. Among the ISN which provides the CIC the quasi-Z-Source Network (qZSN) looks more attractive for PV application because it provides lower input current ripple in comparison to the: EZ – source, Trans-quasi-Z – source[17], and it contains a lower number of the passive elements than LCCT-quasi-Z source network [18].

One of the possible decentralized power grids is presented in [PAPER-I] where the decentralized system contains a small synchronous generator and a few different types of the RES, but the grid fault had occurred and the rest part of the decentralized power grid started to operate in a stand-alone mode. In this system, the PECs were connected in parallel and at the grid fault, one of the PEC that had higher capacity than others was able to change its operation mode from the CSI to the VSI and mimic the behavior of the absent synchronous generator, and started to set the frequency and voltage of the grid based on the load demands. Other PECs in the stand-alone mode kept operating in a normal mode; moreover, they could provide the support of the virtual synchronous generator in the case of a change in the load demand by means of the droop control that is a new available function accepted by updated standards. The droop control is a function that allows us to maintain the voltage and frequency of the grid parameters by changing the active and reactive power production.

Since the load power can fluctuate during the day in a residential micro-grid, and the PV system produces non-stable power value during the day, it is mandatory to use the battery as part of the whole system in order to achieve the power balance.

The residential PV inverter is a small scale power generator which has the power capacity of up to 5 kW [18]. It should be able to regulate input voltage in a wide range which means that it should consist of some boost stage. It should provide CIC and the required quality of the produced current. In order to improve the efficiency of the MPPT

block, it should be able to reduce the DFR of the input power and provide power balance between the produced power and the required power by the load by means of the battery integration.

Currently, the research of quasi-Z-source inverters (qZSI) showing their application for residential application is very limited.

The main goal of this work is to optimize the performance of the novel solar inverter based on the quasi-Z-source network with energy storage utilization making it suitable for residential application. The optimization is concerned with optimal control strategies along with passive components size and volume reduction keeping predefined power quality and level of MPPT performance.

1.2 Hypothesis and Tasks

The aim of the PhD research is to design and experimentally validate a single-phase qZSI with storage integration to be applied for residential application.

Hypothesis:

- The usage of the three-level NPC inverter allows us to improve the quality of the power at the PCC, whereas reducing the voltage stress on the semiconductor devices allows the use of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors with increased frequency;
- The qZS network allows an increase of the input voltage up to the required level on the dc-link and maintain it in a wide range of the input voltage;
- The interface storage converter allows us to provide the power balance between the input and the output sides and even to feed the consumers/load in the case of the absence of the power produced by PV panels;
- The decoupling approach allows us to mitigate the double-frequency ripple of the input power.

Tasks:

- To overview and select the topology of a dc-ac converter that is able to provide a wide range of input voltage regulation along with the capability of battery storage integration;
- To estimate the best decouping approach which ables to mitigate double-frequency ripple of input power taking into account overall power density, overall efficiency and cost;

- To design and improve the grid-connection and battery control strategies for an dc-ac converter with battery storage utilization, a wide range of power and input voltage regulation in terms of stability and power quality at the PCC;
- To verify the developed solution of a solar inverter with battery storage utilization for residential application.

1.3 Scientific Novelties

- New quasi-Z-source based inverter with storage energy integration and unfolding circuit;
- New modified three-level NPC quasi-Z-source inverter with combined storage integration and active decoupling capability;
- Novel tuning approach of the proportional-resonant controller for grid current control strategy with optimized start up transient;
- Comparative analysis of the passive and active power decoupling approach for double-frequency ripple elimination in ISN based converters.

1.4 Practical Outcomes

- Design guidelines for the decoupling approach, its goal is to reduce the DFR of input power and improve the MPPT performance;
- Mathematical guidelines to tune up the applied controllers;
- Design guidelines to optimize the damped Proportional Resonant (dPR);
- Experimental prototype of a single-phase ISN based solar inverter.

1.5 Confirmation and Dissemination of Results

The results of the doctoral thesis have been disseminated at 6 international conferences, at 8 doctoral schools and 2 scientific journals.

The author has published 12 international scientific papers indexed by IEEE Explore, 6 of them associated with the doctoral thesis. The most important papers directly connected to the topic of the dissertation are listed in the Appendix.

Chapter 2
State-Of-The-Art of Residential String Inverters

This chapter gives an overview of the standards of the residential grid-connected PV inverters, which change over time, new functions added due to the high penetration level of the RES into DGS. Also, it reviews different control strategies of the grid connected inverters where the main tasks are to provide the required quality of the grid current even if the grid voltage is distorted, provide fast dynamic response and zero steady-state error. Final goal is to describe power electronics topologies that can be applied for residential PV application, where the most important issue is to provide the regulation of the input voltage in a wide range and to provide CIC.

2.1 Overview of existed standards and requirements

Different countries are applying different standards. The IEC 50438[19] standard is being applied in European countries such as Estonia and Spain, while the IEEE 1547 standards and Rule 21 [1], [2] were designed for the USA. The main differences between these two territories are the parameters of the grid. The reference voltage is 240 V and the frequency is 60 Hz in the USA, while in Europe it is 230 V and 50 Hz correspondingly.

The IEC 50438 standard dates back to 2013, since that time, it has been revised and some changes have been introduced in order to improve the reliability, safety, stability of the grid, the power quality, and control over generation, and storage capabilities, taking into account more specific features of the cooperation between the RES and the DGS. For instance, the tests for verification of interface protection, islanding detection have been

modified; the test of the direct current injection has been added [1] and new functions were added, such as:

- Voltage/Frequency Ride Through. The mentioned standards set clearing time and voltage/frequency deviation from the nominal value in the DGS; during that time, the inverter may stay connected to the grid, but if the anomaly exceeds the clearing time or available voltage/frequency deviation, the inverter should be disconnected. The available voltage/frequency deviation and clearing time are presented in TABLE 1.
- Dynamic Volt/VAr control regulates the voltage fluctuation by injecting or absorbing the reactive power into DGS, Figure 1 between points 1 and 4. The PVs or/and load change can cause the voltage fluctuation in the DGS. If the voltage fluctuations are higher than it is set in Table 1 (Points 1 and 4 in the Figure 2.1), the RES should be disconnected. The Volta/VAr curve can include the deadband or not.

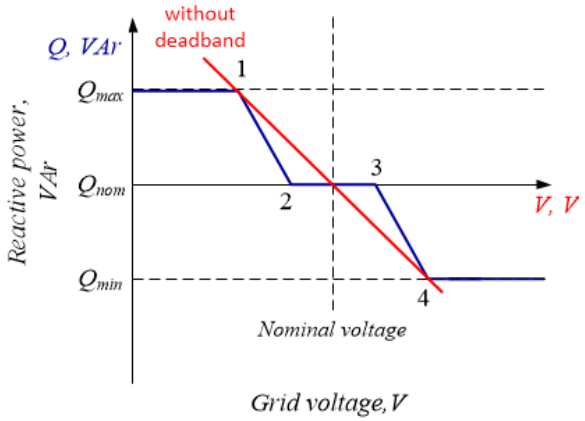


Figure 2.1 Volt/VAr curves.

- Dynamic Freq/Watt control regulates the frequency deviation. The load change may cause the frequency deviation in the DGS. The PEC can provide the frequency support of the DGS by regulating the active power production, between points 1-4 Figure 2. If the frequency fluctuations are higher than it is set in Table 2.1 (Points 1 and 4 in Figure 2.2), the RES should be disconnected. If the frequency deviation exceeds points 2 or 3, then the active power change rate should be equal to 10%/Hz. Without this control and at the over frequency, the inverter increases active power production that may deteriorate the parameters of the grid [20].

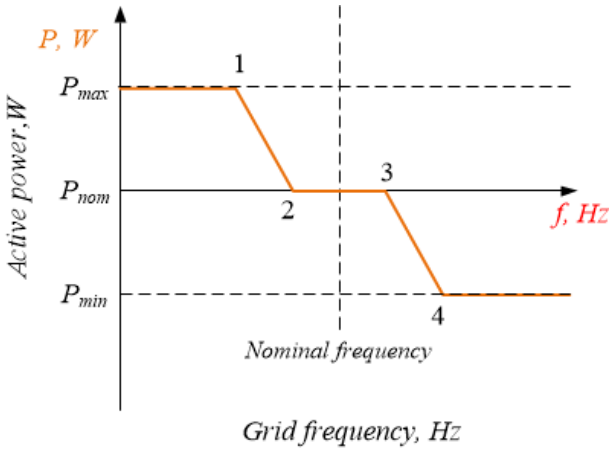


Figure 2.2 Freq/Watt curve.

- Ramp-up power rates. After disconnection when it comes to reconnect the RES to the DGS and if the reconnection is done simultaneously (Curve 1 in Figure 2.3), it may cause the large spike of the active power in the grid and the instability of the system or the frequency deviation. The suitable power rate slope should be set in order to smooth the transition process (Curve 2 in Figure 2.3). There is also another method that allows avoiding any negative subsequences of the reconnection of the RES into the DGS, which is to separate their reconnection time. This method is named as the ”Soft Start“. As a result, the reconnection process can be divided based on two types: ramp-up power rates and random switch within a time window. According to the IEC 50438 standard, in Estonia the RES may start the reconnection process if during 1 minute the voltage range is between 85%-110% and the frequency range is between 47.5 Hz-50.05 Hz.
- Non-Unity Power Factor (PF). Recent PV inverters operated with unity PF, which is unsuitable today because of different types of load that can introduce reactive power into the DGS and other various RES types that can change PF in DGS as well, and some shift may occur due to the large scale of feeder especially in the case of the high penetration level of RES into the DGS. To compensate their influence and improve the stability of DGS, it is required to vary the PF of the PV inverter to regulate voltage by injecting/absorbing the reactive power. Different studies have focused on the influence of different values of the PF [21]. In [22] authors performed an experimental comparison with lead and lag PF. Non-unity PF increased the losses across semiconductor devices of the PV inverter that reduced their lifetime.

According to their results, it was more preferable to set the lag PF since it caused lower energy losses compared to lead PF. The approach proposed in [23] allows control of the flow of the reactive power into the system; their method was named the ”Q at Night“. In [24] authors report their experimental results where they changed the PF between 80% leading and 80% lagging, which caused a change in the reactive power without influencing the active power.

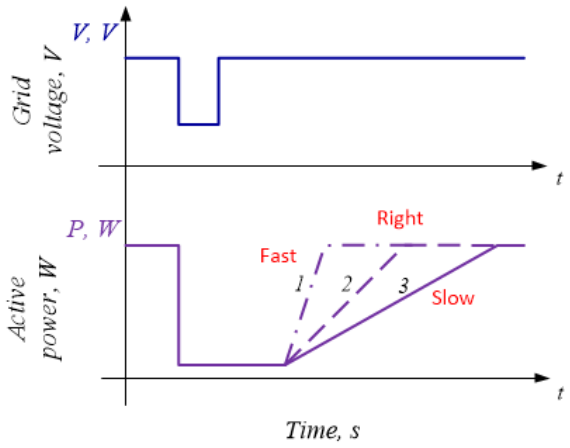


Figure 2.3 Ramp-up power rates.

It is expected that wider functionalities allow more accurate response to a voltage and a frequency deviation of the grid. The islanding mode is not permitted nowadays due to the different interconnection challenges. In the future, this attractive function is expected to be integrated. Different studies are dedicated to this mode [25],[26],[PAPRE-I] The main idea is to connect few interface inverters in parallel that operate normally in the grid connected mode, for instance a CSI. But in the case of the islanding mode, one of the inverters starts to operate as a synchronous generator (VSI) and sets frequency and voltage based on the load demand. The droop control seems a reasonable solution for such systems.

As a conclusion, the residential PV inverter should be able to perform the following tasks [1]:

- Provide the Volt/Freq control;
- Correct work at the grid disturbance;
- Provide protection function;
- Provide the stability of the system;
- Provide the continuity of the service;

- Provide the interaction with the system [27].

From Table 2.1 it is clear that the PECs have different critical points in different countries. This means that the industrial PEC should be able to adapt for different countries by changing its critical points.

Table 2.1 – Measured efficiencies and duty cycle values

Country/Standard	Parameter	tmin	tmax	Trip value
Estonia (IEC 50438)	Over voltage	- 0.1 s	3 s 0.2 s	230 V+10% 230 V+15%
Spain (IEC 50438)		- -	1.5 s 0.2 s	230 V+10% 230 V+15%
Denmark (IEC 50438)		0.1 s 39 s	0.2 s 40 s	230 V+13% 230 V+10%
IEEE 1547		- -	1 s 0.16 s	240 V+10% 240 V+20%
Estonia (IEC 50438)	Under voltage	1.2 s	1.5 s	230 V-15%
Spain (IEC 50438)		-	1.5 s	230 V-15%
Denmark (IEC 50438)		9 s	10 s	230 V-10%
IEEE 1547		- -	0.16 s 2 s	240 V-50% 240 V-12%
Estonia (IEC 50438)	Over frequency	0.3 s	0.5 s	52 Hz
Spain (IEC 50438)		-	0.5 s	50.5 Hz
Denmark		0.1 s	0.2 s	52 Hz
IEEE 1547		-	0.16 s	60.5 Hz
Estonia (IEC 50438)	Under frequency	0.3 s	0.5 s	47.5 Hz
Spain (IEC 50438)		-	3 s	48 Hz
Denmark (IEC 50438)		0.1 s	0.2 s	47.5 Hz
IEEE 1547		-	0.16 s	57 Hz

2.2 Overview of different control strategies

Originally, most of the control techniques were developed for motor drives [28]-[31] and have been applied for grid-connected inverters with minor change of the names: Field Oriented Control (FOC) became Voltage Oriented Control (VOC), Direct Torque Control (DTC) became Direct Power Control (DPC), where the torque and the stator flux were replaced with an active and a reactive power of the grid-connected inverter [32], [28]. The main features of both control methods remained the same. Namely, the VOC

is tightly related to the use of coordinate transformations for grid currents and voltages (abc to αβ, αβ to dq) and additional current control loop that provides fast transient response and high static performance [32]- [34]. The block diagrams of the different control methods are presented in Figures 2.4, 2.5.

The DPC eliminates the current control loop, the conducting state of the converter's switches is defined based on the instantaneous values of the grid voltage space vector and the active and reactive power demand. This control method requires the higher sampling frequency and inherits the variable switching frequency, contrary to the VOC. As a result, DPC requires higher inductances and has a potential problem of the LCL filter resonance [35], [4].

The structure of the common inverter control scheme usually consists of two loops – the outer voltage control loop with slow dynamics responsible for the energy flow between the dc-link and the grid by generating the reference value for the current loop; and the inner current control loop with a fast dynamic responsible for the quality of the current waveform, the current protection. The implementation of the particular control structure depends on the reference frame that is divided into three groups: natural frame (abc), rotating frame (αβ) and synchronous reference frame (dq). The DPC performs the control of the active and reactive power directly and it has no Pulse Width Modulation (PWM) blocks opposite to the VOC methods. Typically, the DPC includes the Hysteresis control or Space Vector Modulation (SVM) or Space Vector Pulse Width Modulation (SPVWM) block with a voltage look up table. Table 2.2 presents the classification of the main current controllers. The PR controller provides theoretically infinite gain at the tuning frequency, which means that the steady state error is minimized. It can operate in the abc reference frame or in the αβ reference frame, which means that there is no need to perform the transformation in comparison to the Proportional Integer (PI)[36] controller that requires the transformation of the reference frame, because it operates in the dq reference frame and it is more suitable to control the dc quantities. Proportional Resonant (PR) controller has a fixed switching frequency that makes this controller more attractive for application than the hysteresis controller although there are hysteresis controllers with fixed switching frequency [37]-[39]. The predictive deadbeat controller [40]-[42] has the following disadvantage: it is a delay that occurs due to the reference value of the next sample that will be known at the end of the modulation period. The MPD [43]-[47] inherits the unpredictable THD of the produced current that makes it complicated to design an output filter. The application of the PR controllers connected in parallel or Harmonic Compensation (HC) circuit [48]-[50] allows the control of the undesired order harmonics in the produced current even if the grid is distorted. The negative aspect of the PR controller can be related to its operating frequency, i.e., if the frequency of the grid is distorted, the performance of the PR controller could be significantly deteriorated. Different types of modulation techniques are described in [51].

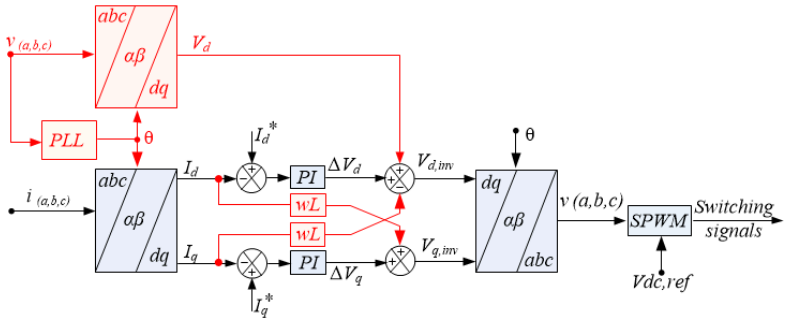


Figure 2.4 Voltage oriented control based on the PI controller.

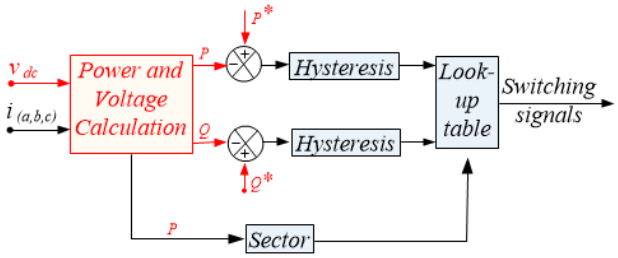


Figure 2.5 Direct power control.

Table 2.2 – Classification of the control methods

Control methods		**Type of the controller**					
		PR	PID	RC	Hysteresis	MPC	DBC
Method	VOC	*	*	*	*	*	*
	DPC				*	*	*
Reference frame	abc	*		*	*	*	*
	αβ	*		*	*	*	*
	dq		*		*	*	*
Linearity	Linear	*	*	*		*	*
	Non-linear				*	*	*
Number of loops	Single loop	*		*	*	*	*
	Multi-loops		*			*	*
Sensor	Sensor	*	*	*	*	*	*
	sensorless						*

2.3 Overview of power electronics transformer-less topologies

In [52], different configurations of PEC topologies for PV application are reviewed. The differences of the topology configurations depend on the following: with or without isolation step, internal or external MPPT block, power range, efficiency, with or without transformer, complexity of the design, with or without dc-dc converter. The transformer-less PV inverters with the dc-dc converter are described in [53], [54] and without dc-dc converter in [55]-[57].

All the proposed transformer-less topologies, in general, can be expressed through two block diagrams, Figure 2.6a,b.

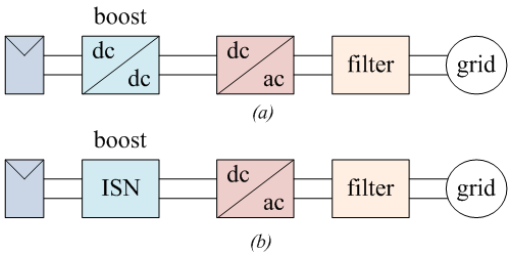


Figure 2.6 Block diagram of the grid connected inverters; traditional approach (a), novel approach (b).

The traditional approach, with the dc-dc converter, is widely used in the industry, Figure 2.6a. The dc-dc boost converter is used there to increase the PV voltage and to convert a Direct Current (dc) power into Alternative Current (ac), the full-bridge inverter is used. In 2002, Peng was the first to propose ISN, Z-source network, which allows regulation of the input voltage in a wide range, provides shoot-through (ST) immunity and allows combining two power conversation steps into one.

Figures 2.7 a,b show two topologies of the PEC. The first topology, Figure 2.7a, shows the traditional concept with some modification and the second, Figure 2.7b, shows the novel concept that is based on the Z-source network.

The topology in Figure 2.7a looks attractive due to the three-level voltage Vab that leads to the improved quality of the produced current. This topology provides low input voltage regulation range due to the low boost factor B=1/(1-Ds) [58] in comparison to the ISN based converters. The topology in Figure 2.7b presents a novel approach based on the Z-source network. Since this topology consists of the Z-source network, it changes the input current discontinuous, i.e., the efficiency of the PVs is worse than that of the ISN, which provides CIC.

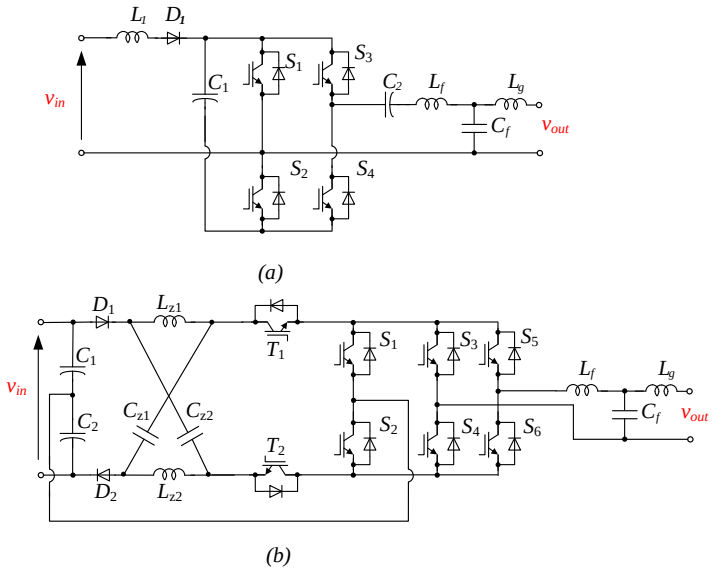


Figure 2.7 A single-phase boost inverter with common ground for photovoltaic application [58] (a), Single-phase Z-source three-level inverter [59] (b).

2.4 Summary of Chapter 2

High penetration level of the RES to the DGS led to the revision of the standards for the grid-connected converters. Based on the new accepted functions the PEC now is considered as AND. The same standard has different critical points for different High penetration level of the RES to the DGS led to the revision of the standards for the grid-connected converters. Based on the new accepted functions, now the PEC is considered as AND. The same standard has different critical points for different countries, which means that the industrial converter should be able to integrate to the country where it is going to be located.

The control methods were introduced to power electronics from the motor drive theory with minor modification. The decision about the applied controllers is usually based on the power capacity of the control system, reference frame and the precision, knowing of the behavior of the system.

Researchers today show high interest in the opportunity to apply the PEC based on the ISN in the industry. The reason is that the ISN allows overcoming a set of limitations that the traditional dc-dc boost converter has, such as: ST duty cycle intolerance, low input voltage regulation range. The ISN allows combining two power conversion steps into one. At the same time, not all of the proposed ISN are suitable for residential PV applications due to the DIC that they provide.

Chapter 3
Impedance-Source Based Inverter with Storage Integration

This chapter addresses the string PV inverter topology. In the analysis, two new possible topologies of the string PV inverter for residential application will be considered. The traditional VSI requires an additional boost stage, the dc-dc boost converter, which would increase the time varying input voltage up to the required level in order to ensure the right direction of the power flow. Moreover, the traditional VSI requires integrating the dead time between switching of the transistor switches; in the opposite case, the ST state may occur, which is dangerous for the traditional VSI because unlimited currents start to flow through the ST circuit [16].

Chapter 1 presented a novel approach based on the ISN, which allows preventing some limitations of the traditional VSI. As stated above, not all ISNs are suitable for PV application while some ISN are. The Quasi-Z-Source Network (qZSN) is one of them. It provides Continuous Input Current (CIC) and is able to regulate the input voltage in a wide range; qZSN provides ST immunity that makes the control strategy simpler because there is no need to introduce dead-time.

For further consideration, the topologies based on the qZSN were selected.

3.1 Novel quazi-z-source derived inverter with unfolding circuit and battery storage integration

Firstly, a novel Quasi-Z-Source (qZS) derived inverter with unfolding circuit and battery storage integration was designed and investigated [PAPER-I] (Figure 3.1).The topology consists of the following components:

- qZS network *(L_1, L_2, C_1, C_2)* to boost the input voltage;
- BIC*(T_1, T_2, L_b, C_b, Bat)* to maintain the virtual dc-link voltage and to control the battery power flow;
- intermediate switching device S_0, which commutates under a non-fixed and a high switching frequency; the S_0 forms positive half-waves of the output signal;
- inverter circuit *(S_1-S_4)* commutates under a low switching frequency and it forms the positive/negative waveforms of a sinusoidal output current;
- output circuit (*Cout*, *Lout*, *Rout*).

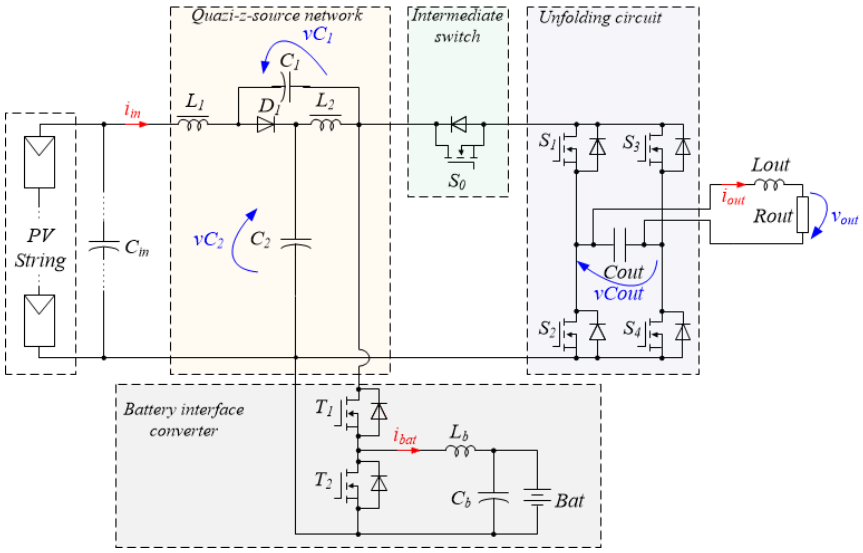


Figure 3.1 Quasi-z-source derived inverter with unfolding circuit and battery storage integration [PAPER-I].

Inverters based on the unfolding circuit [61]-[64] are attractive for their switching frequency of the inverter switches that equals to the line frequency, as a result, the switching losses of the inverter switches are negligible. At the same time, the unfolding circuits are known well to their produced shape of the voltage and current, which have some distortion near zero. It is caused by the uncertain state of the inverter's switches when the voltage reaches zero voltage.

Operation principle and steady state analysis

The operation principle basically can be divided into two operation modes: the formation of the positive half wave of the output signal and the negative. The difference between

these two modes is in the switching states of the inverter switches, which commutate each half period. The time intervals within the modes are symmetrical and for that reason, the consideration of only one of the operation modes is enough. Figure 3.2 shows the operation principle of the formation of the positive half wave of the output signal of the qZS derived inverter with unfolding circuit and battery storage integration.

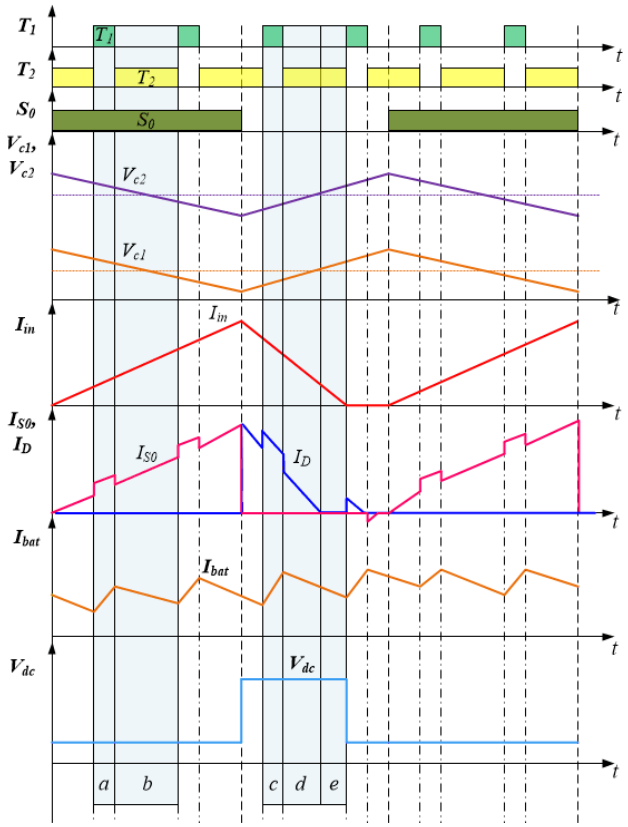


Figure 3.2 Control principles and idealized operating waveforms of the proposed converter in steady state mode.

The switches S1, S4 are conducting within the whole half part of the grid period to form the positive half wave of the output signal. The intermediate switch S0 is responsible for the formation of the sinusoidal shape of the grid current.

The interval a in Figure 3.2 shows the time when the switch S0 is conducting, the impedance capacitors are discharging and transferring their energy to the impedances' coupled inductors, and as a result, the dc-link voltage is increasing. The switch T1 is turned on and the battery is charging, the current's spike across the intermediate switch

is due to the battery's current being added. For this mode, equations of voltages and currents can be presented as follows:

$$v_{L1} = v_{Cout} - v_{C1} - V_{in},\ v_{L2} = v_{Cout} - v_{C2}. \tag{3.1}$$

$$i_{in} + i_{C2} = i_{bat} + i_{S0},\ i_{Cout} + i_{out} = i_{S0}. \tag{3.2}$$

The interval *b* in Figure 3.2 shows the time when the instantaneous voltage across capacitor C_2 is becoming lower than the predefined value; the battery starts to discharge, which means that T_2 is turned on, and T_1 is turned off.

The interval *c* in Figure 3.2 shows the interval when the switch S_0 is turned off. The impedance diode starts to conduct, and the impedance capacitors and the battery are charging. The current across the output capacitor *C* changes its direction, while keeping the direction across the output circuit *L, R*. Although the switches *S1, S4* are turned on, the current across them equals zero.

$$v_{L1} = v_{C2} - V_{in},\ v_{L2} = v_{C1}. \tag{3.3}$$

$$i_{in} + i_{C1} = i_{C2},\ i_{Cout} = i_{out}. \tag{3.4}$$

The interval *d* in Figure 3.2 shows the time when the switch S_0 is turned off, and the impedance diode keeps operating, and the battery is discharging.

The interval *e* in Figure 3.2 shows the time when neither of the switching devices S_0 nor D_1 are conducting and the current flows across the output circuit in the same direction as in the previous operation mode. In the Continuous Current Mode (CCM), the last mode is absent.

In a steady state mode, the average voltage across the inductors is equal to zero. Equations (5-7) 'minus' correspond to the positive part of the output voltage and 'plus' to the negative. The average voltage across the capacitors can be expressed as follows:

$$V_{C1} = \frac{Da(V_{in} \pm V_{Cout})}{1 - 2Da}, \tag{3.5}$$

$$V_{C2} = \frac{V_{in} - Da(V_{in} \pm V_{Cout})}{1 - 2Da}. \tag{3.6}$$

Where Da=t_a/T is a relative time when the intermediate switch is being turned on. The required duty cycle of the switching state of the switch S0 can be calculated as:

$$Da = \frac{V_{dc} - V_{in}}{2V_{dc} \pm 2V_{Cout}}. \qquad (3.7)$$

Where $Vdc = V_{C1} + V_{C2}$ is the desired level of the dc-link voltage.

Closed loop system description

Different types of the control strategies are applied in order to control the whole system, Figure 3.3*a-d*. To control the dc-link voltage, the voltage across impedance capacitors C_2, C_3 is controlled by the buffer circuit, Figure 3.3*a*. To control the buffer circuit, the SPWM block is applied, Figure 3.3*b*.

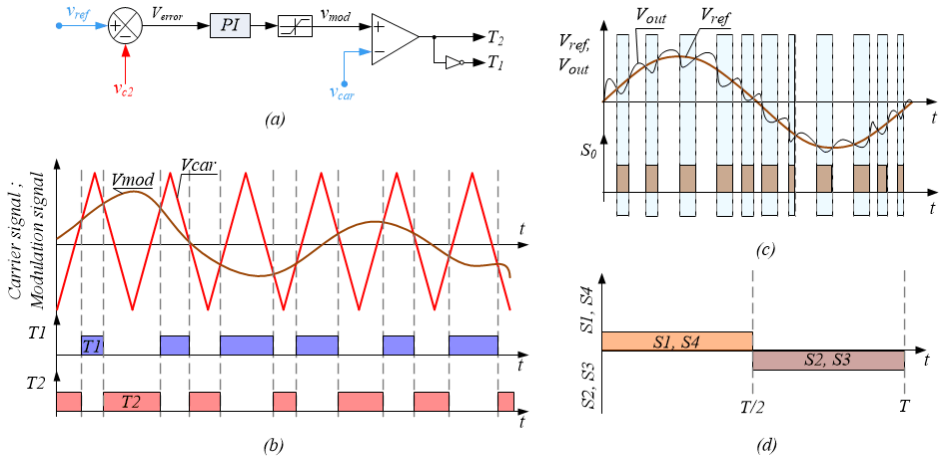


Figure 3.3 The control strategy applied (a); control signals of the modulation techniques applied to the buffer circuit (b); hysteresis control approach for an intermediate modulation switch (c); control signals of the unfolding circuit (d).

To control the output voltage, the hysteresis controller is selected where the reference output voltage is compared with the measured output voltage and on the basis of that error, the intermediate switch is controlled, Figure 3.3*c*. To control the unfolding circuit, a simplified PWM block is applied, Figure 3.3*d*.

3.2 Single-phase three-level quasi-z-source neutral-point-clamped inverter with battery storage integration

Another topology is a single-phase three-level quasi-z-source neutral-point-clamped inverter proposed in 2012 by Power Electronics Group from Tallinn University of Technology [65] (Figure 3.4), but only open loop mode was investigated.

The circuit consists of the following components:

- symmetrical quazi-z-source network *(L_1, L_2, C_1, C_2, D_1, L_3, L_4, C_4, C_3, D_2)* to boost the input voltage;
- three-level inverter circuit, each leg consisting of two complementary switching pairs and four anti-parallel diodes *(S_1-S_8. D_{01}-D_{04})*.

The advantages of this topology are: continuous input current, ST immunity, reduced switching losses, and balanced neutral-point voltage in contrast to the traditional two-level VSI.

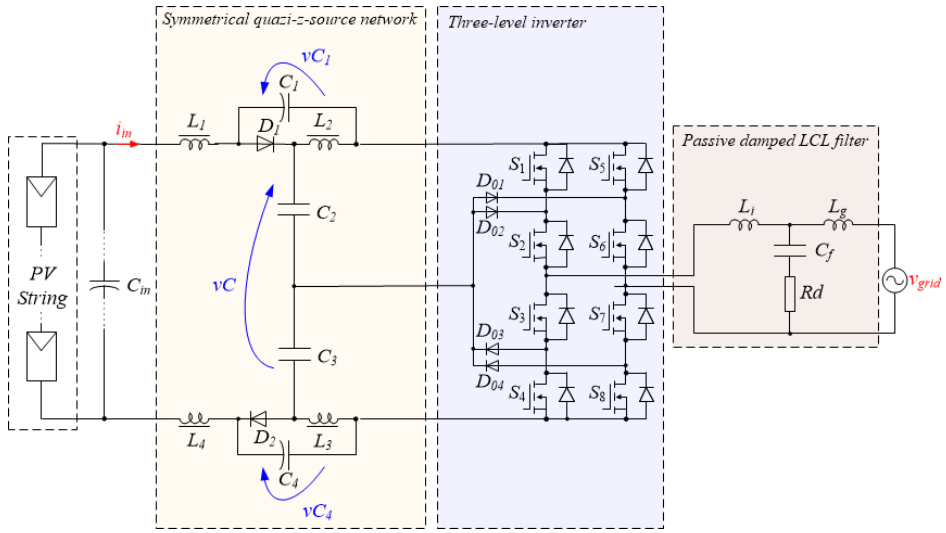


Figure 3.4 Single-phase three-level quazi-z-source neutral-point-clamped inverter.

According to studies in [65], the proposed topology can operate in eight operation modes, some of which are repeated and only the switching state of the transistors or diodes is changed; therefore, in general, the proposed topology can operate in three operation modes: active state, zero state and ST state. The modulation technique is described in [66].

Operation principle of three-level NPC qZSI

The combination of the active states, zero states and ST states allows us to control the dc-link voltage by increasing the input voltage up to a desired level of the dc-link when it is required.

The link between the anti-parallel diodes and two impedance capacitors C_2C_3 denoted as NPC allows reduction of the voltage stress on the switching devices twice. The reduction of the required blocking voltage capability of the inverter switches allows us to use the switching devices with an increased switching frequency. The combination of the produced three-level voltage and the increased switching frequency allows reduction of the size of the output filter and improvement of the THD of the grid current. Also, NPC allows us to use either the separate or single source in the input side. The single source is simpler to use because then the problems that may occur in the case of non-identical input sources are removed.

The CCM of the input current is the desired mode especially for PV applications, but this mode depends on the balance between the input and the output power. In order to ensure the CCM of the input current, all possible scenarios of the operation modes should be taken into consideration at the designing step.

Figure 3.5 shows the equivalent schemes in the different time intervals.

The modes *a,b,c* operate during the formation of the positive grid current and *d,e,c* during the negative. The idealized operating waveforms of the proposed converter in the steady state mode and during the CCM of the input current are presented in Figure 3.6.

The interval *a* corresponds to the conventional active state. The energy flows from the input to the grid.

$$v_{L1} = v_{L3} = \frac{V_{in} - v_C}{2};\ v_{L2} = v_{L4} = -v_{C1} = -v_{C4};\ v_{C2} = v_{C3}, \quad (3.7)$$

$$i_{L1} + i_{C1} - i_{L2} - i_{C2} = 0;\ i_{C3} - i_{L3} - i_{C4} + i_{L4} = 0;\ i_{L2} - i_{C1} - i_{ab} = 0. \quad (3.8)$$

The interval *b* is a zero state; during this interval, the impedance capacitors are storing energy.

$$v_{L1} = v_{L3} = \frac{V_{in} - v_C}{2};\ v_{L2} = v_{L4} = -v_{C1} = -v_{C4};\ v_{C2} = v_{C3}, \quad (3.9)$$

$$i_{L1} + i_{C1} - i_{L2} - i_{C2} = 0;\ i_{L4} + i_{C3} - i_{L3} - i_{C4} = 0. \quad (3.10)$$

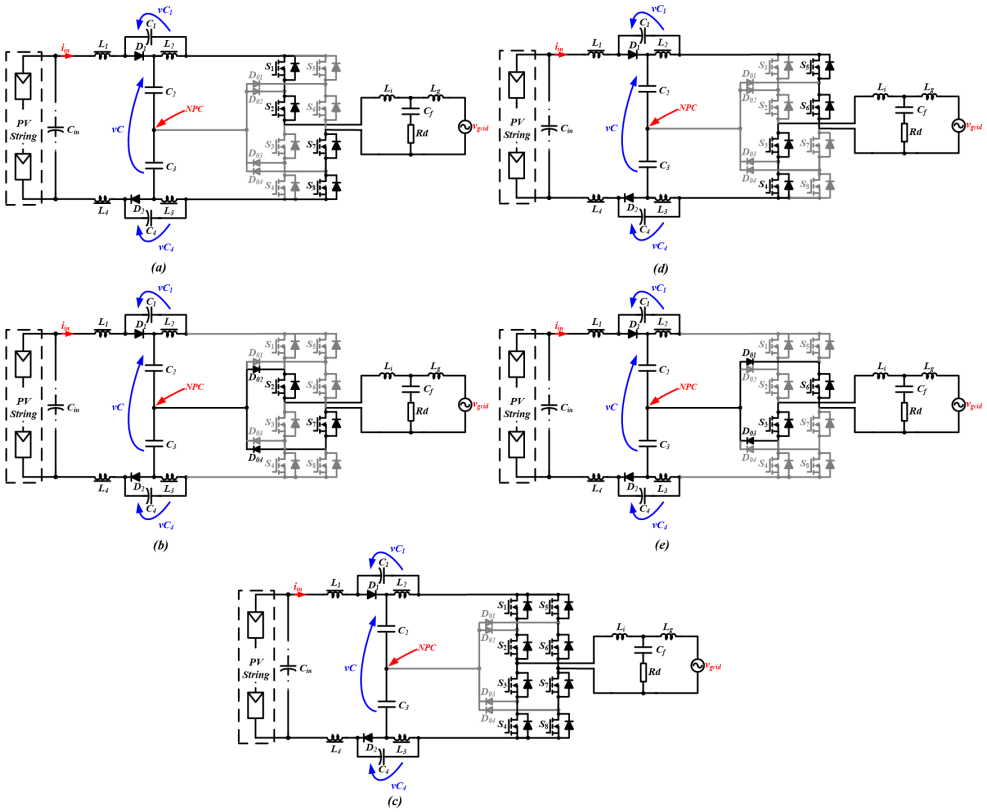


Figure 3.5 Equivalent schemes: active states (a,d), zero states (b,e) and ST state (c).

The interval *c* is ST state. During this mode, the energy that has been stored in the impedance capacitors at the previous step is transfered to the impedance inductors. In the next time interval *a*, the energy stored in the inductors will accumulate with the input energy and as a result, the voltage after impedance networks, virtual dc-link voltage, will be increased.

$$v_{L1} = v_{L3} = \frac{V_{in} + v_{C1} + v_{C4}}{2}\ ;\ v_{L2} = v_{L4} = v_{C2} = v_{C3}\,, \qquad (3.11)$$

$$i_{L1} + i_{C1} = i_{L3} + i_{C4} = 0\,; i_{L4} + i_{C3} = i_{L2} + i_{C2} = 0\,. \qquad (3.12)$$

The simulation results presented in [PAPER-III] show that the investigated topology is able to operate in a wide operation range of the input power; it can operate in a buck and in a boost mode and it is able to produce a grid current of the required quality.

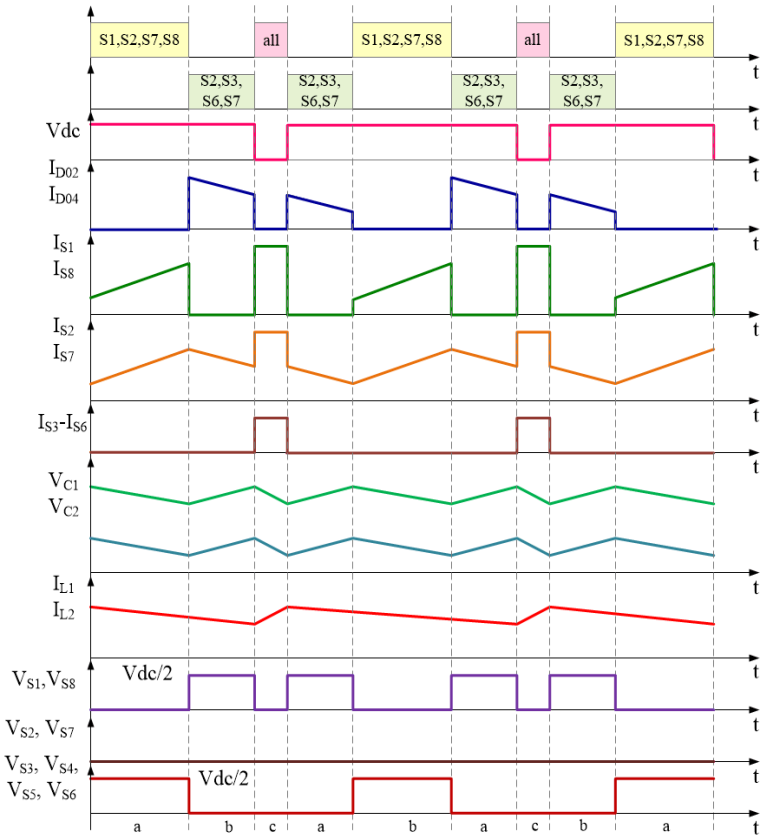


Figure 3.6 Control principle and idealized operating waveforms of the proposed converter in steady state mode.

Selected battery storage integration scenario in a quasi-Z-source inverter

The decentralized power plants require integration of the battery storage into the RESs in order to support the RES such as a PV system during low production period or even to provide the power if the input source is absent.

Two ways of connecting the battery to the impedance network are presented in [67] and [68]. In [69], a brief review of both of them and their negative aspects are discussed, and possible scenarios for solving some drawbacks are pointed out. The main drawback is

that the battery can only provide the power balance between the input and the output side in a limitation input voltage range, otherwise the operation mode moves from the CCM to the Discontinuous Current Mode (DCM). If the input voltage is absent, none of the discussed methods is able to provide the power to the load because of absence of a possibility to increase the battery power up to required level.

In order to overcome the discussed limitation, the storage interface converter was chosen to integrate the battery into the studied topology in Figure 3.7. Because this configuration allows utilizing of the battery even if the input source is absent. In this case, the topology can be represented (Figure 3.8), where the PVs are presented as a diode. On the left side, the dc-dc boost converter is connected to the battery. Thanks to the transistors T1 and T2, the battery power can be increased up to required level, while the ST immunity of the system is kept.

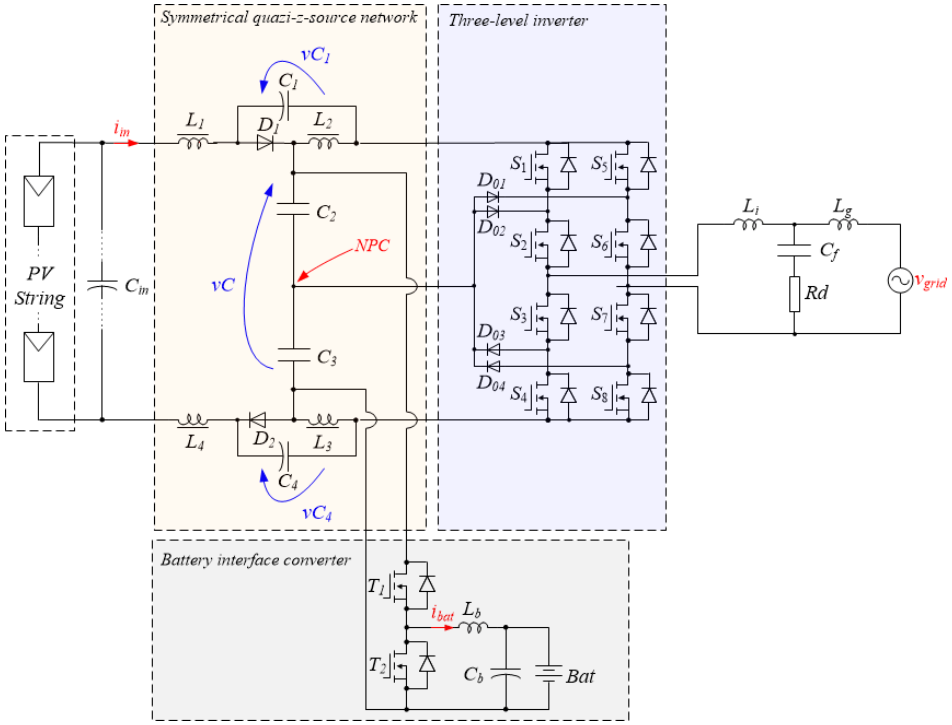


Figure 3.7 Single-phase three-level quazi-z-source neutral-point-clamped inverter with BIC.

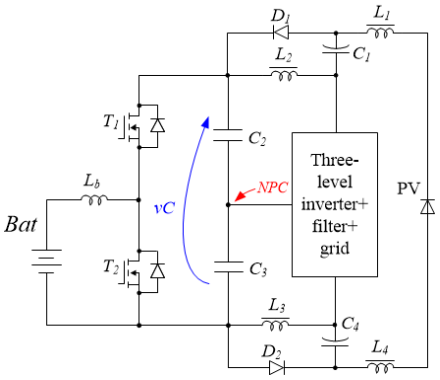


Figure 3.8 The single-phase three-level NPC qZSI with interface storage integration during the absence of the input source.

3.3 Simulation verification of the considered solutions

Figure 3.9 shows the simulation results of two considered topologies. The P_{grid} was 3 kVA in both cases. In [PAPER-I] it is shown that the qZSI based on the unfolding circuit and battery storage integration can operate only in a boost mode.

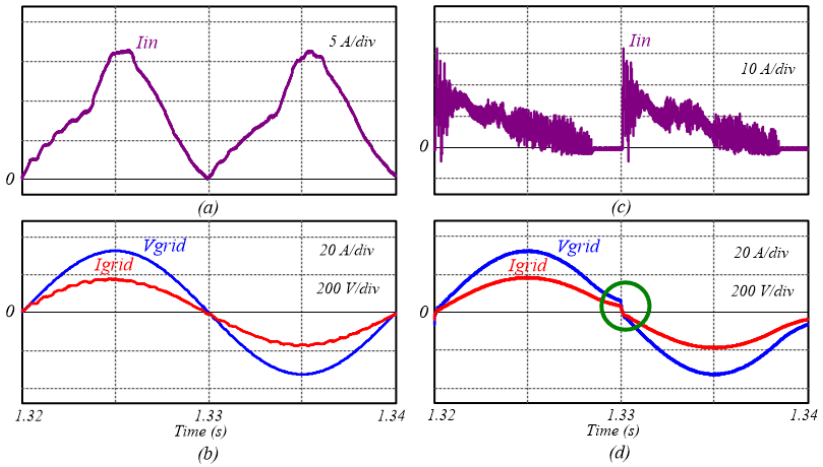


Figure 3.9 Simulation results: single-phase three-level quazi-z-source neutral-point-clamped inverter with BIC (a,b); quazi-z-source derived inverter with unfolding circuit and BIC(c,d).

The simulation results were performed when the Vin was equal to 360 V for the three-level NPC qZSI and 100 V for the qZSI based on the unfolding circuit and battery storage

integration. Those values were considered as nominal values for the topologies. All the others parameters were the same for both topologies.

Figure 3.9*a,b* shows that the produced grid current and input current have better waveforms. The grid current in Figure 3.9*d* has some distortion near zero, which is a common problem of any unfolding circuit due to the uncertain state of the intermediate switch when the voltage before the unfolding circuit and the voltage across the unfolding capacitor are crossing zero point. The waveform of the grid current in Figure 3.9*c* is worse than that in Figure 3.9*a*, which results in a deteriorated performance of the MPPT, and it probably would be more complex to mitigate the ripple of the current in an unfolding circuit application.

Taking into account all the points discussed above, the three-level NPC qZSI looks more suitable for PV applications. The advantages of this topology are: it can operate without battery storage; it provides better results of the grid current and the input current; it can operate in a buck and in a boost mode. The control strategy of the energy storage circuit in this topology is independent of the control strategy of the main circuit that improves the reliability of the system. For those reasons, the three-level NPC qZSI was selected for future consideration.

3.4 Summary of Chapter 3

In this chapter, two topologies of PEC were considered in order to define the final topology for further consideration. The main requirements to the topology are: CIC, wide regulation of input voltage, quality of the produced current. The first topology, the qZSI inverter with unfolding circuit, was proposed by the author during her PhD study program. The second topology, single-phase three-level NPC qZSI, was proposed by Power Electronics Group from Tallinn University of Technology. The comparison between these two topologies has shown that the second topology is more suitable for residential PV applications because in terms of the main requirements, it provides better results than the first topology.

Since this work focuses on the PEC for residential PV applications, it is required to integrate the energy storage into the system. In this chapter, the storage interface converter was proposed. The proposed storage interface converter is able to provide the power balance between the input and output sides; moreover, it is able to provide the power even when the input source is absent during the night period.

Chapter 4

Hardware and Software Design of the Grid-Connected QZSI with Battery Storage Integration

This chapter is dedicated to the hardware and software design of the grid-connected qZSI with battery storage integration. In particular, two power decoupling approaches used to filter the DFR component of input power are addressed. The tuning up process of the dPR controller with the HC circuit used to control the grid current along with the tuning up process of the Proportional Integer Derivative (PID) controller used to control the voltage across impedance capacitors C2 and C3 are presented. Finally, the battery interface conversion will be considered to provide both the power balance and filtering of the DFR component of input power.

The main task of any regulator is to ensure the stability of the system along with providing quality parameters. The residential PV inverters should inject into the grid the current of the required quality, based on the standard EN61000-3-2, the THD should be lower than 5%. In order to control the output current, different types of controllers can be applied. In Chapter 2, it was shown that it is a good solution to regulate ac quantity by the PR with HC circuit due to the ability to control the undesired low order harmonics that can be present in a grid voltage. Since the input voltage is a time-varying component, it is required to use a voltage controller to regulate the voltage across capacitors C2 and C3. Since we are dealing with a single-phase inverter, the input power has a DFR component, which affects the MPPT performance. In order to improve the efficiency the MPPT, different filtering methods can be applied.

4.1 Double-frequency ripple elimination strategy for qZSI

The common problem of single-phase inverters is the DFR of the input power. The grid power consists of two components: the grid voltage and the grid current, which change according to the sinusoidal law with the line frequency. As a result, the grid power has not only an average value, but also the DFR. The grid voltage and grid current are assumed to be in phase:

$$V_g(t) = V_{g\_max}\sin(\omega t),\ I_g(t) = I_{g\_max}\sin(\omega t), \tag{4.1}$$

$$P_g(t) = V_g(t)I_g(t) = \frac{1}{2}V_g(t)I_g(t) - \frac{1}{2}V_g(t)I_g(t)\cos(2\omega t). \tag{4.2}$$

These DFRs are transferred into the input side from the output side [70], [71], deteriorating the efficiency of the PV system. In order to mitigate the DFR of the input power, the filtering systems of the DFR are applied where the ripple component of the power flows across the storage element by passing the input side of the main circuit. As a result, the input power has minimum power pulsation that allows using the storage battery in the input side. Traditionally, to reduce the DFR, the input capacitor is applied. This decision needs no auxiliary components, nor changes in the control strategy [72]. But the required capacitance and voltage are high enough, therefore, for this purpose, an Electrolytic Capacitor (E-cap) is applied. The E-cap is a weak part of the system despite the highest energy density and the lowest price per Joule because of the low ratings of ripple current and the high value of the Equivalent Series Resistors (ESRs), which leads to the heating up of the E-cap, therefore its size is limited. The leakage current due to the electromechanical reaction of the oxide layer reduces the lifetime of the E-cap [73]-[75].

There are two types of filtering methods: APD [76]-[87] that has an additional active component(s) and PPD [88] that has an additional passive component(s) or can be realized just by means of the modified control strategy.

The integration of one of these methods allows attenuation of the DFR of the input power and reduction of the capacitance of the capacitor(s) used as a storage element; as a result, the metallized polypropylene film capacitor or the multi-layer ceramic capacitor can be used instead of the E-cap. Today's markets are offering these types of capacitors with lower energy density, lower field strength and higher price than the E-cap, but their size is smaller and they have better immunity to the leakage current, which improves the reliability of the system in general [74]-[91]. Naturally, every type of a capacitor has its own specific advantages and disadvantages that should be taken into consideration at the design step, such as the operation mode, the environment, the voltage stress, the current ripple, the operation frequency. Further, the APD and the PPD will be compared.

Comparison of the active and passive decoupling approach for double-frequency power ripple cancellation

In order to compare the two approaches: active power decoupling and passive power decoupling, the following parameters can be applied. All energy is being stored in capacitors and inductors, because these parameters reflect the required dimension size of the corresponding components:

$$E_{LW} = \sum_{i=1}^{N_L} \frac{L_i I_{ave(i)}^2}{2}, \tag{4.3}$$

$$E_{CW} = \sum_{i=1}^{N_C} \frac{C_i V_{\max(i)}^2}{2}, \tag{4.4}$$

where N is the number of corresponding passive components.

Secondly, voltage stress on the transistors dictates the type of a switch to be selected from among those available on the market:

$$T_W = \sum_{i=1}^{N_T} V_{T(i)}, \tag{4.5}$$

where N_T is number of transistors.

It should be mentioned that all semiconductor devices are assumed to be of the same type for both cases. Also, switching losses will not be analyzed in detail because of its complexity. The switching losses are assumed to be proportional to the conduction losses. This assumption is quite realistic because switching frequency is the same for all semiconductors in both cases.

The size of the passive components is represented in the relative units (p.u.) in order to neglect the effect of input/output parameters on the final comparison, where

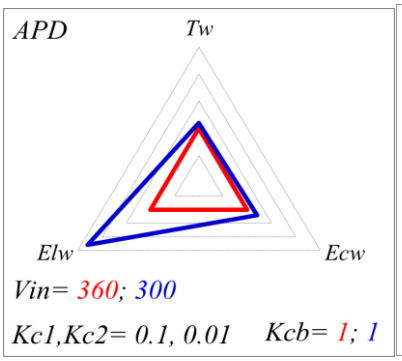
$$C_u = \frac{P_g T}{2\pi V_g^2}, \; L_u = \frac{V_C V_g T_{sw}}{12\pi P_g}. \tag{4.6}$$

Altogether the above parameters reflect the quality of the discussed approaches and give useful information for engineers at the stage of the selection and system design.

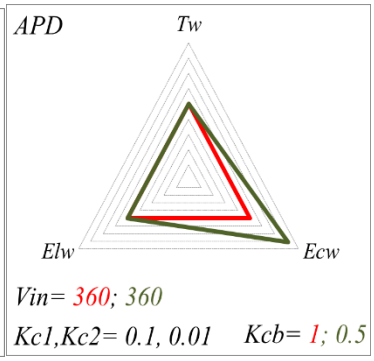
Table 4.1 – Main equations

	APD	**PPD**
C_1,C_4	$C_u \frac{2P_g T_{sw}}{K_{C1}(4V_C^2 - 4V_C V_{in} + V_{in}^2)}$	$C_u \frac{V_g^2(2-Kc1)}{K_{C1}(V_C^2 - 2V_C V_{in} + V_{in}^2)}$
C_2,C_3	$C_u \frac{2P_g T_{sw}(V_C - V_{in})}{K_{C2}V_C(4V_C^2 - 4V_C V_{in} + V_{in}^2)}$	$C_u \frac{V_g^2(2-K_{C2})}{K_{C2}V_C(V_C - V_{in})}$
C_B	$C_u \frac{V_g^2}{k^2 K_{C_B} V_C^2}$	-
L_1,L_3	$L_u \frac{6\pi V_{in}(V_C - V_{in})}{K_{L2}V_g(2V_C - V_{in})}$	$L_u \frac{6\pi V_{in}(V_C - V_{in})}{K_L V_g(2V_C V_{in})}$
L_2,L_4	$L_u \frac{3\pi V_{in}(V_C - V_{in})}{K_{L2}V_g(2V_C - V_{in})}$	$L_u \frac{6\pi V_{in}(V_C - V_{in})}{K_L V_g(2V_C V_{in})}$
L_B	$L_u \frac{12\pi k D_b V_C(k-1)}{K_{L_B} V_g}$	-
T_W	$8(V_{C1} + V_{C2}) + 2V_C$	$8(V_{C1\_max} + V_{C2\_max})$
E_{LW}	$C_1 V_{C1}^2 + C_2 V_{C2}^2 + \frac{C_B(1 + \frac{K_{CB}}{2})^2 V_{CB}^2}{2}$	$C_1(V_{C1\_max})^2 + C_2(V_{C2\_max})^2$
E_{CW}	$\frac{L_B I_B^2}{2} + L_1 I_{in}^2 + (2I_{in})^2 L_2$	$L_1 I_{in}^2 + L_2 I_{in}^2$

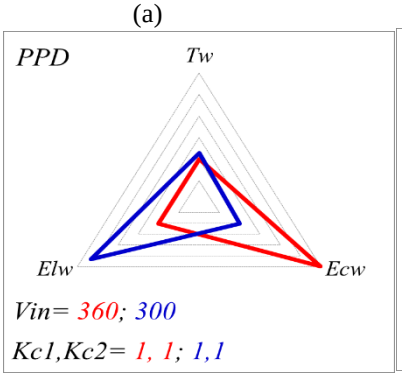
Figure 4.1 shows the diagrams of the energy stored in capacitors and inductors and total voltage stress on the semiconductor devices under different decoupling approaches, different input voltage and different voltage ripple coefficients.


APD
Tw
Elw
Ecw
Vin= 360; 300
Kc1,Kc2= 0.1, 0.01
Kcb= 1; 1

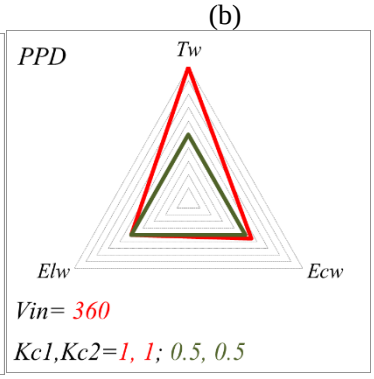
(a)


APD
Tw
Elw
Ecw
Vin= 360; 360
Kc1,Kc2= 0.1, 0.01
Kcb= 1; 0.5

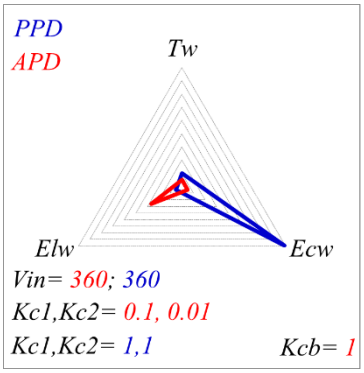
(b)


PPD
Tw
Elw
Ecw
Vin= 360; 300
Kc1,Kc2= 1, 1; 1,1

(c)


PPD
Tw
Elw
Ecw
Vin= 360
Kc1,Kc2=1, 1; 0.5, 0.5

(d)


PPD
APD
Tw
Elw
Ecw
Vin= 360; 360
Kc1,Kc2= 0.1, 0.01
Kc1,Kc2= 1,1
Kcb= 1

(e)

Figure 4.1 Diagrams for comparison of APD and PPD approaches.

Figure 4.1*a* shows the calculated parameters in the case of the APD approach with different input voltages. It can be seen that with the increase of the input voltage, the energy stored in capacitors and inductors is decreasing, and the total voltage stress on the semiconductor devices is decreasing as well. Figure 4.1*b* shows the calculated parameters in the case of the APD approach with different predefined voltage ripple factors of the buffer capacitor. The evident conclusion is that the energy stored in the capacitor is decreasing with the voltage ripple increasing.

Figure 4.1c shows the calculated parameters in the case of the PPD approach with different input voltages. It can be seen that with the increase of the input voltage, the energy stored in the capacitors is increasing, the energy stored in the inductors is decreasing, and the total voltage stress on the semiconductor devices is decreasing as well. Figure 4.1d shows the calculated parameters in the case of of the PPD approach with different predefined voltage ripple factors of the impedance capacitors. The conclusion is: the energy stored in the capacitors and the total voltage stress on the semiconductor devices are increasing with the voltage ripple increase.

Finally, Figure 4.1c shows the comparison of the results between the application of the APD and the PPD. According to the results, the energy stored in the capacitors and the total voltage stress on the semiconductor devices are higher in the case of the PPD while the energy stored in the inductors is lower.

Implementation of the active power decoupling approach for qZSI

The APD approach was implemented and investigated in PSCAD simulation program tools. Figure 4.2 shows the case study system [PAPER-IV]

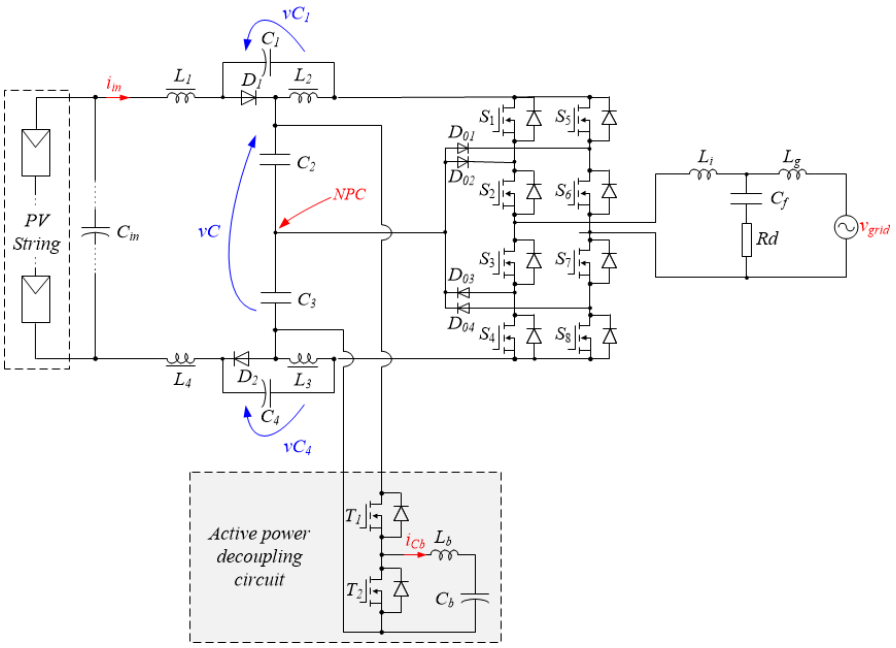


Figure 4.2 The single-phase three-level neutral-point clamped inverter with active power decoupling circuit.

Figure 4.3 shows the block diagram of the control strategy of the investigated topology.

To control the DFR of the input power, the dc-link voltage and/or input current can be under control. In the proposed control strategy, the dc-link voltage is maintained at the constant level by means of the PID controller, Figure 4.3a. Therefore, to mitigate the DFR of the input power, the DFR of the input current should be under control.

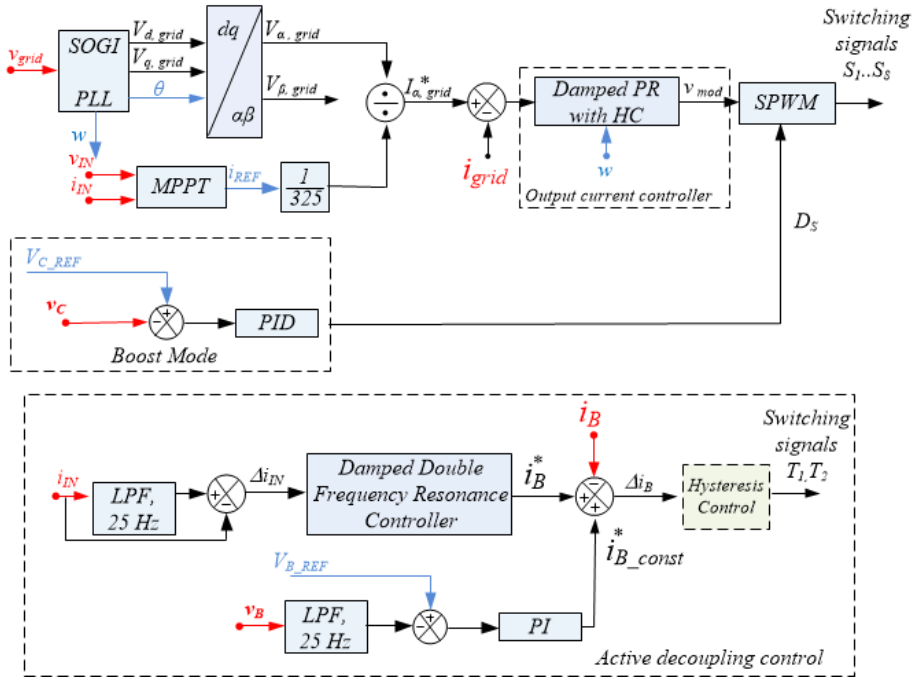


Figure 4.3 Block diagram of the control strategy of the single-phase three-level neutral-point-clamped inverter with the active power decoupling approach: (a) main circuit, (b) decoupling circuit.

In order to circulate the DFR of the input power through the auxiliary circuit, it is necessary to generate the reference decoupling current i_B^*. In the proposed configuration, it cannot be derived directly from the measured output power because of an additional phase shift that will be present due to the passive components of the qZSN. For that reason, the input current is used to obtain the i_B^* by means of the Damped Double Frequency Resonance (DDFR) controller, which highlights the ripples of the double frequency, Figure 4.3*b*.

In order to keep the predefined voltage across the capacitor C_B, it is necessary to form the constant current across the decoupling circuit $i_{B\_const}^*$; for that purpose, the PI controller is used.

Finally, the very simple hysteresis approach of the constant switching frequency is used in order to provide the reference value of the current. The error Δi_B between the reference value and the measured value of the current is applied to its input.

The strategy proposed is quite simple and requires no complex tuning. The Low Pass Filter (LPF) used for filtering the input current has 25 Hz cut-off frequency and can be easily realized in any digital system.

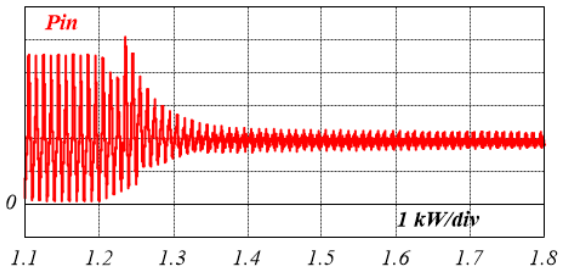


Figure 4.4 Simulation result: input power in the APD approach.

Figure 4.4 shows the input power ripples before and after the launch of the APD approach. The APD starts to operate at the time that equals 1.2 s. The input power ripples are equal to 100% without APD and 12.5% with APD.

Implementation of the passive power decoupling approach for qZSI

The PPD approach was also implemented and investigated in PSCAD simulation program tool. The considered PPD approach is in the modified control strategy. The main topology is depicted in Figure 4.2, but without buck type active power decoupling circuit.

The modified control strategy forms the time-varying ST signal to mitigate the DFR of the input power. The time-varying ST signal causes voltage change in the dc-link; thus, one of the aims is to limit the change in the dc-link voltage in the acceptable range [PAPER-V] Figure 4.5 shows the block diagram of the PPD control strategy.

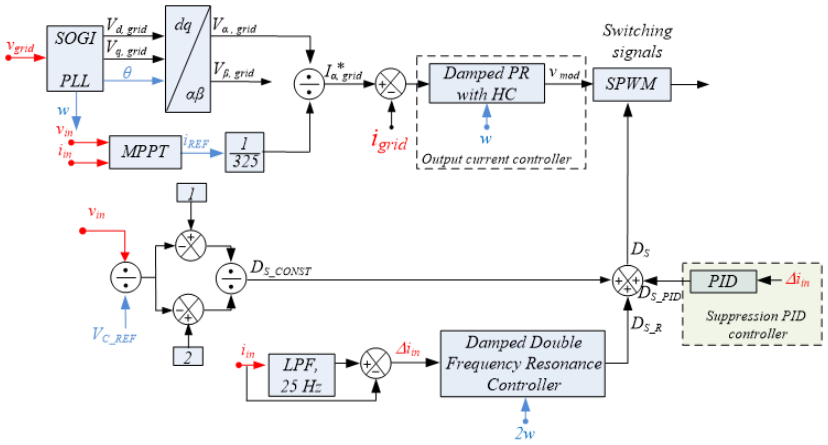


Figure 4.5 Block diagram of the single-phase three-level neutral-point-clamped inverter with the passive power decoupling approach.

The full ST duty cycle *Ds* consists of three components: the constant ST duty cycle *Ds_cons*, which depends on the input voltage and the desired average level of the dc-link voltage; the ST duty cycle, which is changed accordingly to the sinusoidal law with the double frequency relative to the grid frequency; and $Ds_{\_PID,}$ which is used to mitigate the high-frequency ripples of the input power.

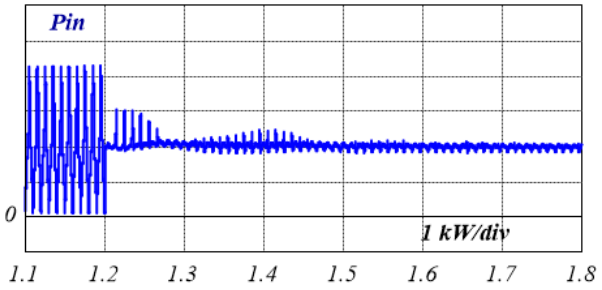


Figure 4.6 Simulation result: input power in the PPD approach.

Figure 4.6 shows the input power ripples before and after the launch of the PPD approach. The PPD starts to operate at the time when it equals 1.2 s. The input power ripples are equal to 100% without APD and 5.5% with PPD.

4.2 Grid-connected control strategy for qZSI with battery storage

The control strategy of the whole system can be divided into two main parts: first, a high speed current control loop that controls the quality of grid current, and second, a low speed voltage control loop that controls the dc-link voltage. Below, the output current control loop is discussed.

To control the quality of the output current in the application of the three-level neutral-point-clamped inverter, which allows an increase of the switching frequency of inverter's switches, thus improving the quality of the grid current, we apply a passive *d*LCL output filter with an dPR output controller.

Passive damped variant of an *LCL* filter was chosen because of the resistor, which is series connected to the filter capacitor and helps to smoothen the possible resonance oscillation, which may occur between *L* and *C* components; thus, it improves the stable-state of the system in comparison to a conventional *LCL* filter [96]. Passive *dLCL* filter was also chosen because of its third order filter, which attenuates the switching order harmonics in the grid current better than an *L* or *LC* filter and also an *dLCL* filter has smaller size than the other two [94], [95]. The main drawback of the application of the *LLCL* filter [97]-[99] is that this type of a filter attenuates the harmonics in a smaller range, near the switching frequency as compared to the *dLCL* filter. The design process of the LCL filter is presented in [100].

The dPR controller with phase compensation was selected since it has a wider frequency range under controlling in comparison to the PR controller [50], and provides the phase compensation caused by digital delay [101], [102].

Proportional-resonant controller design for grid-connected qZSI

In order to tune up the dPR transfer function of the output part, which consists of the dPR, HC circuit and dLCL were calculated[PAPER-VIII]. Figure 4.7 shows the block diagram of the output part. The main object is to achieve the stable state of the system in digital realization where the digital delay is:

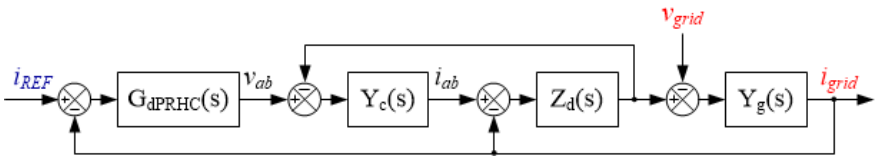


Figure 4.7 Control diagram of the grid current.

where $Y_c(s) = \frac{1}{sL_{fi} + R_{fi}}$, $Y_g(s) = \frac{1}{sL_{gi} + R_{gi}}$, $Z_d(s) = \frac{1}{sC_f} + R_d$, R_{fi} and R_{gi} are parasitic resistance, R_d is damped resistance.

The transfer function of the *dLCL* was calculated by Mason's Gain Rule:

$$G_{dLCL}(s) = \frac{Y_c(s)Z_d(s)Y_g(s)}{1 + Y_c(s)Z_d(s) + Z_d(s)Y_g(s)}. \tag{4.7}$$

Figure 4.8 shows the dPR controller with phase compensation, where Kp is the proportional coefficient, Ki is the integer coefficient, h is order harmonic, ω_c is the cut-off frequency, ω is the angular frequency.

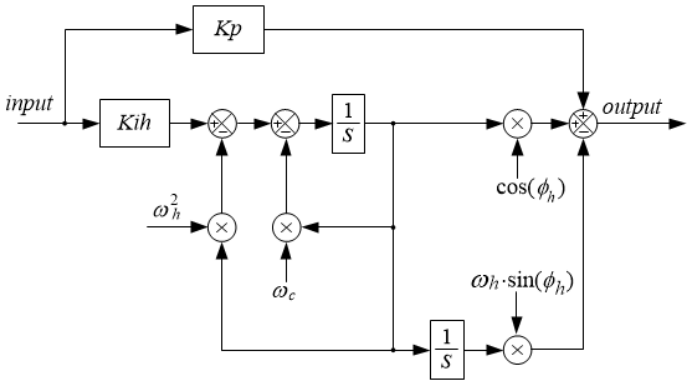


Figure 4.8 dPR controller with phase compensation.

The transfer function of the *dPR* controller with the *HC* circuit and phase compensation is:

$$G_{dPR}(s) = K_p + \sum_{h=1,3,5,7} K_{rh} \frac{s \cdot cos(\varphi_h) - \omega_h \cdot sin(\varphi_h)}{s^2 + 2\omega_{ch}s + \omega_h^2}, \tag{4.8}$$

$$\varphi_h = N \cdot 360^0 \cdot \frac{\omega_h}{2\pi} \cdot \frac{1}{f_s}, \tag{4.9}$$

where *N* is computational delay, *fs* is switching frequency.

Full closed loop transfer function is:

$$G_{dPRHCdLCL}(s) = \frac{dPRHC(s)\,dLCL(s)}{1 + dPRHC(s)\,dLCL(s)}. \tag{4.10}$$

Figure 4.9 shows the bode plot diagrams of $G_{dPRHCdLCL}(z)$. The transformation from s domain to z domain was performed by means of the Tustin with pre-wrapping discretization method.

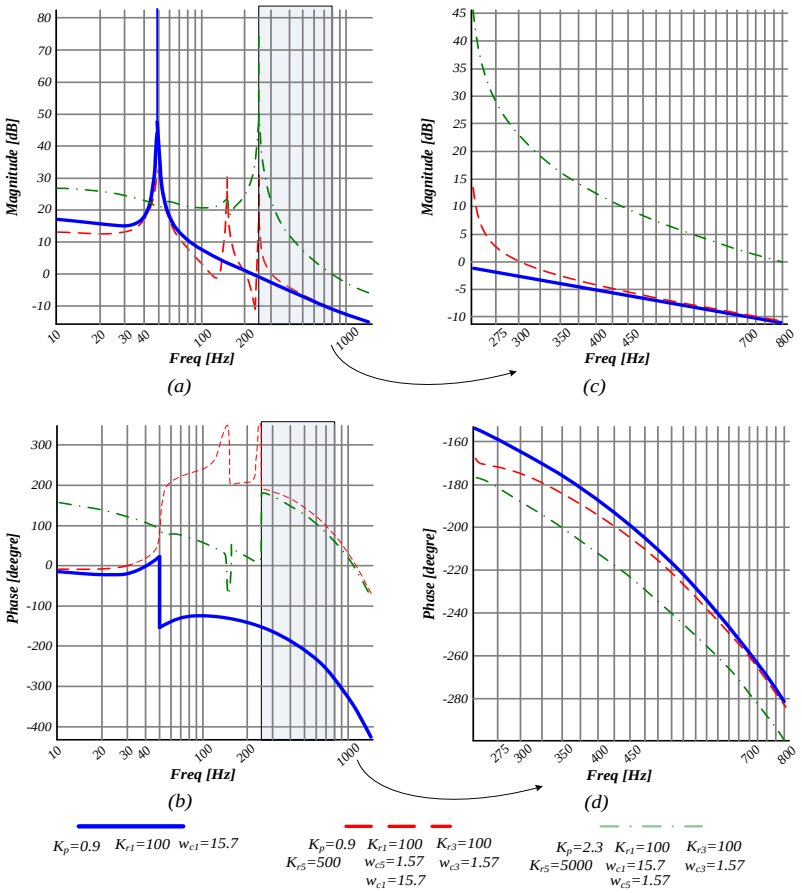


Figure 4.9 Bode plot diagrams of $G_{dPRdHCLCL}(z)$.

Figure 4.10 shows the simulation results of the single-phase three-level NPC qZSI connected to the grid. Figure 4.10a shows the simulation results with stable parameters of the dPR with HC circuit, which is marked as the red line in Figure 4.9. During startup, the grid current has some spikes that can launch the current protection function, which disconnects the PEC from the grid. Figure 10b shows the simulation results with unstable parameters, which are marked as the green line in Figure 4.9. During startup, the grid current has lower current spike compared to the stable parameters. The optimization of

the dPR with the HC circuit based on the combination of the unstable parameters and the stable parameter could allow smoothing the startup grid current value.

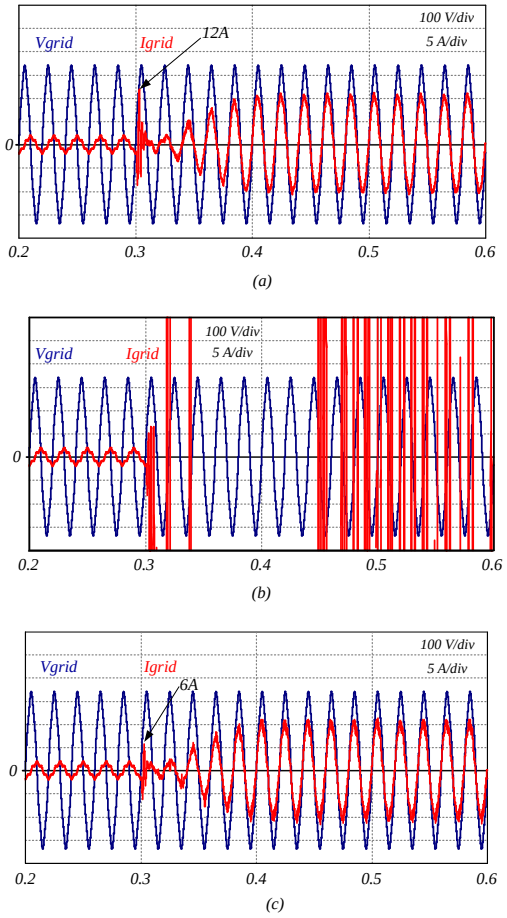


Figure 4.10 Simulation results: nominal PR controller parameters (a), increased PR controller parameters (b), increased controller parameters during starting up along with nominal parameters in steady state mode (c).

Figure 4.10c shows the results of the optimized dPR controller with the HC circuit. In the beginning, the parameters of the current controller were unstable and they were changed until the parameter became stable during 5 fundamental periods. It can be noticed that the startup grid current was smoothened, while the stability of the system remained the same.

PID controller design for qZS capacitor voltage control

As it was mentioned above, the control system of the main topology has two control loops. The tune up process of the PID controller that controls the dc-link voltage, the low speed loop, is presented here. Figure 4.11 shows the equivalent circuits of the qZSI with battery storage integration during the active and ST states.

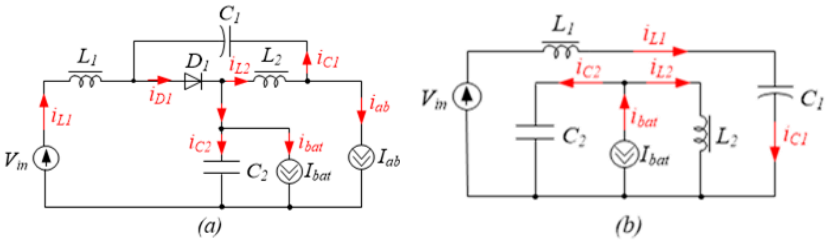


Figure 4.11 Equivalent circuits: active state (a); ST state (b).

To tune up the PID controller, the small signal models commonly used to analyze the dynamic behavior of the system of the qZSI were calculated, Figure 4.11.

In a steady-state mode, it is assumed that the Vin and Vab variables are constant.

The state equation of a system:

$$K\frac{dx(t)}{dt} = Ax(t) + Bu(t)\,; \tag{4.11}$$

$$y(t) = Cx(t) + Eu(t)\,. \tag{4.12}$$

where,

1) The inductor winding voltage and capacitor currents:

$$K = \begin{bmatrix} 2L & 0 & 0 & 0 & 0 & 0 \\ 0 & L & 0 & 0 & 0 & 0 \\ 0 & 0 & L & 0 & 0 & 0 \\ 0 & 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{C}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & C \end{bmatrix} \tag{4.13}$$

2) All of the state variables *x(t)* in the considered case are:

$$x(t) = [i_{in}; i_{L2}; i_{L4}; v_{C1}; v_C; v_{C4}]\,. \tag{4.14}$$

3) The independent inputs of the system are:

$$u(t) = \begin{bmatrix} Vin(t) \\ Vab(t) \end{bmatrix}; \tag{4.15}$$

4) Linear combination of the elements of the *x(t)* and *u(t)* are expressed as *y(t)*.

5) The constant of the proportionality is expressed through A,B,C,E.

The small signal state equations of the qZSI in the active state (D_a), Figure 4.13*a*, are:

$$\begin{cases} L\dfrac{di_{in}}{dt} = V_{in}(t) - 2R\cdot i_{in}(t); \\ L\dfrac{di_2}{dt} = \dfrac{vC(t)}{2} - R\cdot i_2(t); \\ L\dfrac{di_4}{dt} = \dfrac{vC(t)}{2} - R\cdot i_4(t); \\ C\dfrac{dvC_1}{dt} = -i_{in}(t); \\ C\dfrac{dvC}{2dt} = -i_2(t); \\ C\dfrac{dvC_4}{dt} = -i_{in}(t). \end{cases} \rightarrow A1 = \begin{bmatrix} -2R & 0 & 0 & 0 & 0 & 0 \\ 0 & -R & 0 & 0 & 1/2 & 0 \\ 0 & 0 & -R & 0 & 1/2 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \tag{4.16}$$

$$C=\begin{bmatrix}1&0&0&0&0&0\\0&0&0&0&1&0\end{bmatrix};\ B1=\begin{bmatrix}1&0\\0&0\\0&0\\0&0\\0&0\\0&0\end{bmatrix}. \tag{4.17}$$

The small signal state equations of the qZSI in the ST state *(D_s)*, Figure 4.13*b*, are:

$$\begin{cases} L\dfrac{di_{in}}{dt}=V_{in}(t)-vC(t)+2R\cdot i_{in}(t);\\ L\dfrac{di_2}{dt}=R\cdot i_2(t)-\dfrac{vC_1(t)}{2};\\ L\dfrac{di_4}{dt}=R\cdot i_4(t)-vC_4(t);\\ C\dfrac{dvC_1}{dt}=i_2(t)-i_{ab}(t);\\ C\dfrac{dvC}{2dt}=i_{in}(t)-i_{ab}(t);\\ C\dfrac{dvC_4}{dt}=i_4(t)-i_{ab}(t). \end{cases} \Rightarrow A2=\begin{bmatrix}2R&0&0&0&-1&0\\0&R&0&-1&0&0\\0&0&R&0&0&-1\\0&1&0&0&0&0\\1&0&0&0&0&0\\0&0&1&0&0&0\end{bmatrix}; \tag{4.18}$$

$$B2=\begin{bmatrix}1&0\\0&0\\0&0\\0&-1\\0&-1\\0&-1\end{bmatrix}. \tag{4.19}$$

The average signal state equations are expressed as:

$$\begin{cases} A_{av} = \dfrac{d_s(t)\big|_T}{2}(K^{-1}A_1) + \dfrac{d_a(t)\big|_T}{2}(K^{-1}A_2); \\ B_{av} = \dfrac{d_s(t)\big|_T}{2}(K^{-1}B_1) + \dfrac{d_a(t)\big|_T}{2}(K^{-1}B_2); \\ C_{av} = C. \end{cases} \tag{4.20}$$

where $d_s(t)+d_a(t)=1$.

The average state consists of the constant component and variable component:

$$\begin{cases} x(t)\big|_T = X + \hat{x}(t); u(t)\big|_T = U + \hat{u}(t); y(t)\big|_T = Y + \hat{y}(t); \\ d_s(t)\big|_T = D_s + \hat{d}(t); d_a(t)\big|_T = 1 - D_s - \hat{d}(t). \end{cases} \tag{4.12}$$

Based on Eqs. (4.15)-(4.21), Eq. (4.22) can be rewritten as:

$$K\frac{d}{dt}\hat{x} = A\hat{x} + B\hat{u} + [(K^{-1}A_1 - K^{-1}A_2)X + (K^{-1}B_1 - K^{-1}B_2)U]\cdot\hat{d}. \tag{4.22}$$

By applying the Laplace transformation to Eq. (4.23), the small signal model is derived:

$$\begin{cases} x(s) = (s\cdot I - A)^{-1}\cdot B\cdot\hat{u}(s) + (s\cdot I - A)^{-1}\cdot M\cdot\hat{d}(s); \\ M = (K^{-1}A_1 - K^{-1}A_2)X + (K^{-1}B_1 - K^{-1}B_2)U; \\ y(s) = C\cdot\hat{x}(s) = C(s\cdot I - A)^{-1}\cdot B\cdot\hat{u}(s) + C(s\cdot I - A)^{-1}\cdot M\cdot\hat{d}(s). \end{cases} \tag{4.23}$$

where I is diagonal matrix.

Finally, we obtain four transfer functions. The first couple of transfer functions express the dependence of the controlled parameters on the ST duty cycle variation. The second couple of the transfer functions express the dependence of the controlled parameters on the voltage variation.

$$\left[\begin{matrix} G_{id}(s) \\ G_{vd}(s) \end{matrix}\right]\Bigg|_{\hat{u}(s)=0} = C(s\cdot I - A)^{-1}\cdot M\,;\ \left[\begin{matrix} G_{iu}(s) \\ G_{vu}(s) \end{matrix}\right]\Bigg|_{\hat{d}(s)=0} = C(s\cdot I - A)^{-1}\cdot B. \quad (4.24)$$

The PID controller is used to control the dc-link voltage by changing the ST duty cycle; therefore, in order to tune up the PID controller, the following transfer function is considered:

$$G_{vd}(s) = C(s\cdot I - A)^{-1}\cdot M. \quad (4.25)$$

The transfer function of the PID controller is:

$$TrF_{PID} = K_p + \frac{1}{sK_i} + sK_{d.} \quad (4.26)$$

And the total transfer function of the whole system is:

$$TrF_{voltage} = G_{vd}(s)\cdot TrF_{PID}. \quad (4.27)$$

The transformation from the s domain to the z domain was performed by means of the backward discretization method. Figure 4.12 shows the bode plot diagram of the $TrF_{voltage}(z)$.

Figure 4.12 shows two different variants of the coefficients of the PID controller. The green line corresponds to the unstable state of the system, Figure 4.12*a,b*. The reduction of the coefficients allows achieving the stability of the system, the red line, Figure 4.12*c,d*.

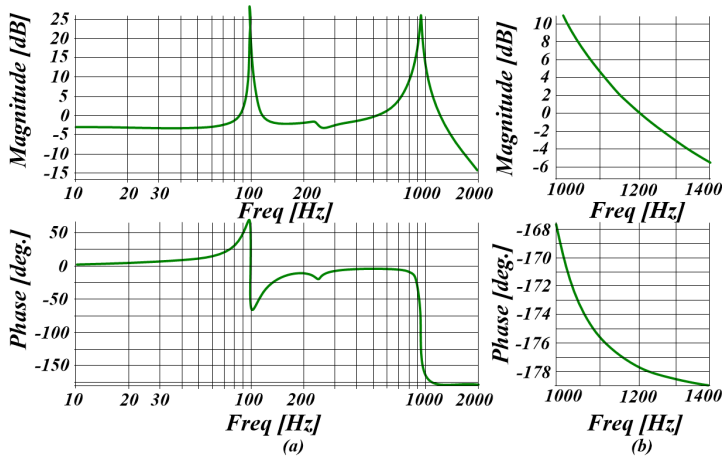


Figure 4.12 Bode plot diagram of the $TrF_{voltage}(z)$.

Battery storage control system design combined with the active decoupling approach

High penetration level of RES into DGS leads to energy fluctuation. For that reason, the integration of the energy storage into RES is a common requirement, which allows control of the power balance between the input and the output sides. In Section 3.2.3 it was shown that the integrating of the interface energy storage circuit into the considered topology is a good solution, because the system is able to provide power even if the input source is absent. Moreover, it is possible to combine the performance of two desired functions - the power balance and the APD - into one circuit, Chapter 3, Figure 3.9. The same idea is reported in [103] but their solution cannot provide power if the power of the input source is twice smaller from that of the nominal.

The proposed solution is presented in [PAPER-VI] where the investigated topology was considered under three different output power demands and it was shown that the active power decoupling circuit was able to provide the power balance and the mitigation of the DFR under different mentioned cases. Also, it is shown in [PAPER-VI] that the sampling frequency and digital delay could cause critical influence on the stability of the system. Figure 13 shows the topology of the single-phase three-level NPC qZSI with battery storage and Figure 14 presents the control strategy.

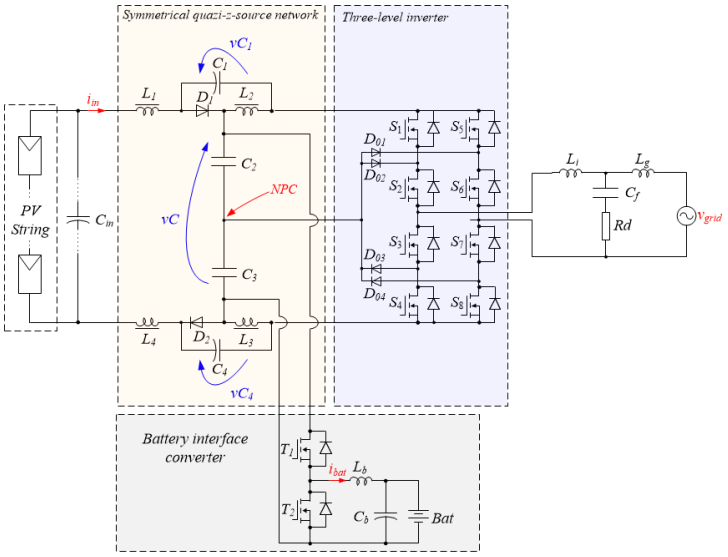


Figure 4.13 Single-phase three-level NPC qZSI with BIC.

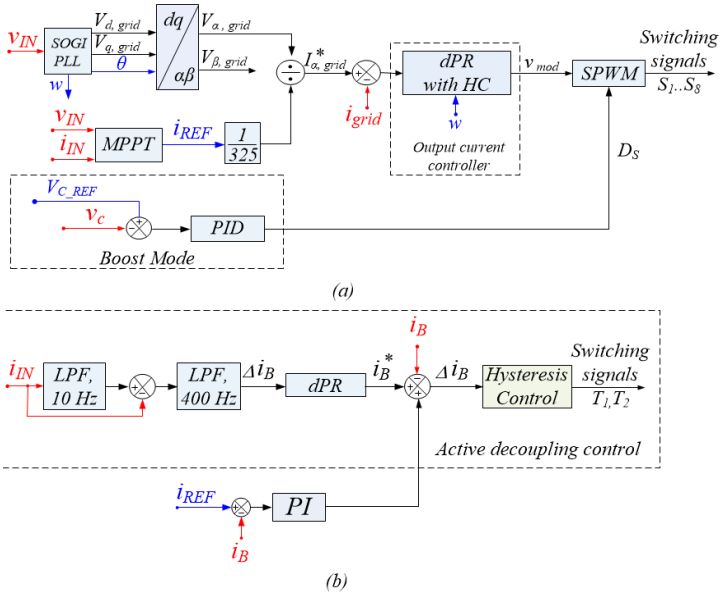


Figure 4.14 Control strategy of single-phase three-level NPC qZSI with BIC.

4.3 Summary of Chapter 4

This chapter has addressed hardware and software design approaches. First of all, two possible approaches how to mitigate the DFR of the input power were considered. Simulation results revealed that both approaches are able to cope with this task. Based on the comparative analyses, the APD is more preferable since it has two benefits: lower energy stored in capacitors and lower total voltage stress on the semiconductor devices, in comparison to the considered PPD. The APD circuit improves the efficiency the MPPT block along the reduction of the efficiency of the system by adding extra power losses caused in its circuit. The integration of the APD function into BIC allows compensation of the power losses caused by the operation of the battery circuit. At the same time, using an auxiliary circuit just for the APD function is not recommended. It may improve the overall power density, but deteriorate the efficiency and increase the cost. Such conclusions are in correlation with industrial string solar inverters where power decoupling is mostly realized by passive components.

Software optimization consists of the grid-connection and the dc-link control. The tuning up process of a current controller was presented. Based on the simulation results, the optimization of the start-up transients was proposed, which allows reduction of a current spike during start-up and avoiding the launch of the current protection function. Also, the tuning up process of the PID controller is presented based on the small signal model of the qZSI.

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Chapter 5
Application Example of qZSI with Battery Storage Integration

In this chapter, the experimental prototype of the single-phase three-level NPC qZSI with BIC will be tested under different conditions. The aim is to obtain the experimental results of the battery utilization, to test the different operation modes of the system (with MPPT, without MPPT) and to determine the CEC of the tested inverter.

5.1 Generalizations of the software and hardware design

The experimental prototype was built based on the scheme in Figure 5.1. Since one PV panel cannot produce the required level of power, there are different ways how to connect them for achieving the desired level of power. For residential application, the string PV system, which allows an increase of the voltage production, is widely used. For the selected topology, a PV installation of 10 series connected PV panels (Bisol BMU-255) is sufficient [104]. The voltage at the Maximum Power Point (MPP) under maximum solar irradiance is about 390 V, which corresponds to the back mode of the system. The boost mode is required during lower solar irradiance (bad weather, a fog etc.) and during partial shadowing. The partial shadowing mostly affects the current production but the reduction of current generation will affect the shifting of MPP and as a result, the voltage production. At low power production, the implementation of battery storage allows supporting the power grid by discharging it, or in an opposite case, by charging battery storage. In the considered case, the lead acid battery storage unit was used with nominal voltage 96 V and capacity about 7 Amp-hour. This choice is not an optimal solution because lead acid battery is sensitive to the current ripple, the LiFePO4 battery or Li4Ti5O12 would be more reasonable to use but their cost is much higher than that of the lead acid battery. To disconnect the PEC from the grid, two relays were integrated to the output side.

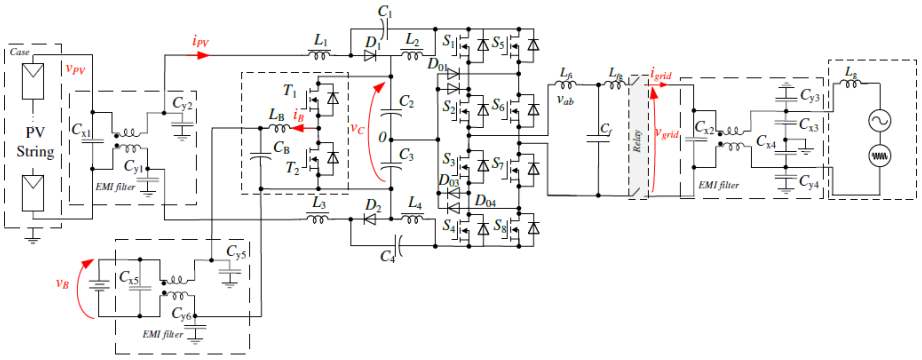


Figure 5.1 Single-phase three-level NPC qZSI with BIC.

In order to suppress the leakage current, two filtering approaches were used. To suppress common mode noise, the y capacitors were used. To suppress the differential mode noise, the x capacitors and coupled inductors were used.

Figure 5.2 shows the structure of the assembled prototype in a 3U box.

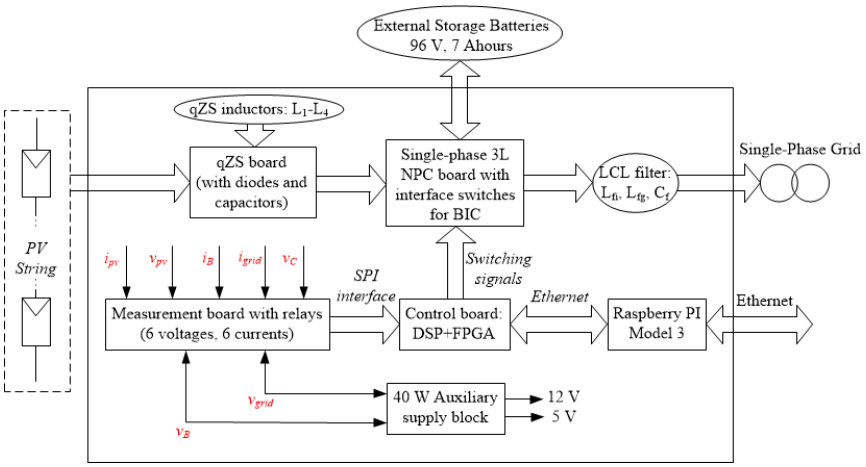


Figure 5.2The block structure of the study prototype.

It consists of four main PCB boards: power board, measurement board, control board (bottom board, top board) and external qZS inductors, storage inductors, inductors of output filters, and a battery. There is a possibility for intercommunication with other similar devices connected to the same grid through Ethernet connection. To provide remote control and energy management, the RPI3 board was used.

The measurement board consists of current sensors TLI4970 with digital output from Infineon and with simple resistor dividers as voltage sensors. For galvanic isolation, operational amplifiers ACPL-C87A and Analog-to-Digital Converters ADC LTC1864CS8 from Linear Technologies were used, which send data to the bottom control board through the SPI interface.

The Field Programmable Filed Array (FPGA) from Altera Cyclone IV EP4CE6E22C8 located on the bottom board was responsible for the communication between the measurement board and the top control board. The FPGA was also responsible for the formation of the switching signals for transistors. To provide the power immunity, the buffer SN74LVCC was used. It converted the voltage from 3.3 V on the FPGA side to 5 V on the outside.

The Digital Signal Processor (DSP) – STM32F417VG is located on the top board. This type of the DSP was selected because it has a 32 bit processor and a MAC controller that allows the implementation of Ethernet communication, SPI and one I2C interface and FPU. To provide the compatibility between MAC and Ethernet, the DP83848 was used.

The computational process was divided between DSP and FPGA in order to avoid additional outlay and fasten the computational process. Due to the FPGA a very high switching frequency of semiconductor devices is achievable. At the same time, computational frequency is limited, especially in a low cost control system applied for low power devices.

The remote control was realized by means of the RPI3 microcomputer with a standard micro - USB connector and Ethernet connection.

Each of these parts can work independently and communicate through SPI. Such combination provides an effective performance of any complex control.

5.2 Description of the experimental setup

Figure 5.3 shows the experimental prototype and Table 5.1 presents its parameters.

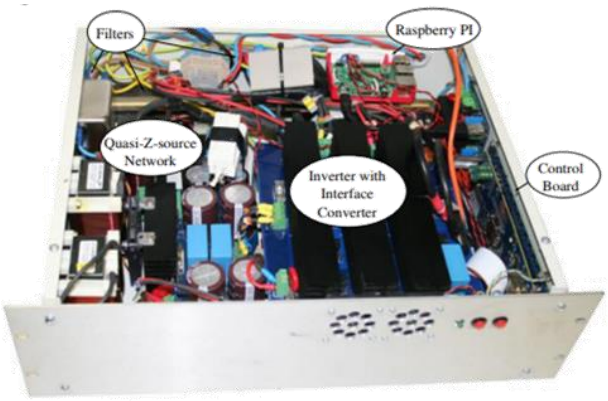


Figure 5.3 Experimental prototype.

Table 5.1 – Parameters of the prototype

Parameter	Value
Capacitances from capacitors C_1 and C_4	2.70 mF
Capacitances from capacitors C_2 and C_3	1.47 mF
Inductances from inductors L_1 and L_3	400 µH
Inductances from inductors L_2 and L_4	200 µH
1st filter inductance Li (inverter) – LCL	440 µH
Filter capacitance C_f – LCL	15.47 µF
2nd filter inductance Lg (grid) – LCL	220 µH
Switching frequency (MOSFET devices)	100 kHz
Sampling frequency (DAC and ADC converters)	8 kHz
Inverter transistors S1,…,S8	IPW65R041CFD
Storage interface transistors T1,...,T2	CMF20120D
NPC diodes and qZS diodes	C2M0080120D
MOSFETS drivers	ACPL-H342
AD converters	LTC1864CS8

5.3 qZSI with remote control for residential application

The qZSI with remote control was tested in the Laboratory of Power Electronics Group in Tallinn University of Technology and in Antwerp for the project horizon 2020 in cooperation with Ubik Solution. Further, the results obtained will be described.

Classical grid-connected mode with MPPT

The solar irradiance influences the MPP, Figure 5.4. With the reduction of solar irradiance, the MPP is reducing as well.

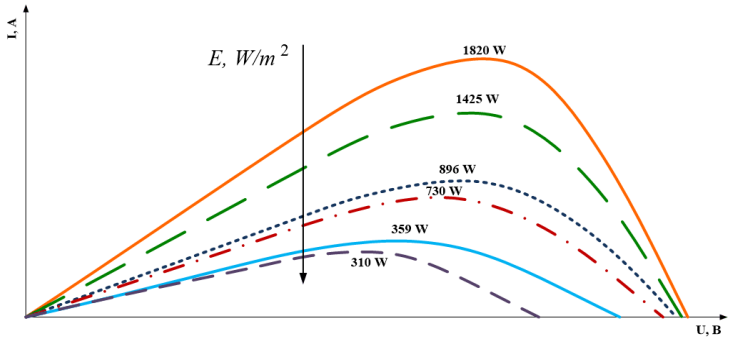


Figure 5.4 MPP under different solar irradiances.

Table 5.2 presents the experimental results of the efficiency of the PV system and the converter under different solar irradiations in %.

Table 5.2 – The experimental parameters under different solar irradiations.

№	I_{SC}	I_{MMP}	V_{OC}	V_{MMP}	E_{MMP}	E_{CONV}	$E_{\%}$
1	*1.2*	*1.1*	*350*	*280*	*94*	*90*	*10*
2	*1.25*	*1.15*	*390*	*310*	*95*	*92*	*20*
3	*2.2*	*2.1*	*440*	*340*	*92*	*96*	*30*
4	*2.6*	*2.5*	*450*	*350*	*97*	*96.2*	*50*
5	*4*	*3.9*	*455*	*355*	*98*	*96.4*	*75*
6	*5*	*4.9*	*460*	*360*	*99*	*96.5*	*100*

Table 5.2 shows that the efficiency of the MPPT is increasing with the increase of the solar irradiance. The reason is that the investigated system was tuned up to track the MPP at the maximum solar irradiance curve by means of P&O method [105]. Solar irradiance decreasing leads to smoother slope of the curve; therefore, it is more difficult to detect the MPP.

The efficiency of the tested converter was increasing with an increase of the solar irradiance. The parameters of the system were chosen to achieve the maximum efficiency at the maximum solar irradiance; therefore, at the reduction of the power, the power losses stay at the same value, which leads to the reduction of the efficiency of the converter. CEC coefficient of the PEC was calculated by the following equation [106]:

$$CEC = 0.04 \cdot Eff\,10\% + 0.05 \cdot Eff\,20\% + 0.12 \cdot Eff\,30\% + 0.21 \cdot Eff\,50\% + \\ +0.53 \cdot Eff\ 75\% + 0.05 \cdot Eff\,100\% \tag{5.1}$$

The full efficiency of the tested converter under different solar irradiances based on Eq. (5.1) is:

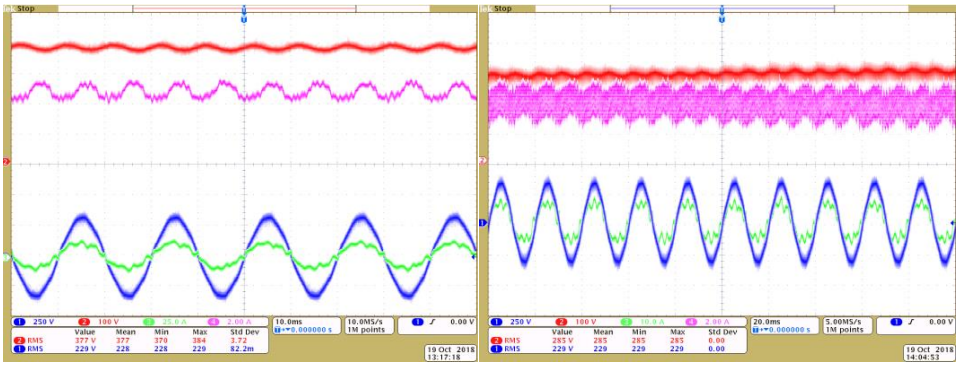
$$FullEffConv = 96\% \tag{5.2}$$

In order to estimate the CEC of the designed converter, it was tested at the nominal input power point under changing power load. Table 5.3 presents the experimental results.

Table 5.3 - Experimental parameters under different load power

№	V_{in}	P_{load}	E_{conv}
1	*360*	*360*	*96.4*
2	*360*	*720*	*96.9*
3	*360*	*1080*	*97.2*
4	*360*	*1800*	*97.6*
5	*360*	*2700*	*98*
6	*360*	*3600*	*97.2*

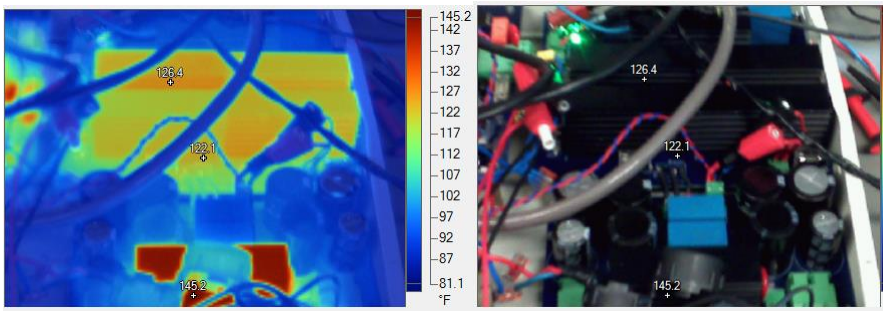
The CEC coefficient was calculated based on Eq. (5.1). The CEC of the tested PEC was 97.6%. Figures 5.5*a*,*b* show the experimental results of the output power equal to 1800 W and 900 W correspondingly. It can be noticed that the quality of the grid current was deteriorated because the low current is harder to control, especially when the current controller was tuned up to control the nominal grid current.



(a) *(b)*

Figure 5.5 Experimental results: input voltage and current, grid voltage and current.

Figure 5.6*a* shows that the heat distribution during the operation time corresponds to Figure 5.5.



(a) *(b)*

Figure 5.5 Experimental results of the thermos camera.

Figure 5.6*b* shows that most of the hot parts of the system were inverter switches and impedance diodes.

Reference active power supporting

Figure 5.7 shows the experimental results of the tested prototype to provide the opportunity for supporting the active power.

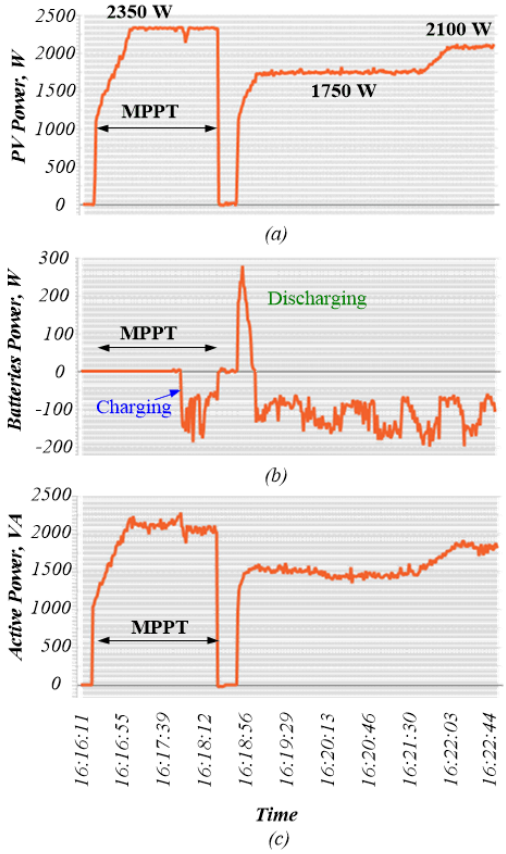


Figure 5.7 Experimental results: PV power (a), battery power (b), active power (c).

During the time intervals *a* and *b*, the system operated in the MPPT mode. During that time, the PV system was producing maximum of the possible power.

During the interval *b*, the battery was charging; as a result, the active power was reduced for the part that was equal to the charging power of battery.

During the interval *c*, the system was not working. At 16:18:40, the power production by the PV system was set 1750 W while the grid power demand was equal to 1500 VA,

interval *e*. Since the power produced by the PV system had some slope in order to fasten the transient process of transferring power to the grid, the battery was discharging during the time interval *d*. After that, the battery was charging. At time 16:21:32, the reference power produced by the PV system was changed to 2100 W while the grid power demand was 1750 VA, interval *f*.

Battery storage utilization for reference grid power supporting

The experimental prototype was tested for provision of power balance by utilization of the battery storage.

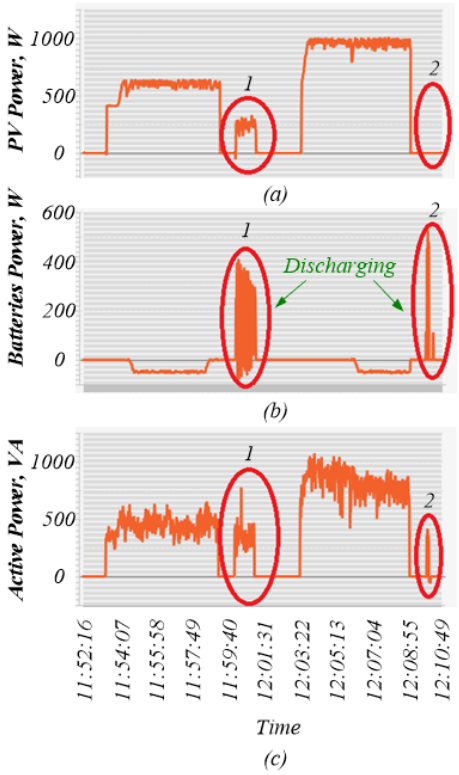


Figure 5.8 Experimental results: PV power (a), battery power (b), active power (c).

Figure 5.8 shows that during the time interval emphasized in circle *1*, the whole active power was received from the PV system and the battery, which means that the battery helps to achieve the power balance during the time when the PV power is insufficient for the grid. The time interval *2* shows the case when only the battery fed the power to the grid, the PV system produced no power. This finding confirms the theoretical and

simulation results that the proposed BIC was able to provide power at the absence of the input source.

5.4 Summary of Chapter 5

In this chapter presented the description of the built prototype of the qZSI with BIC and remote control. The full efficiency of the tested qZSI with BIC under different solar irradiances was 96%. The CEC was 97.6%. The experimental results showed that qZSI with BIC was able to operate in different modes (with MPPT and without MPPT) and it was capable of providing the power even if the input source (during night period) is absent. Based on the experimental results, the proposed topology can be applied for residential PV application.

Chapter 6
Conclusions and Future Works

6.1 Summary of key results

The main aim of the PhD thesis was to design the residential PV inverter with storage integration. The inverter based on the ISN was selected as a solution suitable for residential application with battery storage integration. The ISN based topologies allowed to combine two power conversion steps into one and to regulate input voltage in a wide range. Due to the ST immunity those topologies improve the reliability of the system.

The battery integration was a demanded part of the residential PV inverter. The comparison between APD and PPD approaches along with novel BIC were presented in this PhD thesis. The optimal solution was selected for industrial implementation.

As the main results of this thesis, the author claims the following:

- The single-phase three-level NPC qZSI with BIC was proven as a best solution among inverters with ISN networks. This solution provides CIC along with the low input current ripple and the required lower size of the passive components among other ISNs. Moreover three-level topology allow to use conventional Si MOSFET transistors with increased switching frequency which led to the improved quality of the power at the PCC and increased reliability due to the ST immunity.
- The comparison of APD and PPD approaches revealed that the considered APD required lower value of the capacitance; provide lower total voltage stress on the semiconductor devices, but required higher value of the inductance. At the same time integration of APD method was not recommended for industrial application due to the increased cost and additional power losses caused by the APD circuit. It was shown that for industrial application it would be more reasonable to apply a simple PPD approach based on the capacitor.

- The proposed novel topology with BIC allowed combining the performing two different functions at the same time: power balance and mitigation of the DFR of the input power. Moreover the proposed BIC was able to provide power even when the input source was absent.
- The control system for solar inverter with storage battery integration was designed and tuned. The novel tuning approach of the optimized dPR that allows avoiding triggering the current protection during start-up and providing stable operation despite on significant latency caused by control system was proposed.
- Finally the qZSI with the BIC and the remote control was built, and tasted in the laboratory of the Power Electronic Group in Tallinn University of Technology and in Antwerp for the project horizon 2020 in cooperation with Ubik Solution Company.

The experimental results of the built inverter demonstrated a full efficiency of 96%, and the CEC efficiency of 97.6% under different solar irradiance. The prototype could operate in different modes (with MPPT and without). The experimental results demonstrated that the built up qZSI with BIC can be applied for residential PV application.

6.2 Future work

Future work consists in using theoretical and practical thesis outcomes for further industrial implementation. Advanced research work must be conducted in the cost optimization and reliability assessment.

6.3 Resumen de resultados principales

El principal objetivo de esta tesis doctoral es diseñar un inversor PV residencial con almacenamiento integrado. El inversor basado en el ISN fue seleccionado como una solución adecuada para aplicaciones residenciales con integración de almacenamiento en baterías. Las topologías basadas en ISN permitieron combinar dos etapas de conversión de potencia en una sola y regular la tensión de entrada en una amplia gama de valores. Esta topología mejora la estabilidad del sistema debido a la inmunidad de ST. También se concluye que la integración de la batería es una parte imprescindible para el inversor PV residencial. Además, se ha propuesto la solución óptima para ser implementada en el sector industrial. También se expone una comparación entre APD y los nuevos enfoques de PPD.

Los principales resultados de esta tesis son los siguientes:

- El inversor de tres niveles NPC qZSI con BIC es la mejor solución de entre los inversores con redes ISN. Esta solución proporciona CIC junto con una baja corriente en alterna y una reducción del tamaño de los componentes pasivos de la red del ISN. Además, la topología de tres niveles permite utilizar transistores MOSFET de silicio con una mayor frecuencia de conmutación, con la consiguiente mejora de la calidad de la potencia en el PCC y el aumento de la fiabilidad debido a la inmunidad ST.
- La comparación de APD y de PPD reveló que APD requiere el menor valor de la capacidad posible: proporciona tensiones inferiores en los elementos semiconductores, en contraposición requiere el valor más alto de la inductancia. Al mismo tiempo la integración del método APD no se recomienda para la aplicación industrial debido al elevado coste y las pérdidas de potencia adicionales causadas por el recorrido APD. Se demostró que para la aplicación industrial sería más razonable aplicar un enfoque de PPD simple basado en condensadores.
- La nueva topología propuesta con BIC permite combinar dos funciones diferentes al mismo tiempo: equilibrio de potencia y mitigación del DFR de potencia en la entrada. Además, el BIC propuesto es capaz de proporcionar potencia aun cuando la fuente de energía no está disponible.
- El sistema de control del inversor solar con acumulador integrado se ha diseñado y calibrado correctamente. El nuevo proceso de sintonización optimizado de dPR evita la actuación de la protección de corriente durante el arranque y proporciona una operación estable a pesar de los tiempos de latencia del control.
- Finalmente, el qZSI con BIC se construyó y se provó en el laboratorio de Power Electronic Group en la universidad de Tallin de Tecnología y en Antwerp para el proyecto H2020 en cooperación con Ubik Solutions.

Los resultados experimentales del inversor construido demostraron que bajo diferentes niveles de irradiancia solar su eficacia es iguala al 96% y el CEC al 97,6%. Además, el prototipo podría funcionar en diferentes modos (con MPPT y sin MPPT). Los resultados experimentales demostraron que el qZSI con BIC propuesto se puede aplicar en instalaciones PV residenciales.

6.4 Trabajos futuros

Como trabajos futuros se propone utilizar los resultados teóricos y prácticos de la tesis para su aplicación industrial. Otra línea de investigación consistiría en optimizar el tamaño de los componentes pasivos. Además, se podría investigar como optimizar los costes y mejora de la fiabilidad de los dispositivos desarrollados.

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Appendix

The author´s publications directly connected to the topic of dissertation are added in this appendix, since they are considered as an extension or continuation of the thesis document. All of them are cited in the text.

[PAPER-I] J. Zakis, E. Makovenko, H. Zeng, O. Husev, L. Kutt, "qZSI as Synchro-nverter in Small Scaled Mico-Grid", *Elektronika ir Elektrotechnika (IF-1.088)*, pp.58-62, 2017.

[PAPER-II] E. Makovenko, O. Husev, D. Vinnikov, K. Tytelmaier, C. Roncero-Clemente, E. Romero-Cadaval, S. Bayhan, Y. Liu, "Novel quasi-Z-source derived inverter with unfolding circuit and battery storage", IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), pp. 1-6, 2018.

[PAPER-III] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, F. Blaabjerg, "Single-phase 3L PR controlled qZS inverter connected to the distorted grid", 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2016), pp. 234-239, 2016.

[PAPER-IV] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "Three-level single-phase quasi-Z source inverter with active power decoupling circuit", 18th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM), pp. 497-502, 2017.

[PAPER-V] E. Makovenko, O. Husev, J. Zakis, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "Passive power decoupling approach for three-level single-phase impedance Source Inverter based on resonant and PID controllers", 11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2017), pp. 516-521, 2017.

[PAPER-VI] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "A Single-Phase 3L qZS Inverter Connected to the Distorted Grid with Battery Storage and Active Power Decoupling Function", IEEE 59th International Scientific Conference on Power and

Electrical Engineering of Riga Technical University (RTUCON), pp. x-x, 2018.

[PAPER-VII] O. Husev, E. Makovenko, D. Vinnikov, T. Jalakas, C. Roncero-Clemente, E.Romero-Cadaval, J. F. Martins, V. Delgado-Gomes, V. Fernão Pires, "Single-phase qZS-based PV inverter with integrated battery storage for distributed energy generation", IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), pp. 1-6, 2018.

[PAPER-VIII] O. Husev, C. Roncero-Clemente, E. Makovenko, E. Romero-Cadaval, D. Vinnikov, "Optimization and Digital Implementation of the Proportional-Resonant Controller for Grid-Connected Inverter", *Transactions in Industrial Electronics (IF-7.05), pp X-X, Vol.*

Short Curriculum Vitae

1) Pesonal data

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2) Other names

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Last name Santasheva (end. Makovenko)

3) Professional employment

Period	Organization	Position
2013–2015	Novosibirsk State Technical University	Junior Researcher
2017–	Tallinn University of Technology	Early Stage Researcher

4) Education

Educational insitution	Graduation year	Education (field of study/degree)
Novosibirsk State Technical University	2012	Engineer in Industrial Electronics
Syanogorsk Lyceum No 7	2007	Secondary education

5) Honors and awards

Year	Description
2017	Best paper award at the annual international scientific conference on power and electrical engineering in the subsection of electrical engineering with article entitled: "Comparison of Traditional and Modified DQ Control Approach of Three-Phase Inverter", 12.10.17-14.10.17, Riga (Latvia)
2016	IES Student Paper Travel Awards, 10th International Conference on Compatibility, Power Electronics and Power Engineering, 29.06-01.07, Bydgoszcz (Poland)

6) Field of research:

Natural Sciences and Engineering; Electrical Engineering and Electronics

7) Projects

- PSG142 - Synthesis of output current waveforms of power electronic converters for increasing the hosting capacity of renewable energy sources in the distribution networks;
- PUT1443 - High-Performance Impedance-Source Converters;
- SF0140016s11 New Converter Topologies and Control Methods for Electronic Power Distribution Networks.

8) Publications

2019

Husev, O.; Roncero-Clemente, C.; Makovenko, E.; Pires Pimentel, S.; Vinnikov, D.; Martins, J. (2019). Optimization and Implementation of the Proportional-Resonant Controller for Grid-Connected Inverter with Significant Computation Delay. IEEE Transactions on Industrial Electronics.10.1109/TIE.2019.2898616 [forthcoming].

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Makovenko, E.; Husev, O.; Vinnikov, D.; Tytelmaier, K.; Roncero-Clemente, C.; Romero-Cadaval, E.; Bayhan, S.; Liu, Y. (2018). Novel quasi-Z-source derived inverter with unfolding circuit and battery storage. *12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018): 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), Doha, Qatar, 10-12 April 2018.* IEEE, 1−6.10.1109/CPE.2018.8372557.

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Makovenko, E.; Husev, O.; Zakis; J.; Roncero-Clemente, C.; Romero-Cadaval, E.; Vinnikov, D. (2017). Passive power decoupling approach for three-level single-phase impedance Source Inverter based on resonant and PID controllers. *11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG).* IEEE, 516−521.10.1109/CPE.2017.7915225.

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2016

Makovenko, E.; Husev, O.; Roncero-Clemente, R.; Romero-Cadaval, E.; Blaabjerg, F. (2016). Review of Novel Topologies for PV Applications. In: L. M. Camarinha-Matos, A. J. Falcão, N. Vafaei, S. Najdi (_EditorsAbbr). Technological Innovation for Cyber-Physical Systems (DOCEIS) (369−377). Springer International Publishing. (IFIP Advances in Information and Communication Technology; 470).10.1007/978-3-319-31165-4_35.

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Roncero-Sánchez, P.; Roncero-Clemente, C.; Romero-Cadaval, E.; Husev, O.; Makovenko, E. (2016). Control scheme of a Three-Phase Three-Level NPC qZ-Source inverter with LCL filter for RES applications. IEEE Industrial Electronics Magazine, 6540−6547.10.1109/IECON.2016.7793338.

2013

Makovenko, E. (2013). A Three-Phase Zero-Current-Transition and Quasi-Zero-Voltage-Transition Inverter/Rectifier with Reduced Stresses on Devices and Components. *14th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM).* IEEE EDM, 315−318.10.1109/EDM.2013.6642003.