Comparison of Impedance-Source Networks for Two and Multilevel Buck-Boost Inverter Applications

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Abstract **— Impedance-source networks are an increasingly popular solution in power converter applications, especially at single stage buck-boost power conversion to avoid additional front end dc-dc power converters. In the survey papers published, no analytical comparisons of different topologies have been described, which makes it difficult to choose the best option. Thus, the aim of this paper is to present a comprehensive analytical comparison of the impedance-source based buck-boost inverters in terms of passive component count and semiconductor stress. Based on the waveform of the input current, i.e. with or without a transformer, and with or without inductor coupling, the impedance-source converters are classified. The main criterion in our comprehensive comparison is the energy stored in the passive elements, which is considered both under constant and predefined high frequency current ripple in the inductors and the voltage ripple across the capacitors. Two-level and multilevel solutions are described. The conclusions provide a "one-stop" information source and a selection guide of impedance-source based buck-boost inverters for different applications.**

NOMENCLATURE

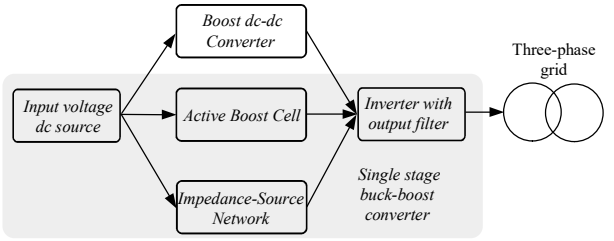
$L_{1, 2}$	inductances
L	relative unit of inductance
$C_{1, 2}$	capacitances
C	relative unit of capacitance
B	boost factor
T_S	switching period
M	modulation index
$K_{C1, 2}$	voltage ripple factors
$K_{L1, 2}$	current ripple factors
V_{IN}	input voltage
V_{PL}	peak line output voltage
$V_{DC1, 2}$	dc-link voltage
$V_{C1, 2}$	capacitor voltage
$V_{L1, 2}$	inductor voltage
ΔV_C	voltage ripple across capacitors
V_{BD}	blocking diode voltage
V_{BT}	blocking transistor voltage
P_{OUT}	output power
P_{IN}	input power
P	power
I_{IN}	input current
I_{AV}	average inductor current
$I_{L1, 2}$	inductors current
$\Delta I_{L1, 2}$	ripple inductors current
$S_{1, 2}$	active boost cell transistors
$T_{1, ..12}$	inverter transistors
$D_{01, 02}$	impedance-source diodes
$D_{1, 6}$	clamping diodes
Vol_L	volume of the inductor
Vol_C	volume of the capacitor
E_{LW}	summarized energy stored in the inductors
E_{CW}	summarized energy stored in the capacitors
D_W	summarized diodes voltage stress
T_W	summarized transistors voltage stress

I. INTRODUCTION

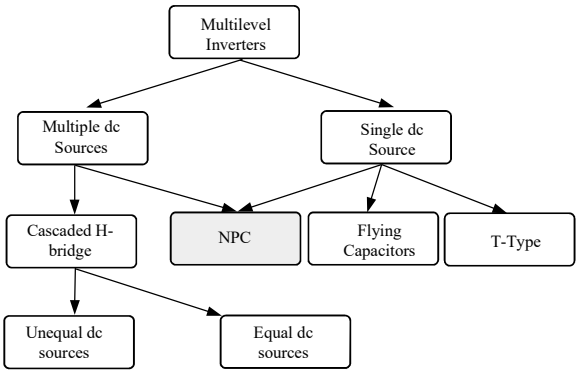
In recent years, renewable energy capacity has been growing rapidly. Renewable Energy Sources (RESs) supplied 16.7% of the world electrical energy consumption in 2010. By the end of 2014, the installed capacity of wind and solar PV power generation had reached 370 GW and 177 GW, correspondingly. The main challenge is the potentially distributed and inherently intermittent nature of these RESs [1]. A fuel cell, another promising renewable technology, is used, for instance, in boat supply systems, in power generation, sustainable transport as a hydrogen buffer [2]. These renewable technologies require power electronic systems for distributed energy harvesting and grid integration.

In PV systems, several configurations may be used. The string technology is a demanded solution where high efficiency of the PV system is required [3], [4]. One of the major drawbacks of the string technology is its poor energy utilization at partial shadowing. It leads to wide range input voltage variations. Traditionally, the Voltage Source Inverters (VSI) or Current Source Inverters (CSI) cannot provide more than twice higher input voltage regulation ratio. The main practical limitation lies in the low modulation index, which in turn leads to poor output current quality. Intermediate voltage boost dc-dc converters are used in order to overcome that drawback. At the same time, this solution is topologically more complex and harder to control because of the two-stage power conversion. Fig. 1*a* shows a generalized concept of the buck-boost dc-ac converter performance for a single input dc source.

The first solution, a two-stage energy conversion, is a traditional approach. The second and the third approach that are based on an intermediate Impedance-Source (IS) network or active boost cell are single-stage energy conversion solutions [5]-[10]. The buck-boost solutions based on an active boost cell are rare in industrial applications.



(a)



(b)

Fig. 1. General structure of the buck- inverter (a) along with simplified classification of the multilevel inverters (b).

Recent solutions based on the IS networks have been extended for various fields of application. Z-Source Inverters (ZSIs) and quasi-Z-Source Inverters (qZSIs) for grid integration into low voltage energy sources were proposed in [11], [12]. ZSIs overcome the limitation of the conventional grid-connected inverters: they have a buck, a boost mode and do not suffer from Shoot-Through (ST) states. ZSI and qZSI utilize the cross-conduction states to boost the input dc-voltage by switching on both the top and bottom switches of at least one inverter leg. This unique boosting technique improves inverter reliability. QZSIs are similar to the previously presented Z-source inverters. The main advantages of qZSI over ZSI are: lower source stress, reduced component ratings and a simple control method. qZSI drives continuous input current from the source and shares a common ground with a dc-source, which is suitable for RESs and other applications [13]-[26], in particular for the PV systems. These inverters are capable of performing Maximum Power Point Tracking (MPPT) with no need for an extra dc-dc converter. At the same time, the main drawback of the ZSI and qZSI lies in the low dc-link utilization under constant boost control [27]-[30]. In order to overcome the drawback, many IS derivations have been proposed [31]-[45]. References [46]-[49] present a good overview of existing solutions.

Another trend in power electronics is the modular and multilevel converter applications. Industry and academia are showing increased attention towards multilevel converters as one of the preferred choices of power electronic conversion for high-power applications. The reason is that they can achieve high power using mature medium-power semiconductor technology. Several review papers have presented good classifications and descriptions of the multilevel converters [50]-[53], for instance, many types of Multilevel Inverters (MLI) are covered in [50]. Fig. 1b shows a generalized simplified classification of the MLIs.

MLIs have advantages over conventional and very well-known two-level inverters. These advantages are: improved output quality and larger nominal power in the converter.

Multilevel converters are a good solution for low power and low voltage applications as well. Reduced voltage stress allows using fast MOSFET semiconductors among industrially verified Si technologies. In particular, Three-Level (3L) inverters have attracted increasing attention in industrial applications, such as motor drives [54], active filters [55], [56], and renewable energy systems [57]. The result is higher power quality, better electromagnetic compatibility, lower switching losses, and no need for a transformer at the distribution voltage level [58]-[60].

Based on [50], it can be concluded that the Neutral-Point-Clamped (NPC) inverter is the most attractive solution for industrial applications. The NPC inverter has become quite popular because of lower number of capacitors, particularly in the 3L case. Although the NPC structure can be extended to a higher number of levels, one of the drawbacks of the NPC inverter most frequently analyzed is the neutral point control or capacitor voltage balance. Among other characteristics, it depends on the modulation index, dynamic behavior, and load conditions, which produce a voltage difference between both capacitors, shifting the neutral point and causing undesirable distortion at the converter output [50]. It limits the number of levels in practical applications.

The Cascaded H-bridge (CHB) solution is well suited for high-power and high-level applications because of the modular structure that enables higher voltage operation with classic low-voltage semiconductors. The phase shifting of the carrier signals moves the frequency harmonics to the higher frequency side, and this, together with the high number of levels, enables a reduction of the average device switching frequency and lower losses. However, it requires a large number of isolated dc sources, which, for instance, could be realized in PV panels.

This paper contains a comprehensive analysis of the IS networks in terms of size and passive element count, amount and voltage level of required semiconductors for a single-stage inverter application. Two- and multilevel buck-boost inverters based on the already existing IS networks are compared. Next, the concept of our analysis and comparison is described. Section III reviews all the recent IS networks. Section IV describes already existing multilevel solutions based on IS networks. A comparative analysis of the topologies discussed is presented in section V and conclusions are given in section VI.

II. Component Design Guidelines

Despite numerous review [46]-[49] and comparison [61]-[67] papers about IS networks, many gaps still exist in the knowledge regarding these topologies. Several papers are devoted to the design of IS networks [15]-[17], [25], [63]-[65]. Each study describes a certain case of IS network with a predefined type of the load.

This paper presents a comparative analysis in terms of size and volume of the passive elements. Also, operation conditions of semiconductors in different IS networks are compared.

This section explains the component design guidelines that are the basis of our comparative analysis. Fig. 2 shows the operation principle of the traditional Z-source network in simple terms.

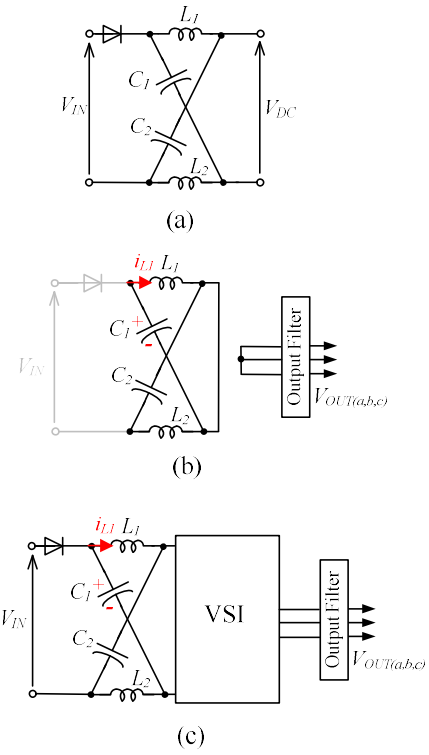


Fig. 2. Basic Z-Source network (a), in ST state (b) and active state (c).

There are two general modes of the operation of the circuit considered. In a ST state, the energy is stored in the Z-Source network elements and the operation mode where the stored energy in the amount of energy source supplies the load. The equivalent circuits for these modes are shown in Figs. 2*b* and 2*c*, respectively. It is known that

$$V_{C1} = V_{C2} = \frac{(1 - D_S)}{(1 - 2 \cdot D_S)} \cdot V_{IN}, \quad (1)$$

$$V_{DC} = \frac{1}{1 - 2 \cdot D_S} \cdot V_{IN}, \quad (2)$$

where D_S is the ST duty cycle, V_{DC} is a dc-link voltage, V_{IN} is the dc input voltage, V_{C1}, V_{C2} are capacitor voltages.

Many modulation techniques [70] - [87] can be applied to such topologies. All of them can be distinguished by the ST state generation. In such topologies, at equally distributed ST states, the modulation index M has its upper limit $M \le 1\text{-}D_S$, but the dc-link voltage has the lowest ripple. In the opposite case (maximum boost control), the modulation index has a wider range ($M \le 1$), but it requires larger passive elements.

To analyze and compare the different topologies, a constant boost control with equally distributed active states was assumed.

The main objects of our comparison were the passive elements and semiconductors. Along with the capacitance, the main parameter for the comparison of the capacitors is the maximum voltage Along with average current, the main parameter for the comparison of the inductors is inductance [67] - [69].

Taking into account the above conditions, the equation for the peak line output voltage V_{PL} as a function of the input voltage can be written as:

$$V_{PL} = M \cdot V_{IN} \cdot \frac{1}{1 - 2 \cdot D_S}, \quad (3)$$

where V_{PL} is a constant voltage level that is considered as a referenced dc-link voltage that must be maintained for the normal operation of the VSI.

At equally distributed active states, the modulation index M has its upper limit $M \le 1\text{-}D_S$. As a result,

$$V_{DC} = \frac{1}{1 - 2 \cdot D_S} \cdot V_{IN} = 2 \cdot V_{PL} - V_{IN}. \quad (4)$$

$$V_{C1} = V_{C2} = V_{PL}. \quad (5)$$

At the same time, high frequency generation of the active states causes high frequency ripples, as illustrated in Fig. 3.

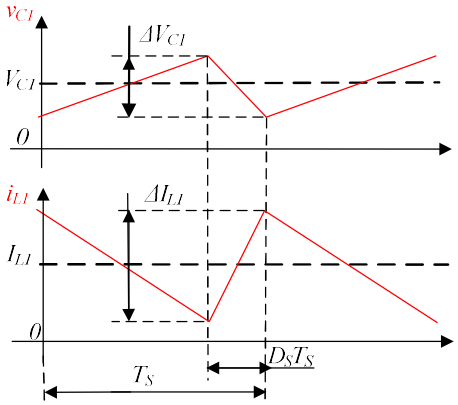


Fig. 3. Idealized waveforms of capacitor voltage and inductor current.

It is evident that the values of the passive components have to be calculated taking into account the predefined high frequency ripples of the voltage and the current. The current ripple through the inductor and the voltage ripple through the capacitors strongly depend on the ST duty cycle D_S:

$$\Delta I_{L1} = \int_0^{T_S \cdot D_S} \frac{di_{L1}}{dt} \cdot dt = \int_0^{T_S \cdot D_S} \frac{V_{C1}}{L_1} \cdot dt = \frac{V_{C1}}{L_1} \cdot T_S \cdot D_S, \quad (6)$$

The average input current is obtained by means of power balance, where it is assumed that the output power P_{OUT} is approximately equal to the input power P_{IN}:

$$P_{IN} = V_{IN} \cdot I_{IN} \approx P_{OUT} = P. \quad (7)$$

At the same time, it can be claimed that the average input current I_{IN} is strongly connected with the average inductor current I_{AV}:

$$I_{IN} = I_{AV}. \quad (8)$$

From the equations presented above, the minimum inductance value can be estimated to maintain the Boundary Conduction Mode (BCM) in the inductor current, which is a condition of normal operation:

$$\frac{\Delta I_{L1}}{2} \le I_{AV}, \quad (9)$$

Finally, the inductances L_1, L_2 in the Z-source network can be expressed as:

$$L_1 = L_2 \ge \frac{T_S}{2 \cdot P} \frac{V_{IN}^2 \cdot (1 - D_S) \cdot D_S}{(1 - 2D_S)}. \quad (10)$$

From the last equation, the minimum inductance value can be estimated to maintain high switching frequency ripples in the inductor current, which is the condition for the BCM operation and depends on the input parameters, i.e. input voltage and power.

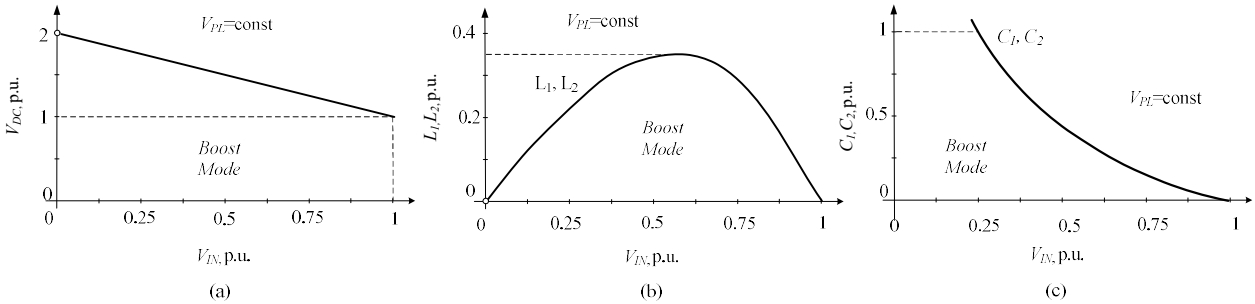


Fig. 4. The characteristics of ZSI: dc-link voltage (a), inductance (b) and capacitances (c) versus input voltage dependences.

The voltage ripple ΔV_{C1} across the capacitors can be analyzed similarly. The capacitor voltage ripple can be expressed as:

$$\Delta V_{C1} = \frac{1}{C_1}\int_0^{T_S D_S} i_{C1}(t)dt = \frac{P}{V_{IN}\cdot C_1}\cdot T_S D_S \,. \quad (11)$$

Taking into account that the average capacitor voltage must be constant, the equation for the voltage ripple factor K_{C1} can be derived as:

$$K_{C1} = \frac{\Delta V_{C1}}{V_{C1}} = \frac{P\cdot T_S\cdot D_S\cdot(1-2D_S)}{K_{C1}\cdot V^2{}_{IN}\cdot(1-D_S)} \quad (12)$$

As a result, the capacitor values can be calculated as:

$$C_1 = C_2 \geq \frac{P\cdot T_S\cdot D_S\cdot(1-2D_S)}{K_C\cdot V^2{}_{IN}\cdot(1-D_S)}, \quad (13)$$

where $K_{C1}=K_{C2}=K_C$.

The above representation of the passive elements calculation is not well informative. In particular, the equations contain the ST duty cycle that depends on the input voltage. In this case, it is more convenient to express the passive components taking into account Eq. (3). Finally, it can be represented as a function of the input voltage V_{IN}:

$$L_1 = L_2 \geq 2\cdot L\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}, \quad (14)$$

$$C_1 = C_2 = C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{2\cdot V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}. \quad (15)$$

In these equations, the L and C are relative units of inductance and capacitance respectively. These parameters are introduced for simplicity for further analysis:

$$L = \frac{V^2{}_{PL}\cdot T_S}{4\cdot P} = 1\ p.u. \quad (16)$$

$$C = \frac{2\cdot P\cdot T_S}{K_{C1}\cdot V^2{}_{PL}} = 1\ p.u. \quad (17)$$

Fig. 4 shows several curves that represent the performed analysis for the passive components and dc-link voltage estimation in relative units as a function of the input voltage where one unit of the voltage corresponds to the V_{PL}.

It should be noted that the buck mode converter works like a traditional VSI and the IS network is not involved in its normal operation. In conclusion, only the boost mode is considered in Fig. 4.

It is evident that the maximum dc-link voltage corresponds to the minimum input voltage. The inductance has a more interesting dependence. The required capacitance value rises rapidly with the input voltage decreasing. It should be noted that all the dependences are derived for constant input power condition. Also, the unity power factor with a symmetrical load is assumed. Losses are not taken into account. It is also clear that the point with zero input voltage is a theoretical assumption. In a real system, passive elements will be selected according to the voltage and power profile of the input source.

The next section presents a comprehensive overview of the existing IS inverters based on the component design guidelines described above. The final equations that define the passive element values and the voltage stress on the semiconductors are summarized in Tables II and III.

III. Overview of the Basic IS Networks

Further modifications of different IS networks are shown in Fig. 5. All IS networks are subdivided into the following groups: separated inductive components (Fig. 5*a, b*), magnetically coupled inductive components (Fig. 5*c-e h-k*), and those transformer-based (Fig. 5*f, g*). The implementation of magnetically coupled inductors or transformers in the IS networks can result in a higher voltage boost factor due to the turns ratio. The IS networks can roughly be divided (Table I) as follows: those with Continuous Input Current (CIC) highlighted in Fig. 5 and other ones with Discontinuous Input Current (DIC).

TABLE I
CLASSIFICATION OF IS NETWORKS

	Separate inductors	Coupled inductors	Transformers
DIC	Z-source	Z-source , T(trans)-Z-source, T(trans)- quasi-source Y-source, T-Z-source, Γ-Z-source	LCCT-Z-source
CIC	Quasi-Z-source, EZ-source	Quasi-Z-source, T(trans)- quasi-source with CIC, LCCT quasi-Z-source	LCCT-Z-source with CIC

Z-source and qZS networks [11], [12] belong to the topologies that can comprise single magnetic components as well as coupled magnetic components; the result is reduced core losses, core size and winding losses. Fig. 5*a* presents the qZS topology. A ZSI has DIC, a qZSI has CIC. It is well known that the boost factor B of both circuits is defined as:

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1-2\cdot D_S}. \quad (18)$$

Fig. 5*b* presents the EZ-source or Embedded Z-source network shown in [14], [31], which has CIC. This topology contains multiple independent voltage sources, which is an advantage (PV panels, fuel cells). At the same time, the EZ-source network is its drawback.

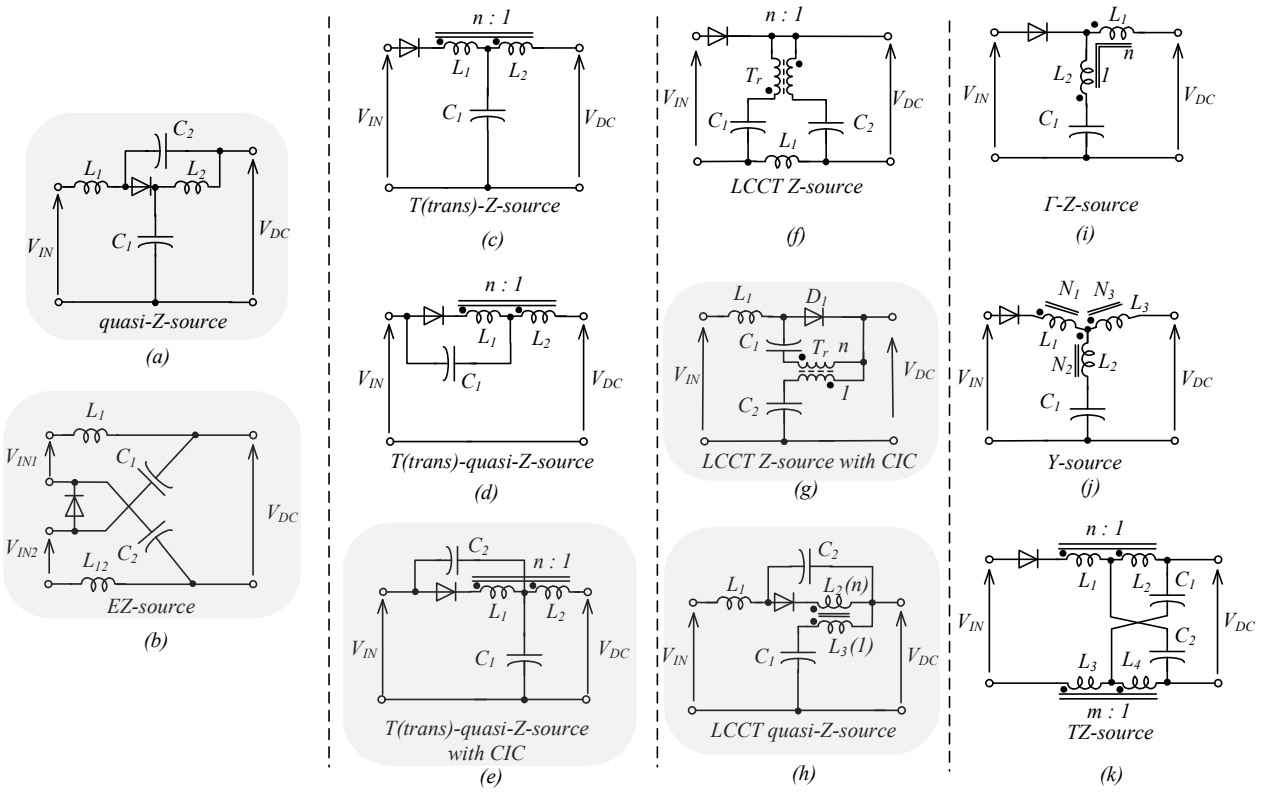


Fig. 5.Existing IS networks.

Additionally, a disadvantage of the network is asymmetrical working at the asymmetrical input voltage. An EZ-source network can be used in a system with an energy storage. The boost factor of the circuit is expressed as given by Eq. (18).

The T (trans)–Z-source (Fig. 5*c*) [39], T(trans)-quasi-Z-source network (Fig. 5*d*) [35], and T(trans)-quasi-Z-source network with CIC (Fig. 5*e*) [40] have magnetically coupled components. These circuits have a higher boost factor than the previous circuits and can be defined as:

$$B = \frac{1}{1-(n+1)\cdot D_S}. \tag{19}$$

where n is the turns ratio of the coupled inductors. The main drawback of these circuits is the leakage inductance.

The LCCT Z-source circuit is an inductor-capacitor-capacitor-transformer Z-source circuit. LCCT Z-source and quasi-Z-source [90], [36], [37] circuits are shown in Figs. 5*f,* 5*g* and 5*h*, respectively. LCCT Z-source and LCCT Z-source with CIC topologies include a high frequency ideal transformer. The capacitors of the LCCT circuit help to prevent the transformer core from saturation [90]. Only one inductive element is used to store the energy during the boost operation. The Quasi-Z-source circuit has CIC. The boost factor of the circuit is expressed by Eq. (19).

Γ-Z-source network [44] contains a coupled inductor as well. The circuit is shown in Fig. 5*i*. Γ-Z-source circuit has DIC and a high boost factor B:

$$B = \frac{1}{1-\frac{n}{n-1}\cdot D_S}. \tag{20}$$

T-Z-source network (Fig. 5*k*) [39] contains a two-winding dual inductor. T-Z-source network has DIC. This circuit has a higher boost factor than the previous circuits because of the turns ratio of the coupled inductor. The boost factor of the circuit is defined as:

$$B = \frac{1}{1-(2+n+m)\cdot D_S}. \tag{21}$$

Due to the resonant effects, the transient currents can be significant. Additionally, element count in this circuit is higher than in the topologies, but the input current is discontinuous.

Y-source network [42] belongs to the IS networks with magnetically coupled components. It is a three-winding inductor. The circuit is shown in Fig. 5*j*. Y-source network has DIC. The boost factor of the circuit is defined as:

$$B = \frac{1}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right)\cdot D_S}. \tag{22}$$

A wide class of the converters based on this network is presented in [42]. However, the buck mode is not experimentally verified. The disadvantage of this topology is the presence of the leakage inductance. It also applies to any other IS topology where the dc-link is connected to a coupled inductor only.

IV. Overview of the IS-Derived Buck-Boost MLIs

The combination of any IS networks with multilevel or cascaded inverters gives a single-stage energy conversion with buck-boost capabilities and reduces voltage stress on the semiconductors. At the same time, most of the

modifications discussed have a larger number of passive components. The following section presents a comprehensive overview along with the comparison of the components.

A. Z-source-derived buck-boost MLIs

Fig. 6 shows Three-Level (3L) Neutral-Point-Clamped (NPC) topologies based on the IS network with DIC. The single-stage buck-boost MLI was proposed in [88] as the logical extension of the Two-Level (2L) inverter and ZSI.

As compared to the traditional NPC inverter, the inverter uses two additional Z-source networks for boosting its input voltage to a higher dc-link voltage.

Although it is theoretically feasible, in terms of economy, it is not the best solution since it uses two isolated input voltage sources and a number of passive elements, which may increase the cost, size and weight of the inverter. To decrease passive component count, the Z-source NPC inverter with a single impedance network has been proposed in [88]. However, this topology (Fig. 6*b*) must also be fed from two input voltage sources. Another option is to use front-end decoupled capacitors.

In the case of separated input voltage source and two ZS networks (Fig. 6*a*), passive element count is larger, but their values per element are smaller. It means that the Z-source network is distributed.

In the topologies with the high-frequency transformers and with two additional capacitors introduced, the Z-source NPC inverter with a single IS network could be supplied from a single input voltage source [89]-[92] (Fig. 6*c*). Fig. 6*d* illustrates a similar solution with a double transformer and a separated input voltage dc source. The main difference lies in the boost characteristic that is equal to Eq. (19).

By using a transformer with a turns ratio different from 1:1, an input voltage gain higher than that with the traditional Z-source network can be achieved. The dc-link utilization is improved as well.

It should be noticed that the instantaneous magnetic flux in the transformer is equal to zero and it can be assumed to be ideal. Fig. 7 illustrates the dependences of passive elements and dc-link voltage versus the input voltage with a different turns ratio *n*. It can be seen that in this solution with *n=2*, the dc-link is utilized better and passive elements are smaller.

At the same time, in [89] these solutions are not verified experimentally. The balancing issue of the transformer may require additional investigations.

The final equations that define the passive element values and the voltage stress on the semiconductors are summarized in Tables II and III.

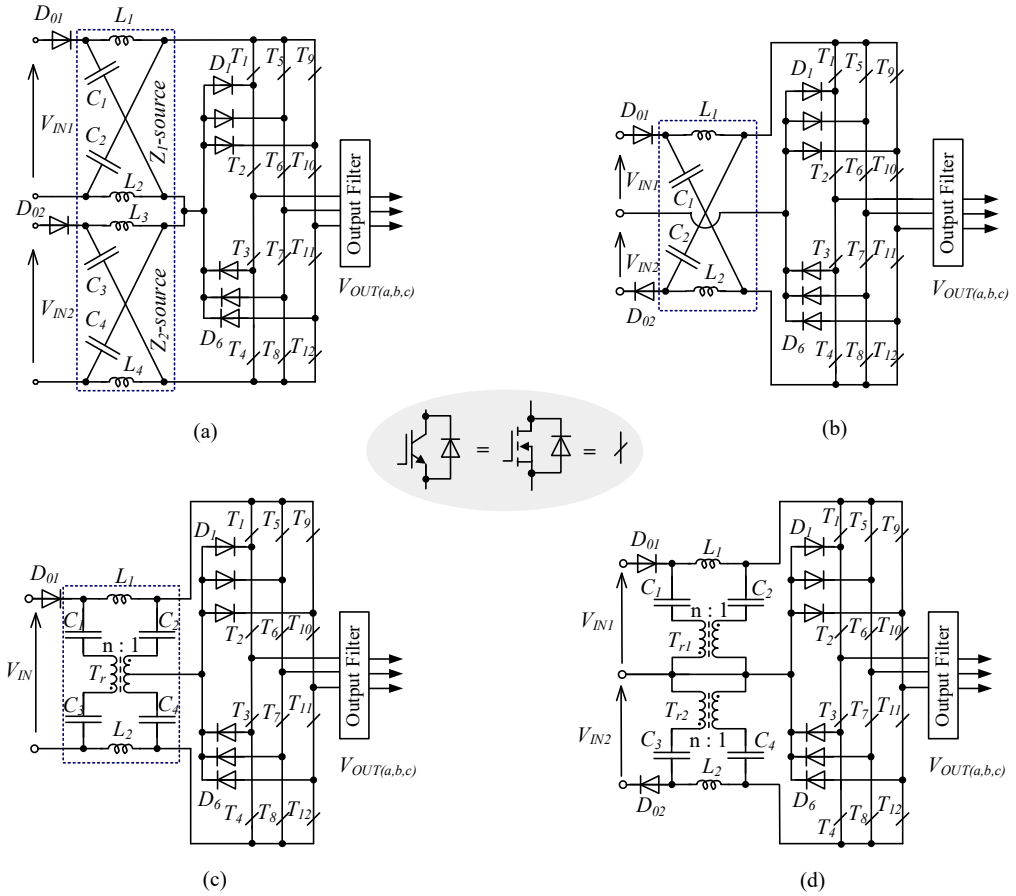


Fig. 6. 3L NPC topologies based on IS network with discontinuous input current: the inverter with two Z-source networks and separated input voltage sources (a); the Z-source NPC inverter with a single impedance network and separated input voltage sources (b); the transformer Z-source NPC inverter with a single input voltage source (c); the transformer Z-source NPC inverter with a separated input voltage source (d).

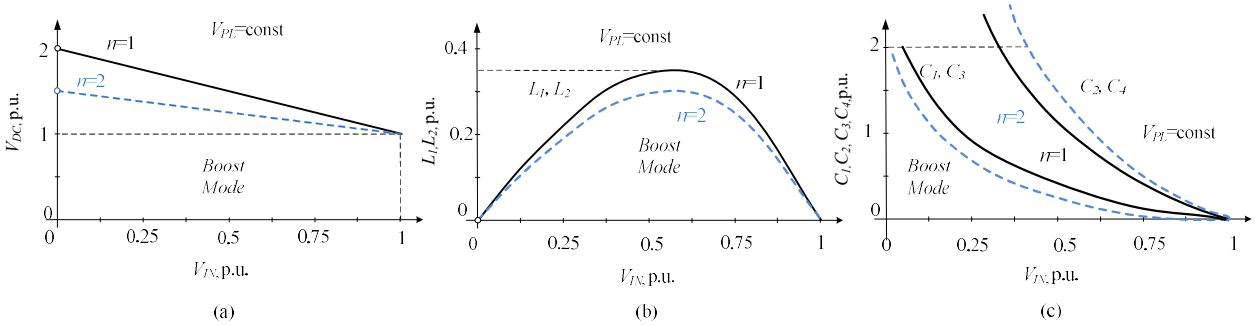


Fig. 7. 3L NPC transformer Z-source inverter: dc-link voltage (a), inductance (b) and capacitances (c) versus input voltage dependences with constant V_{PL}.

Fig. 8 shows a four-level (4L) inverter. In this case, all input power is distributed between several input Z-source networks. The idea presented in [89], [91] is quite simple. It is a generalized example of any Z-source network to MLIs realized on the basis of the "Diode Clamped" topology.

Because of the possibility to regulate the output voltages separately in each Z-source, such MLIs are suitable to be applied in the supply systems with locally dispersed energy sources. At the same time, it should be noted that this topology has not been verified experimentally and requires further investigation.

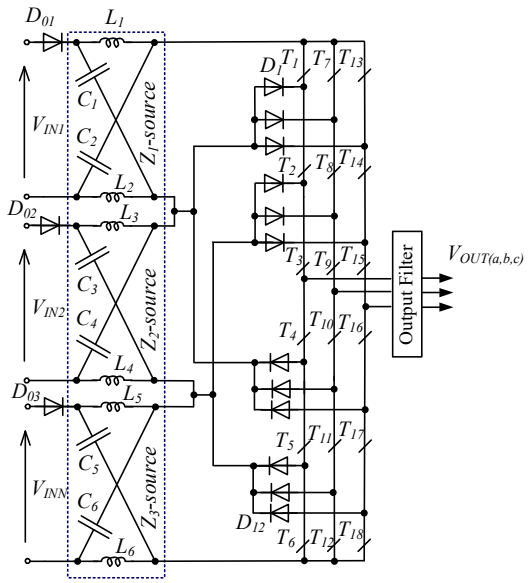


Fig. 8. Four-level diode clamped Z-source inverter.

Fig. 9 illustrates a further extension of the idea of the multiple dc-link source of the multilevel diode clamped topology [93] that has only two impedance Z-source networks. This paper describes also the non-optimized five-level Z-source diode-clamped inverter with four Z-source networks. It is derived similar to the inverter in Fig. 8 by means of adding a voltage source with the Z-source network.

Reference [93] has also revealed newly identified partial ST states, which are discussed in detail in the next section. As a result, the proposed inverter can boost its output voltage, while the switch with more distinct voltage levels is used to improve output waveform quality.

Fig. 10 shows further modifications of the 3L ZSIs. Fig. 10*a* shows the 3L Z-source DC-Link Cascaded (DCLC) inverter [94], [95]. The passive elements are the same as in the NPC. The only difference between the 3L NPC inverter and the DCLC inverter lies in the asymmetrical blocking voltage on the transistors and absence of the clamping diodes. The DCLC inverter can only be modulated using the modified Phase Disposition (PD) pulse-width modulation (PWM) scheme because it lacks redundant switching states.

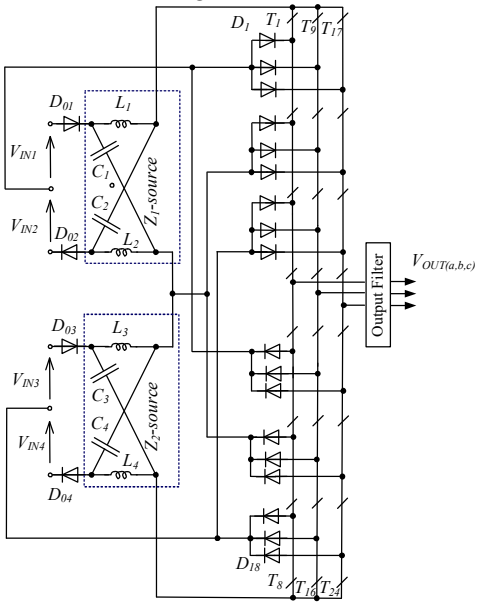


Fig. 9. Five-level diode clamped Z-source inverter.

In the case of the dual configuration (Fig. 10*b*) [94], [95], the phase output voltage of the transformer corresponds to the line input voltage. The dc-link voltage can be twice smaller at the turns ratio equal to 1. The input voltage equal to 0.5 p.u. corresponds to the margin between the buck and the boost modes. The main difference between the dual solution with separated and single Z-source network (Fig. 10*c*) lies in the power flow. In the second case, the amount of passive components is reduced by half, but their sizes are larger.

Cascaded solutions based on the Z-source networks have been reported in several papers [96], [97]. Simple cascading is described in [97]. Two Z-source networks, two isolated input voltage sources and two 2L Full Bridge (FB) inverters provide five-level output voltage per single phase.

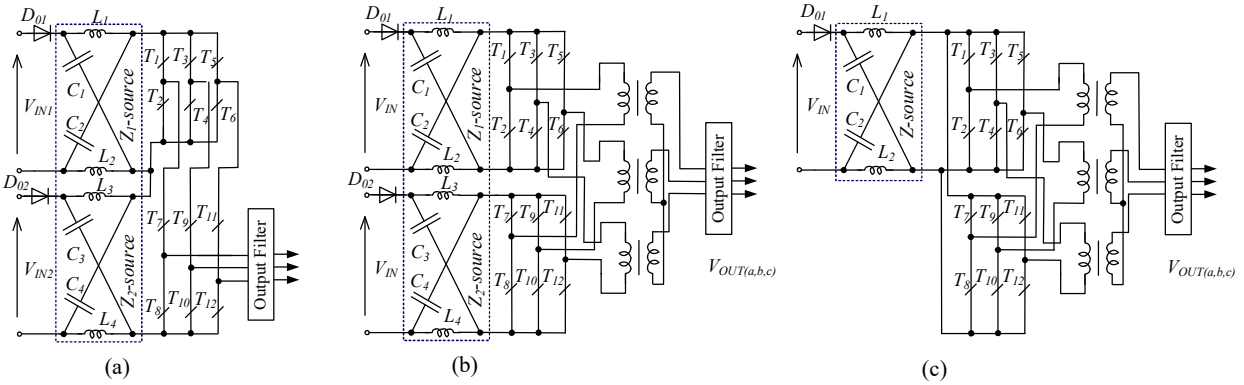


Fig. 10. Modifications of the 3L Z-source based inverters: 3L DCLC inverter with two Z-source networks (a), 3L dual inverter with two Z-source networks (b), 3L dual inverter with single Z-source network (c).

Fig. 11 shows the general principle of more complex cascading of the hybrid-sourced network in the 3L NPC [96]. This method requires three isolated input voltage sources and N networks. The total boost voltage of these converters is

$$V_{PL} = \frac{1-D_S}{1-(1+N)D_S} \cdot V_{IN}, \tag{23}$$

where $V_{IN}=V_{IN1}+V_{IN2}+V_{IN3}$.

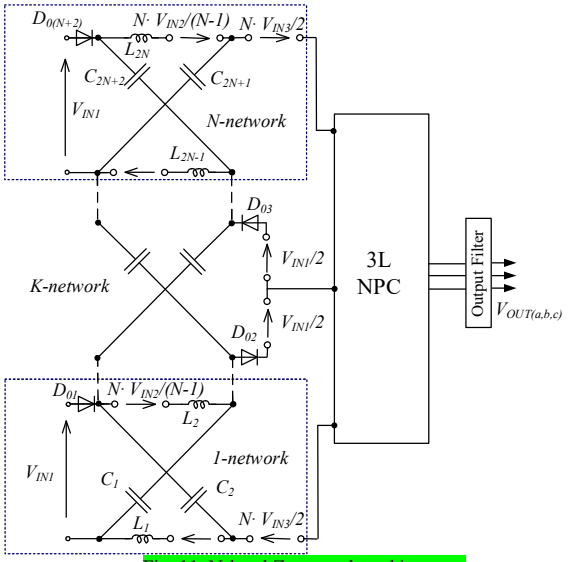


Fig. 11. N-level Z-source-based inverter.

In this method, the number of networks N cascaded together must always be odd with the middle network assumed as

$$K = \frac{N+1}{2}. \tag{24}$$

Note that in order to split the input voltage sources and realize this structure, in addition to impedance network components, decoupled capacitors are required.

Paper [96] describes another cascading method where N-1 additional capacitors and $2(N-1)$ additional diodes are used for connecting N IS networks together at their respective dc-links. Called a dc-link cascaded solution, it ensures very high boost performance:

$$V_{PL} = \frac{1-D_S}{(1-2\cdot D_S)^{\frac{N+1}{2}}} \cdot V_{IN}. \tag{25}$$

References [98] and [99] provide a further comprehensive study of the Z-source-based MLIs, in particular in ac-ac applications.

Fig. 12 shows the multilevel Z-source-based inverter with a reduced number of switches. Paper [100] describes a new inverter topology based on a mixture of cascaded basic units and one FB unit. The basic unit includes one Z-source network, one input dc voltage source and two switches generating two voltage levels. The cascaded basic units produce positive and zero-voltage levels. At the same time, the inverter proposed obtains positive, zero- and negative voltage levels. Only a single-phase solution has been studied in detail, but a three-phase design is also possible.

The basic unit can operate in three different modes: zero, active and ST states. In the ST state, both switches S_1 and S_2 are conducting and the output voltage is zero. The active state is generating when only S_1 is conducting. Zero state corresponds to the S_2 conduction.

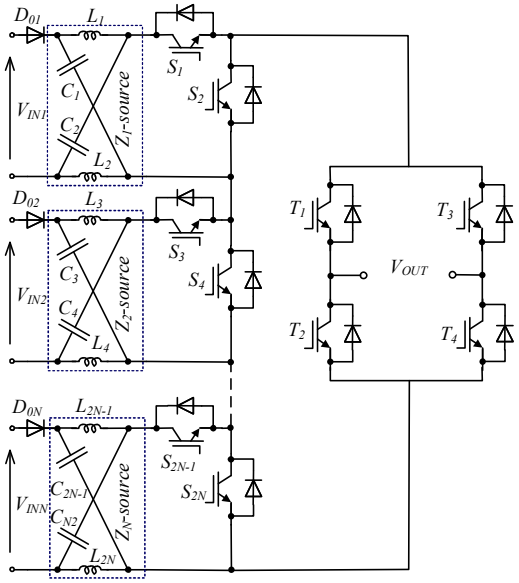


Fig. 12. Z-source-based MLI with a reduced number of switches.

The overall number of power semiconductor switches is reduced with respect to the traditional MLIs. In this topology, the peak output voltage is not limited to the dc sources voltage summation similar to the traditional cascaded MLIs; it can be boosted with Z-source network due to the ST state generation. As compared to the

traditional Z-source inverter, the total harmonic distortion of the injected voltage is decreased.

Fig. 12 demonstrates that any *N*-level topology is achievable under the principle described above. It is obvious that the proposed solution can be expanded to a three-phase system.

Passive elements along with semiconductors of a Z-source network are estimated similar to any of the above presented topologies, as summarized in Tables II and III.

B. Quasi and Trans-quasi-Z-source-derived buck-boost MLIs

Further development of the IS based buck-boost MLIs is connected with trans-Z-source and trans-quasi-Z-SOURCE inverters. In particular, Fig. 13 shows 3L NPC solutions [101], [102].

Resulting from the extended theory of the Z-source inverter, the transformer based Z-source and the quasi-Z-source (trans-Z-source and trans-Quasi-Z-source) inverters are proposed in [35].

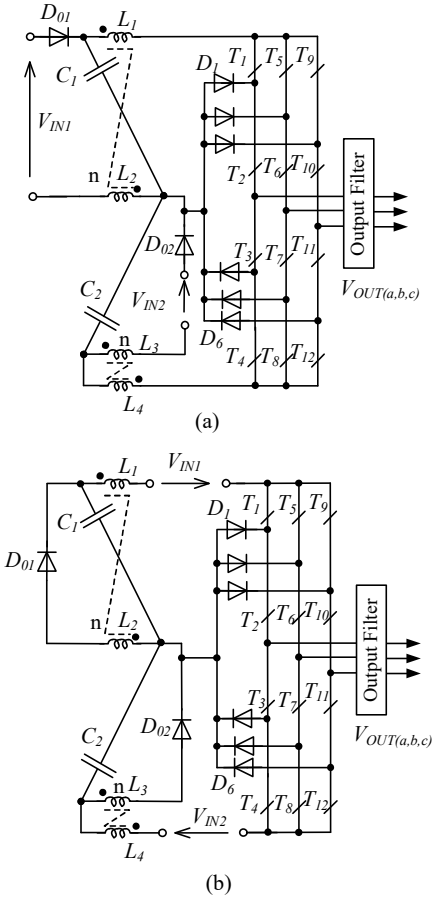


Fig. 13. 3L NPC trans-Z-source inverter (a) and trans-quasi-Z-source inverter (b).

Both of the inverters consist of a transformer to replace the two inductors in the original Z-source impedance network, removing one capacitor from it. This can enhance the boosting capability of the Z-source network and reduce one passive component, thus lowering the size and the cost of the system.

The circuit configuration of the trans-Z-source NPC inverter is shown in Fig. 13*a*. Fig. 13*b* shows the circuit configuration with the trans-quasi-Z-source NPC inverter, where the only difference is the location of the input voltage source. Each of them has two cascaded transformer based IS networks, namely the upper side network and the lower side network. The inductors L_1 and L_2 are the primary and the secondary winding of the transformer located at the upper side network, while L_3 and L_4 are the primary and the secondary winding of the transformer located at the lower side network.

The main difference in the first and the second approach lies in the current shape of the input voltage source, which can have Continuous Conduction Mode (CCM) in the second case unless no null state is used.

At the same time, it should be noticed that these magnetic elements have no instantaneous magnetic flux equal to zero and must be designed as coupled inductors. This solution with n=2 has a better characteristic for dc-link use similar to the transformer based solutions in Figs. 6*c* and 6*d*.

Based on the average flux in the coupled inductors and the values of the passive elements in order to provide CCM and the same voltage ripple across the capacitors, the overall size of the passive elements will be the same as in the transformer Z-source-based solution.

Another solution with CIC is described in [103]-[106]. It is based on the double Quasi-Z-source (qZS) network and single input voltage source (Fig. 14). Resulting from a steady state analysis of the three-phase solution, it can be concluded that the overall size of the magnetics and capacitors is the same as in the 3L NPC solution with two Z-source networks (Fig. 6*a*). The voltage on the capacitors is unequally distributed. Internal capacitors C_2 and C_3 have constant voltage at the constant boost control. The voltages on the capacitors C_1 and C_4 are proportional to the ST duty cycle.

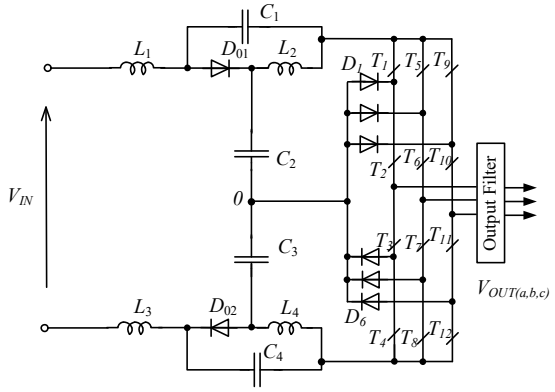


Fig. 14. 3L NPC qZS inverter with continuous input current.

Recently, another trans-Z-source NPC inverter presented in [109], [109] and shown in Fig. 15 was patented [107], [108]. The same topology, called the trans-Z-source NPC inverter, was described in [35]. Also, this topology has the same name and similar configuration as the topology presented in Fig. 13*a*.

To distinguish that topology from the previous one, it will be called a T-source NPC inverter since it is based on the T-source network presented in [33] and patented before in [107].

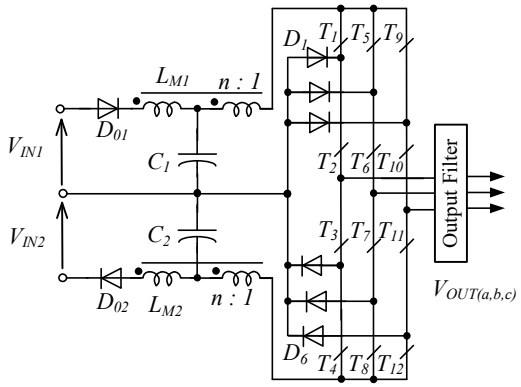


Fig. 15. 3L NPC T-source inverter.

Due to the turns ratio between the coupled inductors, the boost factor is equal to (19). An important issue is that the total instantaneous magnetic flux is not equal to zero. As a result, the magnetic elements must be designed as coupled inductors. The size of the coupled inductor is defined by the magnetizing inductance L_M and the current of the magnetizing inductance I_M. The topology presented has two coupled inductors, the values of which as a function of the input voltage in the BCM are shown in Table III.

By a coupling with the turns ratio different from 1:1, an input voltage gain is similar to the transformer Z-source based inverter. Dc-link utilization illustrated in Table I is improved as well.

In the following papers [110], [111], focus was on the 3L NPC T-source inverter with CIC based on IS networks presented in [40]. It was shown that the CIC T-source inverter has better performance due to the continuous input current. At the same time, the overall size of the passive elements remains the same.

Finally, Fig. 16 reveals the Γ-source inverter proposed in [109].

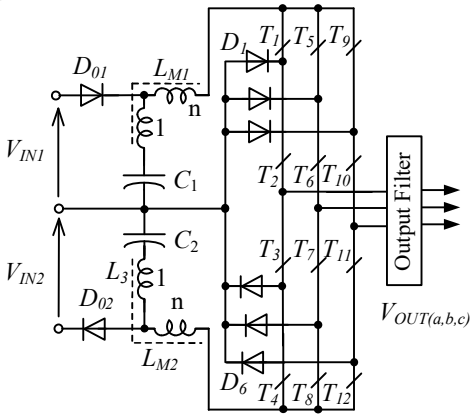


Fig. 16. 3L NPC Γ-source inverter.

It is based on the idea similar to that with the coupled inductors. But in such configurations, the input voltage gain has opposite dependences, where the turns ratio 1:1 corresponds to the maximum boost (20).

Similar to the T-source inverter, dc-link utilization may be improved considerably by proper selection of the turns ratio.

V. Comparative Analysis of the IS-Derived Buck-Boost Inverters

To summarize the results of our comparative analysis of the buck-boost inverters based on IS networks, the relative size of the passive components along with the voltage stress on the semiconductors were estimated.

Our assumption here is that the volume of the magnetics Vol_L is proportional to the stored energy:

$$Vol_L \cong E_L = \frac{L \cdot I_{AV}^2}{2}, \tag{26}$$

which is estimated by means of the inductance L and the average inductor current I_{AV}. For convenience and generalization of the analysis, the summarized magnetics energy in relative units was introduced as:

$$E_{LW} = \sum_{i=1}^{N} \frac{L_i \cdot I_{AVi}^2}{2}, \tag{27}$$

where N is the number of inductances. Such parameters allow estimating and comparing the required amount of magnetic elements, their sizes and cost for a certain topology.

Similar parameters can be introduced for the capacitors:

$$E_{CW} = \sum_{i=1}^{N} \frac{C_i \cdot V_{MAXi}^2}{2}, \tag{28}$$

where E_{CW} is the summarized energy stored in the capacitors.

It is well known that size, volume and cost of the capacitors strictly depend on the maximum voltage and capacitance. The size of the passive elements depends strongly on the material and switching frequency as well, but these parameters were assumed to be the same for all topologies.

In order to estimate the contribution of semiconductors to the topologies above, their amount and blocking voltage was also taken into account. The currents were neglected because of their dependence on the modulation techniques.

$$D_W = \sum_{i=1}^{N} V_{BDi}, \tag{29}$$

$$T_W = \sum_{i=1}^{N} V_{BTi} \tag{30}$$

The power density and the specific weight depend on the introduced parameters.

Fig. 17 shows diagrams that illustrate comparative analysis in terms of the summarized parameters. First of all, it is concluded that high boost performance requires more stored energy in the passive elements. Fig. 17*a* shows that qZSI with a higher boost level must have larger passive elements to provide the same ripple of the current and voltage. In addition, the voltage stress across semiconductors is increasing.

Specifically, Fig. 17*b* shows the comparison between the Z-source NPC inverter and the transformer Z-source NPC inverter in the boost mode with the turns ratio n=2. V_{IN} was equal to 0.5 p.u., which corresponds to half the V_{PL} voltage. It can be seen that due to the transformer and reduced ST duty cycle, the blocking voltage of the

semiconductors is lower, the passive elements are slightly smaller.

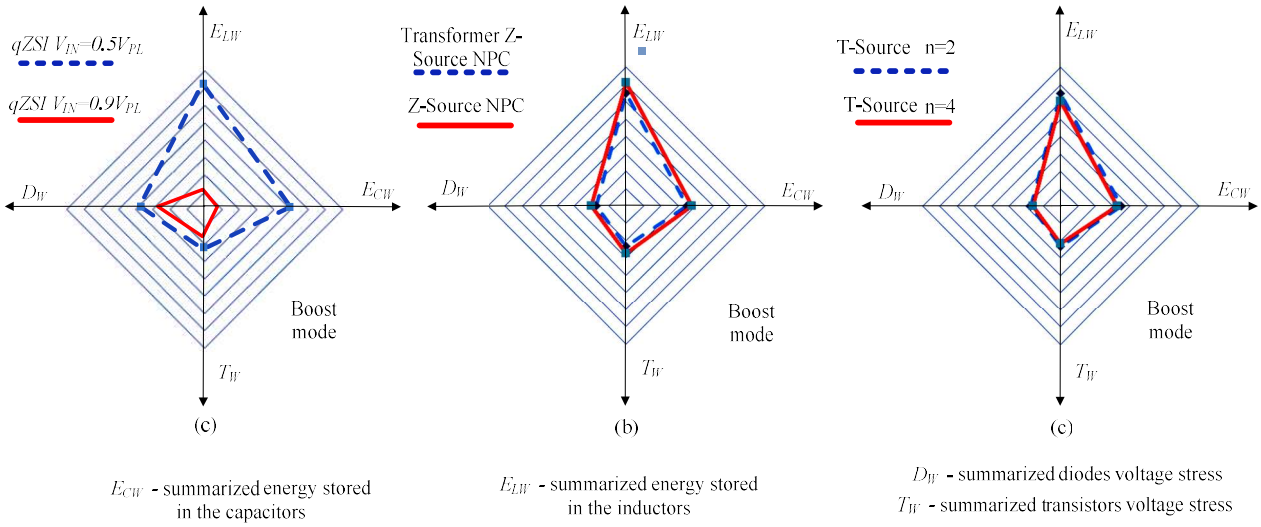


Fig. 17. Comparative analysis: qZSI with high boost versus qZSI with low boost (a); transformer-based Z-source NPC inverter versus Z-source NPC inverter in the boost mode (b); T-source inverter with n=2 versus T-source inverter with n=4 in the boost mode (c).

TABLE II. VOLTAGE STRESS ON THE SEMICONDUCTORS OF THE BUCK-BOOST INVERTERS WITH IS NETWORKS

Topology	IS network		Inverter			
	№	Diodes	№	Transistors	№	Diodes
3L NPC with single/two Z-source networks, 3L NPC qZS inverter (Fig. 6*b*/Fig. 6*a*, Fig. 14)	D_{01}, D_{02}	$V_{PL}-\frac{V_{IN}}{2}$	T_1-T_{12}	$V_{PL}-\frac{V_{IN}}{2}$	D_1,-D_6	$V_{PL}-\frac{V_{IN}}{2}$
3L NPC with single transformer Z-source network (Fig. 6*c*)	D_{01}	$V_{PL}+\frac{V_{PL}}{n}-\frac{V_{IN}}{n}$	T_1-T_{12}	$\frac{V_{PL}}{2}+\frac{V_{PL}}{2\cdot n}-\frac{V_{IN}}{2\cdot n}$	D_1,-D_6	$\frac{V_{PL}}{2}+\frac{V_{PL}}{2\cdot n}-\frac{V_{IN}}{2\cdot n}$
3L NPC with two transformers Z-source network/3L NPC T-source inverter/3L NPC trans-Z/qZS inverter (Fig. 6*d*/ Fig. 15/ Fig. 13*a*/Fig. 13*b*)	D_{01}, D_{02}	$\frac{V_{PL}}{2}+\frac{V_{PL}}{2\cdot n}-\frac{V_{IN}}{2\cdot n}$	T_1-T_{12}	$\frac{V_{PL}}{2}+\frac{V_{PL}}{2\cdot n}-\frac{V_{IN}}{2\cdot n}$	D_1,-D_6	$\frac{V_{PL}}{2}+\frac{V_{PL}}{2\cdot n}-\frac{V_{IN}}{2\cdot n}$
3L DCLC with two Z-source networks (Fig. 10*a*)	D_{01}, D_{02}	$V_{PL}-\frac{V_{IN}}{2}$	T_1-T_6	$V_{PL}-\frac{V_{IN}}{2}$		
			T_7-T_{12}	$2\cdot V_{PL}-V_{IN}$		
3L dual inverter with single Z-source network (Fig. 10*b*)	D_{01}	$V_{PL}-V_{IN}$	T_1-T_{12}	$V_{PL}-V_{IN}$		
3L dual inverter with two Z-source networks (Fig. 10*c*)	D_{01}, D_{02}	$V_{PL}-V_{IN}$	T_1-T_{12}	$V_{PL}-V_{IN}$		
Z-source-based MLI with reduction of switches (Fig. 12)	D_{01}-D_{0N}	$\frac{2\cdot V_{PL}-V_{IN}}{N}$	T_1-T_4	$2\cdot V_{PL}-V_{IN}$		
			S_1-S_{2N}	$\frac{2\cdot V_{PL}-V_{IN}}{N}$		
3L NPC Γ-source inverter (Fig. 16)	D_{01}, D_{02}	$n\frac{V_{PL}}{2}+\frac{V_{IN}}{2}-n\frac{V_{IN}}{2}$	T_1-T_{12}	$n\frac{V_{PL}}{2}+\frac{V_{IN}}{2}-n\frac{V_{IN}}{2}$	D_1,-D_6	$n\frac{V_{PL}}{2}+\frac{V_{IN}}{2}-n\frac{V_{IN}}{2}$

TABLE III. COMPARISON OF PASSIVE ELEMENTS OF THE BUCK-BOOST INVERTERS WITH IS NETWORKS

Topology	Inductors			Capacitors		
	№	Average current	Value	№	Average voltage	Value
2L/3L NPC with single Z-source network (Fig. 6*b* /)	L_1, L_2	$\frac{P}{V_{IN}}$	$2\cdot L\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}$	C_1, C_2	V_{PL}	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{2\cdot V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$
3L NPC/DCLC with two Z-source networks (Fig. 6*a* /Fig. 10*a*)	L_1-L_4	$\frac{P}{V_{IN}}$	$L\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}$	C_1-C_4	$\frac{V_{PL}}{2}$	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$

3L NPC with transformer Z-source network (Fig. 6*c*, Fig. 6*d*)	L_1, L_2	$\frac{P}{V_{IN}}$	$L\cdot\frac{V_{IN}\cdot(n+1)\cdot(V_{PL}-V_{IN})}{V_{PL}\cdot((n+1)\cdot V_{PL}-V_{IN})}$	C_1, C_3	$\frac{V_{PL}}{2}(1+n)-\frac{n\cdot V_{IN}}{2}$	$C\cdot\frac{V^2{}_{PL}}{V_{IN}\cdot((n+1)\cdot V_{PL}-n\cdot V_{IN})}\times$ $\times\frac{(V_{PL}-V_{IN})}{((n+1)\cdot V_{PL}-V_{IN})}$
				C_2, C_4	$\frac{V_{IN}}{2}$	$C\cdot\frac{n\cdot V^2{}_{PL}\cdot(V_{PL}-V_{IN})}{V_{IN}^2\cdot((n+1)\cdot V_{PL}-V_{IN})}$
3L dual inverter with single Z-source network (Fig. 10*c*)	L_1, L_2	$\frac{P}{V_{IN}}$	$2\cdot L\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}$	C_1, C_2	$\frac{V_{PL}}{2}$	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$
3L dual inverter with two Z-source networks (Fig. 10*b*)	L_1-L_4	$\frac{P}{2\cdot V_{IN}}$	$4\cdot L\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}$	C_1-C_4	$\frac{V_{PL}}{2}$	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{2\cdot V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$
Z-source-based MLI with reduction of switches (Fig. 12)	L_1-L_{2N}	$\frac{P}{V_{IN}}$	$\frac{2\cdot L}{N}\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}$	C_1-C_{2N}	$\frac{V_{PL}}{N}$	$C\cdot\frac{N\cdot V_{PL}\cdot(V_{PL}-V_{IN})}{2\cdot V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$
3L NPC trans-Z/qZS inverter (Fig. 13*a*/Fig. 13*b*)	L_1-L_4	$\frac{P}{V_{IN}}$	$L\cdot\frac{V_{IN}\cdot(n+1)\cdot(V_{PL}-V_{IN})}{2\cdot V_{PL}\cdot((n+1)\cdot V_{PL}-V_{IN})}$	C_1-C_4	$\frac{V_{PL}}{2}$	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{V_{IN}\cdot((n+1)\cdot V_{PL}-V_{IN})}$
3L NPC qZS inverter (Fig. 14)	L_1-L_4	$\frac{P}{V_{IN}}$	$L\cdot\frac{V_{IN}(V_{PL}-V_{IN})}{V_{PL}\cdot(2\cdot V_{PL}-V_{IN})}$	C_1, C_4	$\frac{V_{PL}-V_{IN}}{2}$	$C\cdot\frac{V^2{}_{PL}}{V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$
				C_2, C_3	$\frac{V_{PL}}{2}$	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{V_{IN}\cdot(2\cdot V_{PL}-V_{IN})}$
3L NPC T-source inverter (Fig. 15)	L_{M1}, L_{M2}	$\frac{P\cdot(n+1)}{V_{IN}\cdot n}$	$L\cdot\frac{V_{IN}\cdot n^2\cdot(V_{PL}-V_{IN})}{(n+1)\cdot V_{PL}\cdot((n+1)\cdot V_{PL}-V_{IN})}$	C_1, C_2	$\frac{V_{PL}}{2}$	$C\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})\cdot(n+1)}{V_{IN}\cdot((n+1)\cdot V_{PL}-V_{IN})}$
3L NPC Γ-source inverter (Fig. 16)	L_{M1}, L_{M2}	$\frac{P}{V_{IN}}$	$L\cdot\frac{n}{n-1}\cdot\frac{V_{IN}\cdot(V_{PL}-V_{IN})}{V_{PL}\cdot(\frac{n}{n-1}\cdot V_{PL}-V_{IN})}$	C_1, C_2	$\frac{V_{PL}}{2}$	$C\cdot\frac{n}{n-1}\cdot\frac{V_{PL}\cdot(V_{PL}-V_{IN})}{V_{IN}\cdot(\frac{n}{n-1}\cdot V_{PL}-V_{IN})}$

As can be seen from the comparison of the ZSI and the qZSI, no differences in terms of overall size of the passive elements and semiconductors were found. Taking into account that the qZSI solution has the CIC, the Z-source network is not superior over the qZS network.

Under Z-source derived topologies with different passive element count, no differences were found in terms of summarized storage energy in capacitance and inductance. The overall size of the passive components is almost the same. Regarding the reliability issues, it is preferable to have fewer components.

Our further comparison focuses on the solution based on the coupled inductors with different turns ratios (T-source and Γ-source networks). In this model, the coupled inductor is represented by means of the magnetizing inductance and an ideal transformer with the turns ratio n.

Fig. 17*c* shows figures that correspond to different turns ratios of the coupled inductors of the T-source networks. It can be seen that a higher value (n=4) of the turns ratio leads to a reduced ST duty cycle, the blocking voltage of the semiconductors is lower (about 10 %), the passive elements are decreasing as well (about 10 %). At the same time, higher turns ratio of the inductors leads to a more complex design.

It can be concluded that despite the different configurations of the IS networks, the overall size of the magnetics remains the same. Definitely, from a manufacturing point of view, the overall size of the large single inductor can be smaller than the overall size of several separated inductors with the same stored energy.

VI. Conclusions

IS networks are becoming increasingly popular in the research area, in particular in single-stage buck-boost inverter applications. This paper has presented a comprehensive analytical comparison of the IS based buck-boost inverters in terms of passive components and semiconductors. All of them can be classified according to the CIC or DIC, with or without a transformer, with or without inductor coupling.

It should be mentioned that this study focused only on lossless systems. However, resonance phenomena that may occur in any IS networks should be taken into account along with switching frequency selection and closed loop system design.

The main criterion for our comparison was stored energy in the passive elements, which was considered under constant and predefined high frequency current ripple in the inductors and the voltage ripple across the capacitors.

Many solutions based on Z-source and qZS networks exist and are being discussed. We demonstrated clearly that the difference lies in the input current waveform and voltage distribution across the capacitors, but the overall size of the converters designed for identical operating conditions is the same. In addition, there is no difference in terms of voltage stress on the semiconductors. qZSI is a more preferable solution due to CIC. The conclusion may be extended to all IS networks. Solutions with DIC

have no advantages over their modifications with CIC.

A wide input voltage regulation requires larger passive elements. Also, the voltage stress across semiconductors is increasing. The modulation techniques with unequally distributed ST states decrease the voltage stress across semiconductors. In order to mitigate such oscillations, passive element size should be increased as well.

MLIs are now an interesting solution even in low voltage low power applications mostly due to their higher switching frequency and the reduced output filter size. At the same time, novel IS networks extend the input voltage range regulation without increasing the number of energy conversion stages.

Separation of the input voltage source leads to an increased passive element count and probably to deteriorated reliability but the overall size of the converter may be approximately the same.

Several papers have presented inverters based on T-source and Γ-source networks that have coupled inductors and a capability of better dc-link utilization. Better dc-link use is achieved by means of the turns ratio of the coupled inductors different from 1. Along with the reduced capacitor size achieved by the better dc-link use, it leads to a more complex design of the coupled inductors. It is similar to the Z-source transformer based MLIs. In that case, the transformer is separated from the inductors and can be considered as ideal.

In addition, it should be noticed that solutions with improved dc-link utilization (T-source, Y-source, Γ-source) may have a problem in practical applications because of the leakage inductances in the coupled inductors. Very high number of turns ratio of coupled inductors is not recommended for practical implementation.

Inverter stages may differ. Converter types line NPC, DCLC and dual topologies have been discussed in the literature. DCLC topology requires no clamping diodes but half of the transistors have doubled voltage stress. The dual topology semiconductors have twice lower voltage stress than the NPC inverter, but an additional transformer is required.

VII. References

General overview

[1] "Renewables 2015 Global Status Report," Renewable Energy Policy Network for the 21st Century, Paris, France, June 2015.

[2] "The Fuel Cell Industry Review 2012," Fuel Cell Today, Royston, United Kingdom, 2012.

[3] S.B. Kjaer, J.K. Pedersen, and F. Blaabjerg, "A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules," *IEEE Trans. Ind. Appl.*, vol.41, no.5, pp. 1292- 1306, Sept.-Oct. 2005.

[4] D. Meneses, F. Blaabjerg, O. García, J.A. Cobos, "Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application," *IEEE Trans. Power Electron*., vol. 28, no. 6, pp. 2649-2663, 2013.

Active buck-boost inverters

[5] J. Kikuchi and T. A. Lipo, "Three-phase PWM boost-buck rectifiers with power-regenerating capability," *IEEE Transactions on Industry Applications,* vol. 38, pp. 1361-1369, Sept./Oct. 2002.

[6] F. Gao, P.C. Loh, D.M. Vilathgamuwa, F. Blaabjerg, C.K. Goh and J. Q. Zhang, "Topological and Modulation Design of a Buck-Boost Three-Level Dual Inverter," in *Proc. IEEE-IECON' 06*, 2006, pp. 2408-2413.

[7] F. Gao, R. Teodorescu, F. Blaabjerg, P.C. Loh and D.M. Vilathgamuwa, " Performance Evaluation of Buck-Boost Three-Level Inverters with Topological and Modulation Development," in *Proc. Power Electronics and Applications, 2007 European Conference on*, 2007, pp. 1-10.

[8] F. Gao, R. Teodorescu, F. Blaabjerg, P.C. Loh, and D.M. Vilathgamuwa, "Topological design and modulation strategy for buck–boost three-level inverters," *in Proc. IEEE PESC, 2007*, pp. 1578–1584.

[9] F. Gao, R. Teodorescu, F. Blaabjerg, P.C. Loh, and D.M. Vilathgamuwa, "Topological design and modulation strategy for buck–boost three-level inverters," *IEEE Trans. Power Electron*., vol. 24, no. 7, pp. 1722 - 1732, July 2009..

[10] R.L. Mathew, K.S. Jiji "A three level neutral point clamped Inverter with buck-boost capability for renewable energy sources", *International Conference on Sustainable Energy and Intelligent Systems (SEISCON 2011)*, 2011 p.201 – 206.

Impedance-source networks

[11] F.Z. Peng, "Z-Source Inverter," *IEEE Trans. Ind. Applicat.*, vol. 39, no. 2, pp. 504-510, Mar./Apr. 2003.

[12] J. Anderson, F.Z. Peng, "Four quasi-Z-Source inverters," *IEEE Power Electronics Specialists Conference, PESC'08*, pp. 2743-2749, 2008.

[13] F.Z. Peng, X. Yuan, X. Fang and Z. Qian, "Z-source inverter for adjustable speed drives," *IEEE Trans. Power Electron.(Letter)*, vol. 1, no. 2, pp. 33-35, June 2003.

[14] P.C. Loh, F. Gao, F. Blaabjerg, A.L. Goh, "Buck-boost impedance networks" *in Proc. of 2007 European Conference on Power Electronics and Application*s, 2-5 Sept. 2007, Aalborg. pp. 1 – 10.

[15] S. Rajakaruna, L. Jayawickrama, "Steady-state analysis and designing impedance network of Z-source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2483-2491, July 2010.

[16] Yifan Yu; Qianfan Zhang; Xiaofei Liu; Shumei Cui, "DC-link voltage ripple analysis and impedance network design of single-phase Z-source inverter" *in Proc. of 14th European Conference on Power Electronics and Applications (EPE 2011),* 2011, pp. 1 – 10.

[17] D. Sun, G. Baoming, X. Yan, D. Bi, H. Abu-Rub, F.Z. Peng, "Impedance design of quasi-Z source network to limit double fundamental frequency voltage and current ripples in single-phase quasi-Z source inverter" *in Proc. of Energy Conversion Congress and Exposition (ECCE),* 2013, pp. 2745 – 2750.

[18] F.Z. Peng, A. Joseph, J. Wang, M. Shen, L. Chen, Z. Pan, E. O. Rivera and Y. Huang, "Z-source inverter for motor drives," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 857-863, Jul. 2005.

[19] D. Vinnikov, I. Roasto, T. Jalakas, "An Improved High-Power DC/DC Converter for Distributed Power Generation," *in Proc. of 10th International Conference on Electrical Power Quality and Utilisation, EPQU'09*, pp.1-6, 15-17 Sept. 2009

[20] D. Vinnikov, I. Roasto, "Quasi-Z-Source-Based Isolated DC/DC Converters for Distributed Power Generation," *IEEE Trans. Ind. Electron.*, Vol. 58, no. 1, pp. 192-201, Jan. 2011.

[21] R. Strzelecki, D. Vinnikov, "Models of the qZ-Converters," *Przeglad Elektrotechniczny (Electrical Review)*, vol.86, no.6, pp.80-84, 2010.

[22] J. Zakis, D. Vinnikov, O. Husev, I. Rankis, "Dynamic Behaviour of qZS-based Bi-directional DC/DC Converter in Supercapacitor Charging Mode," *in Proc. of International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM'12*, pp.764-768, 20-22 June 2012.

[23] D. Vinnikov, I. Roasto, "Impact of Component Losses on the Voltage Boost Properties and Efficiency of the qZS-Converter Family," *in Proc. of 7th International Conference-Workshop Compatibility and Power Electronics, CPE'011*, pp.303-308, 1-3 June 2011.

[24] O. Husev, L. Liivik, F. Blaabjerg, A. Chub, D. Vinnikov, I. Roasto. "Galvanically Isolated Quasi-Z-Source DC-DC Converter with a Novel ZVS and ZCS Technique", *IEEE Trans. Ind. Electron.*, vol 62, no 12, pp. 7547-7556, 2015.

[25] M. Shen "Z-source inverter design, analysis, and its application in fuel cell vehicles", *PhD thesis*, Michigan State University, 2006.

[26] A.S. Khlebnikov and S.A. Kharitonov, "Application of the Z-Source Converter for Aircraft Power Generation Systems," in *Proc. EDM 2008*, pp. 211-215, July 2008.

[27] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L.M. Tolbert, D.J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress", *IEEE Trans. Industry Applic*., Vol. 42, no. 3, pp. 770-778. 2006.

[28] F.Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter", *IEEE Trans. Power Electron*., vol. 20, no. 4, pp. 833-838. 2005.

[29] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L.M. Tolbert, D.J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress", *IEEE Trans. Industry Applic*., Vol. 42, no. 3, pp. 770-778. 2006.

[30] O. Ellabban, J. Van Mierlo, P. Lataire, "Comparison between different PWM control methods for different Z-source inverter topologies", *in Proc. of 13th IEE European Conference on Power Electronics and Applications, EPE '09*, pp.1,11, 8-10 Sept. 2009.

[31] P.C. Loh, F. Gao, F. Blaabjerg, "Embedded EZ-Source Inverter," *IEEE Trans. Ind. App.*, vol. 46, no. 1, pp. 256-267, Jan./Feb. 2010.

[32] R. Strzelecki, M. Adamowicz, B. Balkowski, N. Strzelecka: "The buck-boost inverter circuit especially designed for single-stage power conversion," *PL Patent Application P386084*, Sep. 09, 2008.

[33] R. Strzelecki, M. Adamowicz, N. Strzelecka and W. Bury, "New type T-source inverter," in *Proc. CPE 2009*, pp. 191-195, May 2009.

[34] M. Adamowicz, J. Guzinski, D. Vinnikov, N. Strzelecka, "Trans-Z-source-like Inverter with Built-in DC Current Blocking Capacitors", in *Proc. CPE 2011*, pp. 137-143, June 2011.

[35] W. Qian, F.Z. Peng, and H. Cha, "Trans-Z-Source Inverters," *IEEE Trans. Power Electron* , vol. 26, no. 12, pp. 3453 – 3463.

[36] M. Adamowicz, R. Strzelecki, F.Z. Peng, J. Guzinski and H.A. Rub, "New Type LCCT-Z-Source Inverters," *in Proc. of EPE 2011*, pp. 1-10, Sept. 2011.

[37] M. Adamowicz. "LCCT-Z-source inverters" in Proc. 10th EEEIC 2011. 8-11 May 2011.pp. 1 -6.

[38] P.C. Loh, D.Li and F. Blaabjerg, "Γ-Z-Source Inverters," *IEEE Trans. Power Electron,* vol. 28, no. 11, pp. 4880-4884, Nov. 2013.

[39] M.K. Nguyen, Y. C. Lim and Y. G. Kim, "TZ-Source Inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5686-5695, Dec. 2013.

[40] M.K Nguyen, Y.C. Lim, S.J. Park "Improved trans-Z-source inverter with continuous input current and boost inversion capability*" IEEE Trans. Power Electron*. Vol. 28, No. 10, pp. 4500-4510, Oct. 2013.

[41] M.K Nguyen, Y.C. Lim, S.J. Park, Y.G. Jung. "Cascaded TZ-source inverters" *IET Power Electronics*. Vol.7, No. 8, pp. 2068 – 2080, August 2014.

[42] Y.P. Siwakoti, P.C. Loh, F. Blaabjerg and G. E. Town, "Y-Source Impedance Network," *IEEE Trans. Power Electron. (Letter)*, vol. 29, no. 7, pp. 3250-3254, Jul. 2014.

[43] W. Mo, P.C. Loh, A. Andrew, F. Blaabjerg, "Single stage buck-boost DC-AC neutral point clamped inverter", *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 318-323.

[44] W. Mo, P.C. Loh and F. Blaabjerg, "Voltage type Γ-source Inverters with Continuous Input Current and Enhanced Voltage Boost Capability," *in Proc. of 15th International Power Electronics and Motion Control Conference, EPE-PEMC 2012 ECCE Europe*, Novi Sad, Serbia, pp. 1-8.

[45] M. Zhu, Kun Yu, F.L. Luo; "Switched Inductor Z-Source Inverter," *IEEE Trans. Power Electron.*, vol.25, no.8, pp. 2150-2158, Aug. 2010.

[46] Y.P. Siwakoti, F. Peng, F. Blaabjerg, P. Loh, G.E. Town, "Impedance Source Networks for Electric Power Conversion Part-I: A Topological Review," *IEEE Trans. Power Electron.*, vol.30, no. 2, pp. 699-716, Feb. 2015.

[47] L. Yushan., H. Abu-Rub., G. Baoming. "Z-source/quasi-Z-source inverters: derived networks, modulations, controls, and emerging applications to photovoltaic conversion" *IEEE Industrial Electronics Magazine*, Vol. 8, No. 4. pp. 32-44, Dec. 2014.

[48] A. Chub, D. Vinnikov,F. Blaabjerg, F.Z. Peng "A Review of Galvanically Isolated Impedance-Source DC–DC Converters" *IEEE Trans. Power Electron.*, vol.31, no. 4, pp. 2808 - 2828, April 2016.

[49] Y.P. Siwakoti, F. Peng, F. Blaabjerg, P. Loh, G.E. Town, "Impedance Source Networks for Electric Power Conversion Part-II: Review of Control Method and Modulation Techniques," *IEEE Trans. Power Electron.*, vol.30, no. 4, pp. 1887 - 1906, April 2015.

Multilevel Inverters

[50] L.G Franquelo, J. Rodriguez, J.I. Leon, S. Kouro, R. Portillo, M.A.M. Prats, "The age of multilevel converters arrives", *IEEE Ind. Electron. Mag*., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[51] S. Kouro, M. Malinowski, K Gopakumar, J. Pou, L.G Franquelo, B. Wu, J. Rodriguez, M.A. Perez, J.I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron*., vol.57, no.8, pp.2553-2580, Aug. 2010.

[52] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives", *IEEE Trans. Ind. Electron*., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[53] J. Rodríguez, J.S. Lai, F.Z. Peng, "Multilevel Inverters: A Survey of topologies, controls, and applications", *IEEE Trans. Ind. Electron.,* vol. 49, no. 4, pp.724-738, August 2002.

[54] K.B. Lee, S.H. Huh, J.Y. Yoo, F. Blaabjerg, 'Performance improvement of DTC for induction motor-fed by three-level inverter with an uncertainty observer using RBFN', *IEEE Trans. Energy Conv.*, 2005, 20, (2), pp. 276 - 283.

[55] O. Vodyakho, C.C. Mi, 'Three-Level Inverter-Based Shunt Active Power Filter in Three-Phase Three-Wire and Four-Wire Systems', *IEEE Trans. Power Electron*., vol. 24, no. 5, pp. 1350-1363, 2009.

[56] H. Akagi, R. Kondo, 'A Transformerless Hybrid Active Filter Using a Three-Level Pulsewidth Modulation (PWM) Converter for a Medium-Voltage Motor Drive', *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1365-1374, 2010.

[57] C. Xia, X. Gu, T. Shi, Y. Yan, 'Neutral-Point Potential Balancing of Three-Level Inverters in Direct-Driven Wind Energy Conversion System', *IEEE Trans. Energy Conv.*, vol. 26, no. 1, pp. 18 – 29, 2011.

[58] M.I. Milanés-Montero, E. Romero-Cadaval, F. Barrero-González, 'Hybrid Multiconverter Conditioner Topology for High-Power Applications', *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2283-2292, 2011.

[59] J.C. Rosas-Caro, J.M. Ramirez, F.Z. Peng, A. Valderrabano, 'A DC–DC multilevel boost converter', *IET PEL*., , 3, (1), pp.129-137, 2008.

[60] H.W. Ping, N.A. Rahim, J. Jamaludin, "New Three-Phase Multilevel Inverter with Shared Power Switches", *Journal of Power Electronics*, vol. 13, no. 5, pp. 787-797, Sep. 2013.

Comparison of Topologies

[61] A. Van den Bossche, V.C. Valchev, "Inductors and Transformers for Power Electronics", Published in 2005 by CRC Press Taylor & Francis Group.

[62] T.E. Shults, O. Husev, J. Zakis "Overview of impedance source networks for voltage source inverters", *in Proc. of Micro/Nanotechnologies and Electron Devices (EDM 2015), 16th International Conference of Young Specialists, pp. 514-520*.

[63] W.T. Franke, M. Mohr, F.W. Fuchs, "Comparison of a Z-source inverter and a voltage-source inverter linked with a DC/DC-boost-converter for wind turbines concerning their efficiency and installed semiconductor power*", in Proc. of Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 1814 – 1820.

[64] M. Shen, A. Joseph, J. Wang, F.Z. Peng, "Comparison of Traditional Inverters and Z-Source Inverter Power Electronics", *in Proc. of Specialists Conference, 2005. PESC '05*., pp. 1692 – 1698.

[65] M. Shen, A. Joseph, J. Wang, F.Z. Peng, D.J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles", *Power Electronics in Transportation*, pp. 125 – 132. 2004.

[66] A. Battiston, J.P. Martin, E.D. Miliani, B. Nahid-Mobarakeh, S. Pierfederici, F. Meibody-Tabar, "Comparison criteria for electric traction system using zsource/quasi z-source inverter and conventional architectures", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 467-476, 2014.

[67] A.M. Roldan, A. Barrado, J. Pleite, J. Vazquez, E. Olias, "Size and cost reduction of the energy-storage capacitors'", *in Proc. 19th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2004, pp. 723–729.

[68] J. Biela, J.W. Kolar, "Using Transformer Parasitics for Resonant Converters—A Review of the Calculation of the Stray Capacitance of Transformers", *IEEE Trans. Ind. Appl*., vol. 44, no. 3, pp. 223-233. 2008.

[69] H. Wang; F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview", *IEEE Trans. Ind. Appl*., vol. 50, no. 5, pp. 3569 - 3578. 2014.

Modulation techniques

[70] P.C. Loh, F. Blaabjerg, S.Y. Feng, K.N. Soon, "Pulse-width modulated Z-source neutral-point-clamped inverter," *in Proc. of Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06*. 19-23 March 2006.

[71] P.C. Loh, F. Gao, F. Blaabjerg, S. Y. C. Feng and N. J. Soon, "Pulse-width-Modulated Z-Source Neutral-Point-Clamped

Inverter," *IEEE Trans. Ind. Applicat.*, vol. 43, no. 5, pp. 1295-1308, Sep./Oct. 2007.

[72] F. Gao, P.C. Loh, F. Blaabjerg and R. Teodorescu, "Modulation Schemes of Multi-Phase Three Level Z-Source Inverters," in *Proc. PESC 2007*, pp. 1905-1911, June 2007.

[73] P.C. Loh, F. Blaabjerg, C.P. Wong, "Comparative Evaluation of Pulse-Width Modulation Strategies for Z-Source Neutral-Point-Clamped Inverter," *in Proc. of 37th IEEE Power Electronics Specialists Conference, PESC '06*. 18-22 June 2006.

[74] P.C. Loh, F. Blaabjerg and C.P. Wong, "Comparative Evaluation of Pulsewidth Modulation Strategies for Z-Source Neutral-Point-Clamped Inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1005-1013, May 2007.

[75] P.C. Loh; D.G. Holmes, Y. Fukuta, T.A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Trans. Ind. Applicat.*, vol.39, no.5, pp.1386,1395, Sept.-Oct. 2003.

[76] J.H.G Muniz, E.R.C. da Silva and E.C. dos Santos Jr., "A Hybrid PWM Strategy for Z-Source Neutral-Point-Clamped inverter," *in Proc. IEEE APEC 2011*, pp. 450-456, Mar. 2011.

[77] P.C. Loh, F. Gao, F. Blaabjerg, W.L. Sok, "Operational Analysis and Modulation Control of Three-Level Z-Source Inverters With Enhanced Output Waveform Quality," *IEEE Trans. Power Electron.*, vol.24, no.7, pp.1767,1775, July 2009.

[78] F.B. Effah, P. Wheeler, J. Clare, A. Watson, "Space-Vector-Modulated Three-Level Inverters With a Single Z-Source Network," *IEEE Trans. Power Electron.*, vol.28, no.6, pp.2806-2815, June 2013

[79] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, D. Boroyevich, "A Carrier-Based PWM Strategy With Zero-Sequence Voltage Injection for a Three-Level Neutral-Point-Clamped Converter," *IEEE Trans. Power Electron.*, vol.27, no.2, pp.642,651, Feb. 2012

[80] J.H. Kim; S.K. Sul, P.N. Enjeti, "A Carrier-Based PWM Method With Optimal Switching Sequence for a Multilevel Four-Leg Voltage-Source Inverter," *IEEE Trans. Ind. Applicat.,* vol.44, no.4, pp.1239,1248, July-Aug. 2008.

[81] O. Husev, S. Stepenko, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "Single Phase Three-Level Quasi-Z-Source Inverter with a New Boost Modulation Technique," in *Proc. IECON 2012*, pp. 5852-5857, Oct 2012.

[82] C. Roncero-Clemente, O. Husev, T. Jalakas, E. Romero-Cadaval, J. Zakis, V. Mmiñambres-Marcos, "PWM for Single Phase 3L Z/qZ Source Inverter with Balanced Power Losses". *Elektronika ir Elektrotechnika*, vol. 20, no. 6, pp. 71-76, 2014.

[83] Y. Liu, Baoming Ge, H. Abu-Rub, F.Z. Peng, "Phase-shifted pulse-width-amplitude modulation for quasi-Z-source cascade multilevel inverter-based photovoltaic power system," *IET Power Electron.*, vol.7, no.6, pp.1444-1456, 2014.

[84] Y. Liu, G. Baoming, H. Abu-Rub, F.Z. Peng, "An Effective Control Method for Quasi-Z-Source Cascade Multilevel Inverter-Based Grid-Tie Single-Phase Photovoltaic Power System," *IEEE Trans. Ind. Inform.*, vol.10, no.1, pp.399-407, Feb. 2014.

[85] Y. Liu, G. Baoming, H. Abu-Rub, F.Z. Peng, "An Effective Control Method for Three-Phase Quasi-Z-Source Cascaded Multilevel Inverter Based Grid-Tie Photovoltaic Power System," *IEEE Trans. on Ind. Electron.*, vol.61, no.12, pp.6794-6802, Dec. 2014.

[86] Y. Liu, G. Baoming, H. Abu-Rub, F.Z. Peng, "A Modular Multilevel Space Vector Modulation for Photovoltaic Quasi-Z-Source Cascaded Multilevel Inverter,", *in Proc. of IEEE APEC 2013*, pp. 714-18, Mar. 2013.

[87] B.P. Mcgrath, D.G. Holmes, T.A. Lipo, "Optimized space vector switching sequences for multilevel inverters", *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293-1301, 2003.

Impedance-Source Multilevel Inverters

[88] P.C. Loh, S.W. Lim, F. Gao and F. Blaabjerg, "Three-Level Z-Source Inverters Using a Single LC Impedance Network," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 706-711, March 2007.

[89] R. Strzelecki, M. Adamowicz, D. Wojciechowski 'Buck-Boost Inverters with Symmetrical Passive Four-terminal Networks', *Proc. Compatibility in Power Electronics, 2007. CPE '07* , May 2007, pp.1-9.

[90] R. Strzelecki, W. Bury, M. Adamowicz and N. Strzelecka, "New alternative passive networks to improve the range output voltage regulation of the PWM inverters", *in Proc. of IEEE APEC*, pp. 857 -863, 2009.

[91] R. Strzelecki, D. Wojciechowski, M. Adamowicz, "Multilevel, multiphase inverter supplying by many sources, specially different voltage and non-connection sources, "*Patent Application P379977*, Jun. 19, 2006.

[92] R. Strzelecki, D. Wojciechowski, M. Adamowicz: "Principle of symmetrization of the output voltage of the multilevel inverter supplying by many different voltage sources, especially with four-terminal impedance networks," *PL Patent Application P379978*, Jun. 19, 2006.

[93] F. Gao, P.C. Loh, F. Blaabjerg, R. Teodorescu, D.M. Vilathgamuwa, "Five-level Z-source diode-clamped inverter", *IET Power Electron.,* 2010, vol. 3, no. 4, pp.500-510.

[94] P.C. Loh, F. Gao, F. Blaabjerg, "Topological and Modulation Design of Three-Level Z-Source Inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2268-2277, Sep. 2008.

[95] F. Gao, P.C. Loh, F. Blaabjerg and D. M. Vilathgamuwa, "Dual Z-Source Inverter With Three-Level Reduced Common Mode Switching," *IEEE Trans. Ind. App.*, vol. 43, no. 6, pp. 1597-1608, Nov./Dec. 2007.

[96] D. Li, F. Gao, P.C. Loh, M. Zhu and F. Blaabjerg, "Cascaded Impedance Networks for NPC Inverter," *in Proc. of IPEC, 2010,* pp. 1176-1180.

[97] A.S. Priyaa, R. Seyezhai, B.L. Mathur, "Design and Implementation of Cascaded Z-Source Multilevel Inverter", *in Proc. of Advances in Engineering, Science and Management (ICAESM), 2012 International Conference on*, 2012 , pp. 354 – 360.

[98] F. Gao, P.C. Loh, F. Blaabjerg and D.M. Vilathgamuwa, "Performance Evaluation of Three-Level Z-Source Inverters Under Semiconductor-Failure Conditions," *IEEE Trans. Ind. Applicat.*, vol. 45, no. 3, pp. 971-981, May/June 2009.

[99] P.C. Loh, F. Gao, P.C. Tan and F. Blaabjerg, "Three-Level AC-DC-AC Z-Source Converter Using Reduced Passive Component Count," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1671-1681, July 2009.

[100] M.R. Banaei, A.R. Dehghanzadeh, E. Salary, H. Khounjahan and R. Alizadeh, "Z-Source-based multilevel inverter with reduction of switches," *IET Power Electron*., vol. 5, no. 3, pp. 385-392, 2012.

[101] W. Mo, P.C. Loh, D. Li, F. Blaabjerg "Trans-z-source neutral point clamped inverter", *in Proc. of Power Electronics, Machines and Drives (PEMD 2012),* 27-29 March 2012, pp. 1-5.

[102] D. Li, P.C. Loh, M. Zhu, F. Gao, F. Blaabjerg, " Cascaded Multicell Trans-Z-Source Inverters," *IEEE Trans. Power Electron.,* vol. 28, no. 6, pp. 826– 836, 2013.

[103] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter ", *IET Power Electron.*, vol. 8, no. 1, pp. 1-10, 2015.

[104] O. Husev, C. Roncero-Clemente, E. Romero-C*adaval, D. Vinnikov, T. Jal*akas, "Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application". *Electric Power Systems Research,* vol. 130, no. 1, pp. 10–21, 2016.

[105] C. Roncero-Clemente, O. Husev, S. Stepenko, D. Vinnikov, E. Romero-Cadaval, "Output voltage control system for a three-level neutral-point clamped quasi-Z-source inverter", *Przegląd Elektrotechniczny*, no. 5, pp. 76-80, May. 2013.

[106] O. Husev, S. Stepenko, C. Roncero-Clemente, E. Romero-Cadaval, R. Strzelecki, "Experimental investigation of high frequency 3L-NPC qZS inverter for photovoltaic application", *in Proc. 39th Annual Conf. IEEE Industrial Electronics Society (IECON 2013),* Vienna, Austria, 2013, pp. 5967–5972.

[107] R. Strzelecki, M. Adamowicz, B. Balkowski, N. Strzelecka: "Multi-level inverter circuit especially for voltage boost," *PL Patent Application P386085*, March. 29, 2010.

[108] R. Strzelecki, M. Adamowicz,B. Balkowski, N. Strzelecka: "The buck-boost inverter circuit especially designed for single-stage power conversion," *PL Patent Application P386084*, Sep. 09, 2008.

[109] W. Mo, P.C. Loh, F. Blaabjerg, P.Wang, "Trans-Z-source and Γ-Z-source neutral-point-clamped inverters", *IET Power Electron*., vol. 8, no. 4, pp. 371-377, 2015.

[110] T. Shults, O. Husev, F. Blaabjerg, "Design and comparison of three-level three-phase T-source inverters" *in Proc. of Power Engineering, Energy and Electrical Drives (POWERENG),* pp. 564–569, 2015.

[111] T. Shults, O. Husev, F. Blaabjerg, "Design of Three-Phase Three-Level CIC T-Source Inverter with Maximum Boost Control in *Proc. of IEEE-IECON*, 2015, pp. 2408-2413.