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TESIS DOCTORAL

Convertidor Electrónico Reductor/Elevador para la Conexión Activa De Instalaciones Fotovoltaicas a la Red

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DOCTORAL THESIS

Buck/Boost Electronic Converter for Active Connection of Photovoltaic Installations to the Grid

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Declaration

I hereby declare that this submission is my own work and achievement for the doctoral degree at University of Extremadura, and it does not contain material which has been accepted for the award of any other academic degree or diploma of the university or other institute of higher learning.

Carlos Roncero Clemente

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Abstract

Shortage of fossil fuel and the necessity of reducing CO_2 emissions among other reasons have significantly grown the number of the inverter-based distributed generator connected to the low-voltage distribution network. Many of them interact with renewable energy sources such as photovoltaic modules and wind turbines, besides they are present in any energy storage process.

Focusing the attention on the photovoltaic systems, it has been observed that for a long time, photovoltaic inverter function was merely to inject power into the main grid with a unitary power factor but, new trends and policies propose to integrate them as active and smart devices. This current philosophy contributes to the change from the traditional and linear power systems to the smartgrid and microgrid concepts. In this way, inverters would be able to contribute to the local voltage support, improve the power quality and give rise to flexibility and security of supply.

Concurrently industry and research are aiming at cost reductions and enhanced performance of the energy conversion process, with a focus on the inverter topologies. Photovoltaic inverters are traditionally characterized by two-stage conversion process, composed by a dc-dc boost converter and the voltage source inverter. Some innovative ideas seem quite suitable for this application because they can step up the dc input voltage in a single power conversion stage by using impedance source network, quasi impedance network or its derivations. This family of converters allows among other advantages the following: voltage boost/buck, extended range of operation, low cost and high efficiency, strong electromagnetic immunity, no need for dead time, minimum number of semiconductor devices, improved reliability and performance, and short-circuit protection. Furthermore, impedance networks have been integrated with multilevel bridges to acquire their intrinsic advantages.

However, because of the relatively early stage, only few studies deal with the grid-connected integration with closed loop control systems, which basically must provide coexistence of an operation strategy of the inverter, a maximum power point tracker algorithm, a dc-link voltage control method and a special modulation technique to embed the shoot-through states into the normal ones.

This PhD research presents a novel solution for energy conversion in photovoltaic applications based on the aforementioned concepts. A new inverter topology called “three-level neutral-point-clamped quasi-impedance source inverter” both in single and

in three phase variants is proposed, analysed and calculated along a new modulation technique to generate the shoot-through states uniformly distributed during the whole fundamental period. To operate in grid-connected mode and deal with the aforementioned new trends related to the electrical systems, different closed loop operation strategies are designed and proposed as well. Taking into account these last functionalities, the proposed inverter is considered as an active device, presenting a smart behaviour in its integration with the main grid.

Resumen

La escasez de las fuentes de energía basadas en combustibles fósiles y la necesidad de reducir las emisiones de CO_2, entre otros motivos, han provocado un aumento en la conexión a las redes de distribución de baja tensión de generadores distribuidos que emplean inversores. Muchos de ellos actúan de interfaz con fuentes de energías renovables como módulos fotovoltaicos y turbinas eólicas, además de formar parte de cualquier sistema de almacenamiento de energía.

Particularizando en los sistemas de generación fotovoltaica, se observa que durante mucho tiempo y desde sus inicios, estos inversores han estado actuando básicamente mediante la inyección de potencia activa en la red, con factor de potencia unitario. Pero las nuevas tendencias de operación e incluso normativas de distintos países, proponen que estos dispositivos sean integrados como elementos más activos e inteligentes. Esta filosofía en la operación contribuye a la evolución de los tradicionales sistemas de potencia lineales hacia los conocidos conceptos de microrredes y redes inteligentes. De esta manera, los inversores contribuirían al control de tensión en el nodo a nivel local y mejorarían la calidad de la energía, además de contribuir a una mayor flexibilidad y seguridad del suministro eléctrico.

Simultáneamente a esta tendencia de operación, la industria y los grupos de investigación se han planteado como reto el reducir el coste y mejorar los rendimientos de los procesos de conversión de energía, focalizando la atención en las topologías inversoras. Los inversores fotovoltaicos tradicionales se caracterizan por contar con una doble etapa de conversión de energía, a través de un convertidor continua-continua elevador y un inversor en fuente de tensión. Algunas de las ideas innovadoras en este campo parecen muy adecuadas para aplicaciones fotovoltaicas dado que pueden elevar la tensión continua de entrada en una sola etapa de conversión a través del uso de una red impedante o alguna de sus derivadas. Esta familia de convertidores permite: elevar y reducir la tensión, dotar al convertidor de un mayor rango de operación en cuanto a tensión de entrada, menor coste y mayor eficiencia, mayor inmunidad electromagnética, ausencia de necesidad de tiempos muertos, mayor rendimiento y protección frente a cortocircuitos de rama, entre otros.

Sin embargo, dada la reciente aparición de estos convertidores, no existen demasiados estudios en cuanto a su integración como elementos conectados a la red con algoritmos de control en lazo cerrado, en los cuales deben coexistir una estrategia de operación del inversor, un algoritmo del punto de máxima potencia, un método de control del bus de

continua y una técnica de modulación especial que permita generar estados de conducción simultáneo entre interruptores de la misma rama además de los estados normales.

Esta tesis doctoral presenta una solución novedosa para la conversión de energía en sistemas fotovoltaicos teniendo en cuenta los aspectos previos. Se propone, analiza y calcula una nueva topología inversora conocida como "inversor de tres niveles con el punto neutro fijado con fuente cuasi impedante", tanto en versión monofásica como en trifásica. También se propone una nueva técnica de modulación que permite generar los estados de conducción simultánea entre interruptores de una misma rama de manera uniforme durante todo el periodo fundamental. Por último, se han desarrollado y propuesto diferentes algoritmos de control en lazo cerrado para su operación en conexión a red. Teniendo en cuenta estas últimas funcionalidades añadidas, el convertidor propuesto se considera un elemento activo, comportándose de manera inteligente en lo que respecta a su conexión y operación con la red principal.

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Nomenclature

- a - mathematical operator for *abc* to α-β transformation
- ac - alternating current
- A_{ac} - amplitude of y_{ac}
- A_{dc} - amplitude of x_{dc}
- ANPC - Active NPC
- APF - Active power filter
- APOD - Alternative Phase Opposition Disposition
- B - Boost factor
- CCM - Continuous Conduction Mode
- C_f - Capacitance of the output filter
- CHB - Cascaded H-Bridge
- C_i – Capacitor
- CMC - Cascade Matrix Converter
- CPWM - Continuous Pulse Width Modulation
- CSI - Current Source Inverter
- C_{st} - ST carrier
- D_A - duty cycle of the active states
- dc - direct current
- DCLC - DC-Link Cascaded
- DCM - Discontinuous Conduction Mode
- D_i - General diode
- DG - Distributed Generator
- DPWM - Discontinuous Pulse Width Modulation
- DPWMMAX - Discontinuous Pulse Width Modulation that the MAXimum signal defines the zero sequence
- DPWMMIN - Discontinuous Pulse Width Modulation that the MINimun signal defines the zero sequence
- D_s - Shoot-through Duty Cycle
- D^*_s – Reference Shoot-through Duty Cycle
- D_Z - duty cycle of the zero states
- $\bar{D}_s$ - Average D_s
- EI - Edge Insertion
- ESS - Energy Storage System
- f - frequency

- FB - Full Bridge
- FC - Flying Capacitor
- f_{res} - resonance frequency
- f_{sw} - switching frequency
- f_1 - line frequency
- G - Voltage gain
- GTO - Gate Turn-Off Thyristor
- H-NPC - Neutral-point-Clamped and H-Bridge
- h_{sw} - switching harmonic order
- HV-IGBT - High Voltage IGBT
- IGBT - Isolated Gate Bipolar Transistor
- IGCT - Integrated Gate-Commutated Thyristor
- InC - Incremental Conductance
- I^*_{grid} - Reference grid current
- I_{sc} - Short circuit current
- I_{MPP} - Maximum power point current
- I_{OUT} - Output current
- I_d - d component of the output current
- I^*_d - d component of the reference output current
- I_q - q component of the output current
- I^*_q - q component of the reference output current
- I_{pv} - Photovoltaic current
- i_a - output current
- i_{Ci} - instantaneous current across a capacitor
- $i_{DC\sim}$ - Output current at low frequency
- i_{DC_Max} – Peak value of the output current at low frequency
- $i_{grid}(t)$ - instantaneous injected current
- $\vec{i}_{grid}$ - Reference injected current vector to the grid
- i_{in} - input current
- $i_{L1\sim}$ - ac component of the input current
- $\hat{i}_{Li\sim}$ - peak value of the current in the inductance
- k - number of output voltage level
- K_{C1} - voltage ripple factor in C_1
- K_{C2} - voltage ripple factor in C_2
- K_{CL1} - Low frequency voltage ripple factor for capacitors C_1 and C_4
- K_{CL2} - Low frequency voltage ripple factor for capacitors C_2 and C_3
- K_L - Predefined ripple in the inductor current
- K_{LH1} - High switching frequency current ripple factor
- K_{LL1} - Low frequency input current ripple factor
- K_{LL2} - Low frequency current ripple factor for inductors L_2 and L_4
- K_i - Integral constant of PI controller
- K_p - Proportional constant of PI controller

- L - weighted inductance
- LCCT-qZSN - Inductor–Capacitor–Capacitor–Transformer qZSN
- LCI - Load Commutated Inverter
- L_f - Inductance of the output filter
- L_g - grid inductance
- L_i - Inductance i
- L_{i} - inverter inductance
- m_f - frequency modulation index
- M - Modulation index
- MBC - Maximum Boost Control
- MCBC - Maximum Constant Boost Control
- ML - MultiLevel
- MLI - MultiLevel Inverter
- MMC - Modular Multilevel Inverter
- MOSFET - Metal Oxide Semiconductor Field Effect Transistor
- MPP - Maximum Power Point
- MPPT - Maximum Power Point Tracking
- $\mathrm{MR_i}$ - Modified reference signal
- MToe - Million Tonnes of oil equivalent
- MTBF - Mean Time Between Failures
- MTTF - Mean Time to Failures
- n - turns ratio
- N - Number of cascaded impedance networks
- NPC - Neutral-Point-Clamped
- NPC-CHB - Neutral-Point-Clamped and Cascaded H-Bridge
- $\mathrm{N_p}$ - Parallel connected PV panels
- $\mathrm{N_s}$ - Series connected PV panels
- NTV - Nearest Three Vector
- P - Active power
- $P^{(g)}$ - Generated active power
- PCC - Point of Common Coupling
- PD - Phase Disposition
- PI - Proportional-integral controller
- P_{IN} - Input power
- POD - Phase Opposition Disposition
- P_{OUT} - Output power
- PSC - Phase Shifted Carrier
- PV - Photovoltaic
- PWM - Pulse-Width-Modulation
- P^* - Reference Active Power
- P&O - Perturb and Observe
- qZSI - quasi-Impedance-Source Inverter
- qZSN - quasi-Impedance-Source-Network

- Q - Reactive power
- $Q^{(g)}$ - Generated reactive power
- Q^* - Reference Reactive Power
- r - index that relates L_g and L_i
- R - resistance
- R_f – resistance of the L filter
- RCM - Reduced Common Mode
- REC - Reduced Element Count
- $\mathrm{Ref_i}$ - Reference signal i
- RES - Renewable Energy Sources
- $\mathrm{R_G}$ - Gate Resistor
- S - Apparent power
- SBC - Simple Boost Control
- SHE - Selective Harmonic Elimination
- SIDER - Smart Inverter for Distributed Energy Resources
- SL-qZSN - Switched Inductor quasi-Impedance-Source-Network
- ST - Shoot-Through switching states
- S_{Ti} - Binary gate signal of T_i
- S_{Tx} - Binary gate signal of top switch of branch x
- SVC - Space Vector Control
- SVPWM - Space Vector PWM
- t_A - time duration of the active states
- t_S- time duration of the shoot-through states
- t_Z - time duration of the zero states
- T - Temperature
- T - fundamental period
- $\mathrm{T_i}$ - Constant time of the integral controller
- $\mathrm{THD_I}$ - current Total Harmonic Distortion
- $\mathrm{THD_U}$ - voltage Total Harmonic Distortion
- THIPWM - Sinusoidal PWM with the Third Harmonic Injection
- T_i - General semiconductor switch
- T_0 - ST time interval
- TPES - Total Primary Energy Supply
- Trans-qZSN – qZSN with two coupled inductor
- T_{sw} - switching period
- $\mathrm{T_{on}}$ - Conduction time in semiconductor
- T_{sw} - Switching period
- $\vec{u}$ - unitary vector in direction of $\vec{V}_{ab}$
- u_{cmv} - common mode voltage
- $\vec{u}_d$ - unitary vectors in the d direction
- $\vec{u}_q$ - unitary vectors in the q direction

- v^*_{ab} - Reference output voltage between branches
- v_{ab} - output voltage between branches
- v_{ao} - output voltage between middle point of branch *a* and neutral point
- $v_{a,ref}$, $v_{b,ref}$ and $v_{c,ref}$ - References or modulating signals
- $v_{gen}(t)$ - instantaneous generator voltage
- $v_{pcc}(t)$ - instantaneous PCC voltage
- v_{Li} - instantaneous voltage across an inductance
- v_n - bottom ST envelope
- v_{n1} - First bottom ST envelope in MCBC
- v_{n2} - Second bottom ST envelope in MCBC
- v_p - upper ST envelope
- v_{p1} - First upper ST envelope in MCBC
- v_{p2} - Second upper ST envelope in MCBC
- v_{xn} - output voltage between middle point of branch and neutral point of the load
- V_{AB} - average output voltage between branches
- $\vec{V}_{ab}$ - Reference output voltage vector of the fundamental component in terminals of the 3L-NPC-qZSI
- V^*_{ab} - Reference RMS output voltage of the fundamental component in terminals of the 3L-NPC-qZSI
- V^*_c – reference value of the dc link voltage
- V^*_d - *d* component of the reference output voltage
- V^*_q - *q* component of the reference output voltage
- $\vec{V}_L$ - Reference voltage drop vector in the filter inductance
- V^*_L - Reference RMS voltage drop in the filter inductance
- V^*_R - Reference RMS voltage drop in the resistance of the filter inductance
- $\vec{V}_R$ - Reference voltage drop vector in the resistance of the filter inductance
- $\vec{V}_{grid}$ - Voltage grid vector
- V_{Ci} - average voltage across the capacitors over one switching period
- V_{dc} - dc voltage source
- V_g - *RMS* grid voltage value
- V_{gen} - RMS voltage at the terminal of generator
- V_i (h_{sw}) - output voltage at the switching frequency
- V_{inv} - RMS fundamental component of line-to-neutral inverter voltage
- V_{IN} - input voltage source
- V_{Li} - average voltage across an inductance
- V_{MPP} - Maximum power point voltage
- V_{oc} - Open Circuit Voltage
- V_{pv} - Photovoltaic voltage

- V^*_{pv} - Reference photovoltaic voltage
- V_{pcc} - RMS voltage at the PCC
- $v_{pcc,i}$ - instantaneous voltage at the PCC in phase i
- V_{OUT} - Output voltage
- V_s - Boosted voltage
- VSI - Voltage Source Inverter
- V2G - Vehicle to Grid
- $\hat{v}_{ac}$ - peak value of the phase-to-neutral output voltage
- $v_{Ci\sim}$ - ac voltage component of the capacitor i
- $\hat{v}_{C1\sim}$ - peak value of the ac voltage component of the capacitor i
- W - Solar irradiance
- x_{dc} - dc variable
- y_{ac} - ac variable
- Z_{gen} - Reactance of the generator
- ZSI - Impedance-Source Inverter
- ZSN - Impedance-Source-Network
- ΔV_{c1} - Voltage ripple in C_1
- ΔV_{c2} - Voltage ripple in C_2
- δ - Angle between V_{gen} and V_{pcc}
- θ - phase
- θ_{grid} - Grid phase
- ω_1 - fundamental pulsatance
- 2L - Two-Level
- 3L - Three-Level
- 3L-NPC-qZSI - Three-Level Neutral-Point-Clamped quasi-Impedance-Source Inverter

Chapter 1
Introduction

1.1 Photovoltaic energy injection into the grid

World Total Primary Energy Supply (TPES) was 13555 Million Tonnes of oil equivalent (MToe) in 2013, where its 13.5 % (1829 MToe) was generated from Renewable Energy Sources (RES) as Fig. 1.1 a) represents. Solid biofuels (excluding wastes) is the largest renewable energy source, representing 10.4 % of world TPES and 73.4 % of global renewables supply as Fig. 1.1 b) depicts. Hydroelectric power is the second largest source, providing 2.5 % of world TPES and 17.8 % of renewables. Geothermal, liquid biofuels, biogases, solar, wind, and tide each represent a smaller share and make up the rest of the renewable energy supply. Growth of solar photovoltaic and wind power have been especially high during the last years, which grew at average annual rates of 46.6 % and 24.8 %, respectively (see Fig. 1.2) [1].

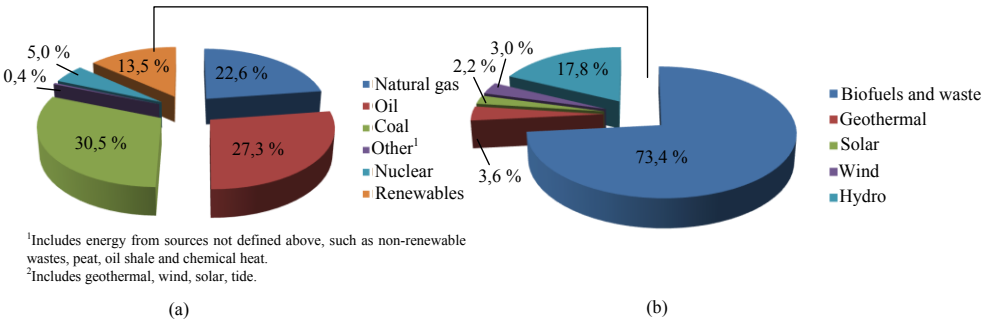


Fig. 1.1. a) 2013 fuel shares in world total primary energy supply. b) 2013 product shares in world renewable energy supply.

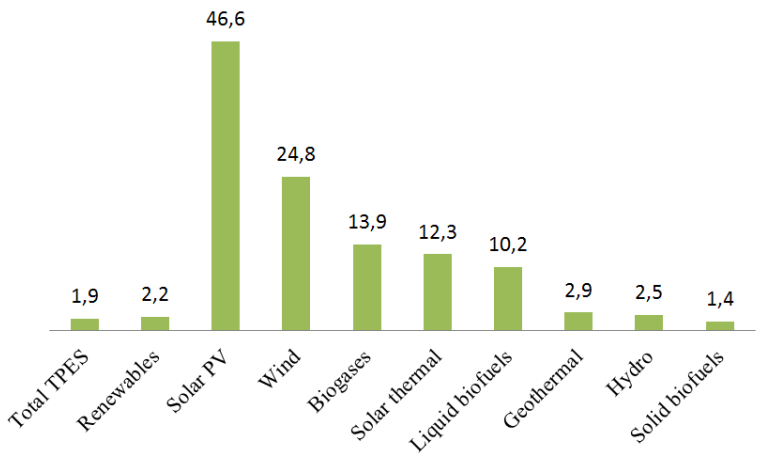


Fig. 1.2. Annual growth rates of world renewable supply from 1990 to 2013.

Lack of conventional energy sources and concern about environmental pollution are some of the reasons of this significant growth. As an important challenge, the target of the European Union is to reach 20 % of energy production by RES in 2020.

In the case of photovoltaic (PV) energy we can distinguish between grid-connected system and off-grid installation. In the first case, there are several possible typologies according to the inverter configuration (central, string or module), to the number of energy conversion stages and to the existence of transformer: transformer-based (at the high or at the low frequency side) or transformer-less. Fig. 1.3 schematically shows grid-connected photovoltaic installations.

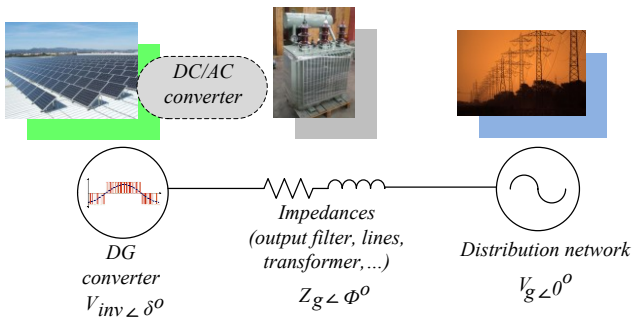


Fig. 1.3. General scheme of a grid-connected photovoltaic system.

The photovoltaic inverter is the key element in grid integration of PV systems because it enables the efficient and flexible interconnection of different elements to the electric power system. Aforementioned reasons have produced a fast rise in the number of inverter-based Distributed Generators (DG) connected to the low-voltage distribution

network. Hence the inverter will be a major player in future distributed power system scenarios based on smartgrid and microgrid concepts.

For a long time, PV inverters' function was merely to inject power into the main grid with a unitary power factor as the control reference [2] but, under new trends and policies for PV plants, they are integrated as active and smart devices. In this way, PV inverters would be able to contribute to the local voltage support, to improve the power quality and to give rise to flexibility and security of supply. Some of those new demands for inverters are power flow controls [3], voltage level restoration at the Point of Common Coupling (PCC) [3]-[5], active filtering capabilities [5], integration with energy storage systems [6] and communications compatibilities [7].

Due to the high cost of solar energy (although the cost of PV panels have dropped during 2008 by around 40 % to levels under € 2/W), industry and research are aiming at cost reductions and enhanced performance of the energy conversion process, with a focus on the inverter topologies. The inverter is traditionally characterized by two-stage converters composed by a dc-dc boost converter and the Voltage Source Inverter (VSI) but, innovative ideas in terms of inverter circuitries have emerged during the last years. Some of them seem quite suitable for PV applications because they can step up the dc input voltage in a single power conversion stage by means of shoot-through (ST) switching states. They are known as Z-Source Inverters (ZSI) [8], quasi-Z-Source Inverters (qZSI) [9] and its derivations [10]. The ZSI/qZSI fulfils buck/boost capability in single-stage topology and overcomes the limits of traditional VSIs. Hence, high reliability, high efficiency, large operation range and low cost can be achieved.

Furthermore, ZSI family has been integrated with multilevel inverter (MLI) bridges [11] to acquire their intrinsic advantages such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased dv/dt, better harmonic performance, soft switching possibilities without additional components and higher switching frequency due to lower switching losses, among others.

However, because of the relatively early stage, only few studies deal with the grid-connected integration with closed loop control systems, which basically must provide coexistence of an operation strategy of the inverter, a Maximum Power Point Tracking (MPPT), a dc-link voltage control method and a special modulation technique to embed the shoot-through states into the normal ones.

1.2 Thesis motivation

This thesis is a part of the research project dealing with the development of new concept of photovoltaic inverters called "Smart Inverter for Distributed Energy Resources (SIDER)", launched in 2006 by University of Extremadura. This project, supported by the Spanish Government, was divided into three subprojects that were carried out by the University of Extremadura, University of Córdoba and University of Cádiz. The different subprojects dealt with subjects regarding power control and quality through

the power electronic devices, communication between different grid-connected devices to develop new protection systems (special mention is on islanding detection) and signal processing for the detection and characterization of disturbances.

Focusing on the subproject developed by University of Extremadura, attention was paid in the design and development of an inverter with the necessary topology, elements, control strategy, tracking technique and switching signal generation to provide this new equipment with the characteristic to become a SIDER. It is interesting to highlight two main functionalities that were implemented: 1) control of the voltage at the point of common coupling (both the fundamental component and the harmonics) and 2) generation planning, trying to change the consideration of the power plant from non-manageable to quasi-manageable (by using energy storage system).

During the development of this project, the possibility of getting a strategic collaboration with Tallinn University of Technology raised up in 2012, with the main objective of exploring new inverter topologies devoted to photovoltaic applications since the cost reduction and enhanced performance of the energy conversion process are requested. These specific research activities were supported by the project SIDER (TEC2010-19242-C03.01) and the grant (BES-2011-043390) from the Ministry of Economy and Competitiveness from Spain, the project (SF0140016s11) and the grants (ETF8538 and ETF8687) from Estonian Ministry of Education and Research and the grant (COST ACTION MP1004) from European Union.

From the technical point of view, this research lies in the new single stage inverter topologies, suitable for PV applications since they have intrinsic advantages. In the project SIDER the solution was based on a traditional topology, hence new and further functionalities would appear. As a result, a new topology called “Three-Level Neutral-Point-Clamped quasi-impedance Source Inverter” (3L-NPC-qZSI) both in single phase and in three phase systems is proposed and validated experimentally, trying to get the advantages of both qZS Networks (qZSN) and multilevel bridges. Besides a new modulation technique to generate the Shoot-Through (ST) switching signals and different control strategies are investigated to increase the overall performance of the photovoltaic energy conversion process.

1.3 Objectives of the thesis

The main goal of the PhD research is to develop a new single stage inverter topology for PV applications, its modulation technique and control algorithms to improve the traditional solutions.

The objectives of the PhD research are classified into two categories: general (related to the PhD student education) and specific ones (related to the topic of dissertation):

General objectives

- To go in depth and to extend the acquired knowledge during the development of the SIDER project.
- To maintain and to reinforce the research collaboration with foreign universities.
- To increase the skills and experience of the PhD student and his research group.
- To generate new useful knowledge and to publish the results in specific journals.
- To share the new developments and proposals to the industry.
- To define directions for future research and international research projects.

Specific objectives

- To analyse and classify the current state-of-the-art and trends both in single stage buck/boost multilevel inverters and in their modulation techniques.
- To propose, to size and to validate a new single stage buck/boost multilevel inverter and a new modulation technique.
- To develop different control strategies for this new inverter for photovoltaic applications in grid-connected mode for it to behave as an active device.

1.4 Structure of the thesis

The framework of this PhD thesis is divided into 5 chapters and 1 appendix.

Chapter 2 summarizes and covers the different alternatives of the VSI topologies. Starting from the different basic two-level traditional solutions for single phase and three-phase applications, the review and description of the two-level inverter based on impedance-Source-Network (ZSN), qZSN and its derived network are presented with the focus of the boost operation in a single stage. Subsequently some of the well-known multilevel bridges are classified and presented, in order to identify their main features and advantages such as an improved quality of the voltage waveform and the optimization of the power switches among others. Then, a deep review of the multilevel buck/boost inverter reported in the literature is described because they inherit the advantages of inverters based on ZSN and multilevel configurations. Finally and starting from the aforementioned basis, it is possible to test the new proposed 3L-NPC-qZSI. The passive element sizing in both the power switching devices and the output filter are explained to demonstrate how the prototypes were assembled.

Chapter 3 deals with the basics of the switching signal generation or modulation techniques. At the beginning, the traditional sinusoidal Pulse-Width-Modulation (PWM) or carrier based methods for two-level single-phase and three-phase VSIs are described. In this last case the continuous and discontinuous pulse-width-modulation are distinguished, depending on the zero sequence voltage. Then, a classification of multilevel

modulation methods as extension of the two-level is depicted. Right after it, the most common modulation techniques oriented to two-level inverter based on ZSN are explained. These ones have a main particular feature, an additional state called the shoot-through state, which produces the simultaneous conduction of switches of the same phase branch to boost the input voltage. According to the voltage gain or boost factor, the simple boost control, the maximum constant boost control and the maximum boost control are compared. Finally, a deep and updated review of the modulation methods for multilevel impedance source inverters (based on sinusoidal pulse-width-modulation or space vector modulation) allows understanding the new proposed techniques both in single phase and in three phase configuration. Their principle of operation is explained in detail and experimentally validated.

Chapter 4 is intended to the operation strategies for performing grid-connected active functions for the new proposed "three-level neutral-point-clamped quasi-impedance source inverter". Based on mature control strategies for traditional grid-connected inverters, several new control strategies based on closed control loops along with different dc-link voltage control loops have been developed and explained. The first operation functionality is devoted to regulate the injected active and reactive power into the electrical grid, where different approaches were taken into account as well as the maximum power point tracking algorithm. Then its integration with energy storage system is presented and discussed for a better management of the active power between the photovoltaic plant, the storage system and the grid. Finally the capability of this new inverter to develop active filtering functions is studied, and a new control strategy is derived from the traditional approaches.

Chapter 5 summarizes the key results that have been obtained during the research and the possible continuations or future research works are highlighted.

Since the PhD is based on the different papers that the author has published, Appendix contains the book chapters, journal papers and conference contributions directly connected to the topic of dissertation and they are considered as an extension or continuation of the different chapters. Some special citations to these publications are remarked during the chapters, providing further details about this PhD research.

1.5 Results, novelties and dissemination

This section presents the most important findings obtained during the PhD research. As main scientific novelties, the following ones are highlighted:

- Analysis of the current state-of-the-art of the multilevel buck/boost inverter topologies.
- Analysis of the current state-of-the-art of the multilevel buck/boost inverter modulation techniques.

- Proposal, validation and assembly of a new topology for this family of converters, called "three-level neutral-point-clamped quasi-impedance source inverter" in single phase and three-phase version.
- Development and validation of new modulation techniques for this family of inverters that generate the traditional switching states and the ST states.
- Proposal and validation of new maximum power point tracking algorithms for this system.
- Development and proposal of new operation strategies based on different control variables to deliver active power and reactive power regulation and active filtering capabilities for this new inverter, to integrate it as active device into the electrical grid, along with dc-link voltage control methods.

The results obtained during the PhD research have been reported at 2 book chapters and published in 14 journal papers, in 15 international conferences and in 8 national conferences. 11 of the journal papers are published in journals included in the JCR list. The conference contributions were peer-reviewed and the majority of them are available in IEEE database. The most important papers directly connected to the topic of this PhD are listed and added in the Appendix. In addition, one co-authored patent application was submitted to the European patent office.

Concurrently, in terms of international collaboration of the University of Extremadura, this coordinate research has permitted the mobility and cooperation between different members of the group that the author belongs to, and members of Tallinn University of Technology (Estonia) and Aalborg University (Denmark) besides other European universities and institutions. It has also helped to apply for new collaborative and international projects in different calls for future research and development.

Chapter 2
Three-Level Neutral-Point-Clamped qZSI Topology

2.1 Introduction

Power electronic converters that change dc voltages and currents to ac waveforms are known as inverters. Their main objective is to build, from one or multiple dc power supplies, an ac switched pattern output waveform, with a fundamental component with adjustable phase, frequency and amplitude to deal with a certain application. This concept is represented in Fig. 2.1, for a generic dc variable x_{dc}, normally current or voltage. A_{dc} represents a constant amplitude of x_{dc}. In the other side, A_{ac}, f and θ are the adjustable amplitude, frequency and phase of the fundamental component of the switched ac variable (y_{ac}). This procedure is achieved by the proper control of the static power switches that interconnect the dc source to the ac load/grid, using the different configurations or conduction states provided by a certain topology.

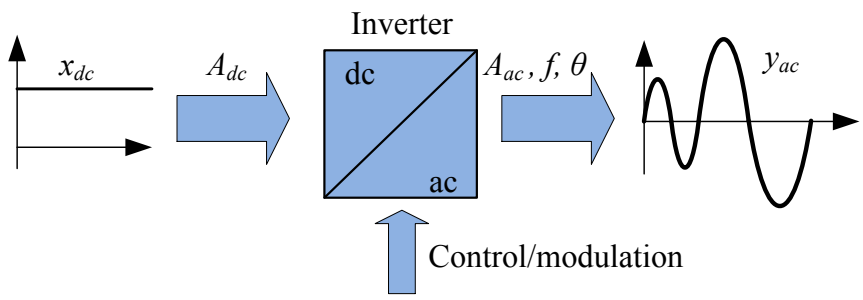


Fig. 2.1. Principle of operation of an inverter.

The dc power supplies can be either current or voltage sources, dividing the inverter family into two main traditional groups: current source inverter (CSI) and VSI, as depicted in Fig. 2.2. This figure also classifies the different type of CSI and VSI topologies depending on their power range of application. On the one hand, CSI have dominated the medium-voltage high-power range with the PWM-CSI and the load-commutated inverter (LCI) [12]. On the other hand, VSIs are widely found in low-and medium- power applications with single-phase and three-phase two-level VSI. Finally, VSI has been also proposed as an attractive solution in the medium-voltage high-power range by means of multilevel topologies [13].

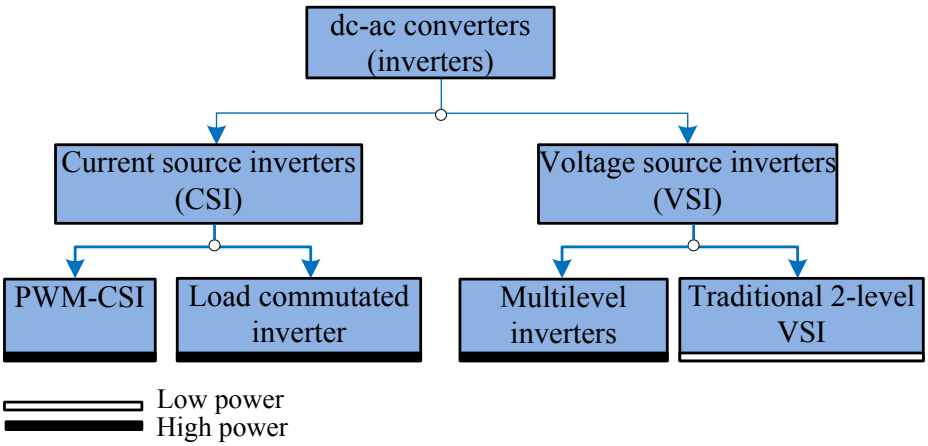


Fig. 2.2. Inverter topology traditional classification.

2.2 Two-level traditional VSI topologies

2.2.1 Single phase

Fig. 2.3 represents the half bridge, a) with IGBT and b) with MOSFET, considered as the basic two-level single-phase inverter. It is composed by one inverter leg or branch, containing two semiconductor switches (T_1 and T_2) and two freewheeling diodes (D_1 and D_2) to provide a negative current path through the switch when necessary. It also includes two capacitors to split the total dc link voltage and to provide a 0 V midpoint for the load (also known as neutral point). The load is connected between this node and the inverter leg output phase node *a*. *P* and *N* denote the positive and negative bus bars respectively. The dc voltage source (a battery, fuel cell, rectifier, PV panel, etc.) is represented by V_{dc}.

The switches are controlled by binary gate signals (S_{T1} and S_{T2}) which can be 1 or 0, that represent the "on" or "off" state respectively. This control must be alternate to avoid simultaneous conduction of T_1 and T_2 since it would short-circuit the dc link. With a simple reasoning, it is easy to understand the deduced information in Table 2.1.

The fact that there are only two possible output voltages is why this VSI is known as two-level inverter.

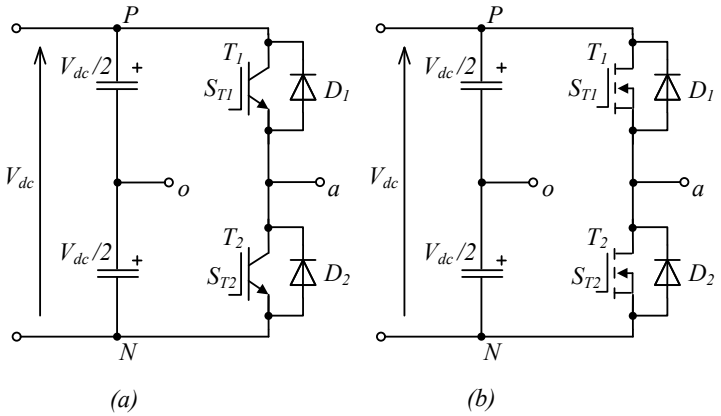


Fig. 2.3. a) Half-bridge inverter topology with IGBT. b) With MOSFET.

Table 2.1. Half-bridge switching and conduction states.

Switching state	**Gate signal (S_{T1})**	**Output voltage (v_{ao})**	**Conduction state**	**Output current (i_a)**	**Semiconductor conducting**
1	1	$V_{dc}/2$	(a)	< 0	D_1
			(b)	> 0	T_1
2	0	$-V_{dc}/2$	(c)	> 0	D_2
			(d)	< 0	T_2

Other important feature to mention is that the commutation of a power devices is not instantaneous, hence a dead time has to be included before a switch-on, to avoid a simultaneous conduction between both switches. This dead time is just a little bit larger than the switch-off commutation (for IGBT, this values is around two micro seconds).

Although S_{T1} is a binary signal that generates two different states, there will be four different conduction states depending on the current polarity, which determines whether the power switches or the diodes are conducting. The four conduction states are represented in Fig. 2.4, where a hypothetical ac square-wave operation of the inverter feeding an inductive load is considered. Note that it does not illustrate a real current waveform for such voltage.

For semiconductor sizing considerations, while not conducting, the power switch is blocking the total V_{dc}. Therefore, this topology is more common in applications in the low voltage range.

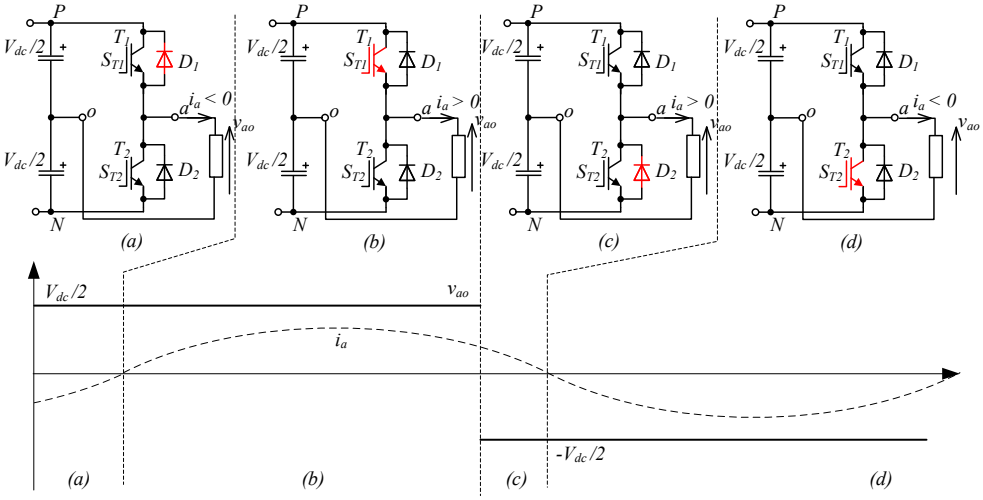


Fig. 2.4. Half-bridge inverter conduction states when a) $v_{ao} = V_{dc}/2$ and $i_a < 0$, b) $v_{ao} = V_{dc}/2$ and $i_a > 0$, c) $v_{ao} = -V_{dc}/2$ and $i_a > 0$ and d) $v_{ao} = -V_{dc}/2$ and $i_a < 0$.

Other alternative single-phase topology is the H-bridge VSI (also known as full-bridge). Basically it is composed by two half-bridge inverter legs in parallel connection to provide two output nodes *a* and *b*, to connect the load between them (as Fig. 2.5 shows). For this reason, the midpoint in the dc link is no longer necessary, hence just one capacitor is required.

Since this inverter is controlled with two complementary binary signals (S_{T1} and S_{T2}, S_{T3} and S_{T4}), it generates $2^2 = 4$ different switching states, which are illustrated in Fig. 2.6, and an arbitrary switching pattern is produced. Possible output voltage values and switching states are summarized in Table 2.2.

A general expression for the output voltage is:

$$v_{ab} = (S_{T1} - S_{T3})V_{dc}, \quad S_{Ti} \in \{0,1\}\,. \tag{2.1}$$

Note that there are two switching combinations that generate both a zero voltage level. This feature is known as redundancy, which can be used for other purpose since it does not affect the voltage applied to the load.

Likewise in the previous topology, each power switch is blocking the total V_{dc} when not conducting. Therefore, like in the previous case, this topology is also limited to low voltage range. Nevertheless, the H-bridge can be used as a basic module for larger multilevel converters, with more voltage levels, suitable for medium-voltage applications [14].

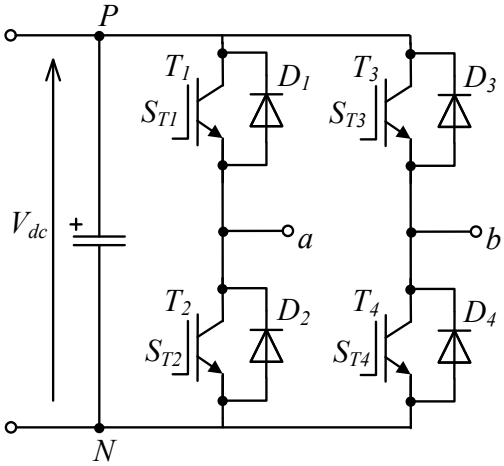


Fig. 2.5. H-bridge inverter power circuit (IGBT based).

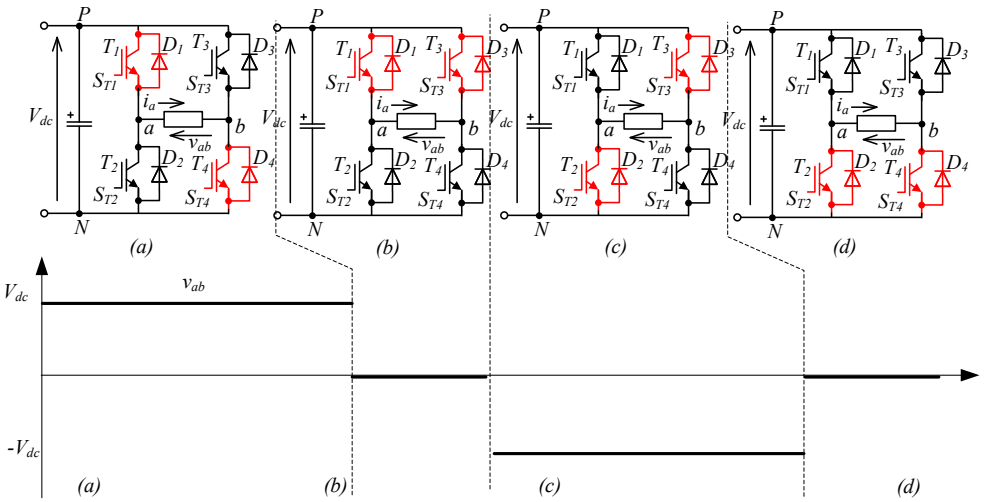


Fig. 2.6. H-bridge switching states. a) $v_{ab} = V_{dc}$, b) $v_{ab} = 0$, c) $v_{ab} = -V_{dc}$ and d) $v_{ab} = 0$.

Table 2.2. H-bridge switching states.

Switching state	**Gate signal (S_{T1})**	**Gate signal (S_{T3})**	**Output voltage**
1	1	*0*	V_{dc}
2	1	1	0
3	0	1	$-V_{dc}$
4	0	0	0

2.2.2 Three phase

The three-phase VSI is built with three paralleled inverter legs, as the same as shown before for the half- and-H bridge, as depicted in Fig. 2.7. It has a similar operation. Each inverter branch has its own binary and complementary signal for identical reasons. The inverter phase output voltages can be obtained by

$$v_{xN} = S_{Tx} V_{dc}, \quad S_{Ti} \in \{0,1\}, \quad x = a,b,c.. \tag{2.2}$$

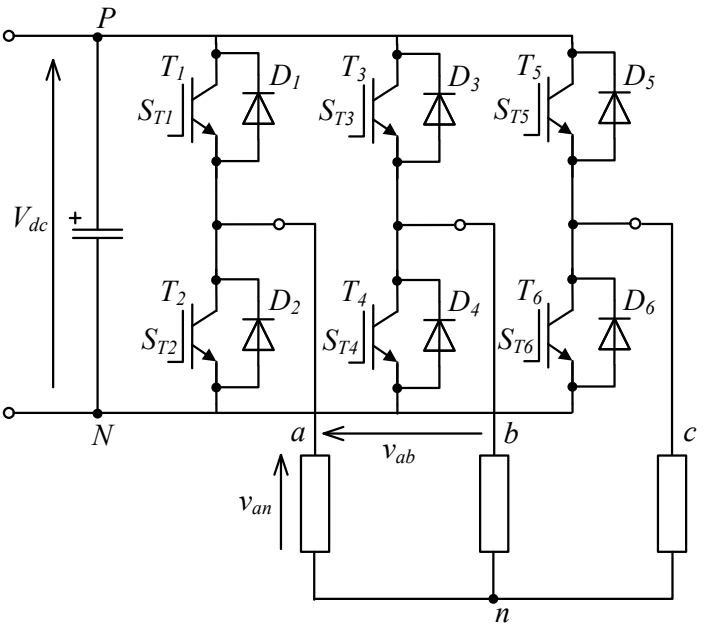


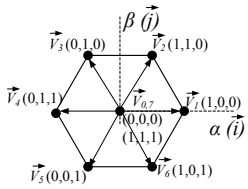
Fig. 2.7. Full-bridge three-phase VSI topology (with Y-connected load).

Since this topology is controlled with three binary signals, 2^3=8 different states are possible. They are listed in Table 2.3, where both the corresponding phase output voltage and the space vectors have has been included along their representation in the *α-β* complex plane. Each voltage reference vector can be computed and the resulting vector is mapped in this *α-β* complex plane as

$$V_i = \frac{2}{3} V_{dc} \left[S_{T1} + a S_{T3} + a^2 S_{T5} \right], \; a = -\frac{1}{2} \vec{i} + \frac{\;}{2} \vec{j}. \tag{2.3}$$

As main feature, this configuration produces a switched ac waveform between 0 and V_{dc}, unlike the previous single-phase inverters, where the output voltage is ± V_{dc}/2. Therefore the three-phase inverter has a dc component equal to V_{dc}/2. However this dc offset is common to the three phases hence, due to the connection, it does not appear in the line to line and load voltage values.

Table 2.3. Two-level three-phase VSI switching states.

	Gate signal (S_{Ti})			**Output voltage**			**Space vector**	**Representation in α-β complex plane**
	S_{T1}	S_{T3}	S_{T5}	v_{an}	v_{bn}	v_{cn}		
1	0	0	0	0	0	0	$\vec{V}_0 = 0$	
2	1	0	0	V_{dc}	0	0	$\vec{V}_1 = 2/3\, V_{dc}$	
3	1	1	0	V_{dc}	V_{dc}	0	$\vec{V}_2 = 2/3\, V_{dc} e^{j(\pi/3)}$	
4	0	1	0	0	V_{dc}	0	$\vec{V}_3 = 2/3\, V_{dc} e^{j(2\pi/3)}$	
5	0	1	1	0	V_{dc}	V_{dc}	$\vec{V}_4 = -2/3\, V_{dc}$	
6	0	0	1	0	0	V_{dc}	$\vec{V}_5 = 2/3\, V_{dc} e^{j(4\pi/3)}$	
7	1	0	1	V_{dc}	0	V_{dc}	$\vec{V}_6 = 2/3\, V_{dc} e^{j(5\pi/3)}$	
8	1	1	1	V_{dc}	V_{dc}	V_{dc}	$\vec{V}_7 = 0$	

While not conducting, each power switch blocks the total V_{dc}, hence this topology is restricted to low-voltage applications as well, and it is currently the dominating topology in industry environments at this voltage level. Nevertheless, HV-IGBT, GTO, and IGCT-based inverters or inverters with several IGBTs in series (for higher voltage) or in parallel (for larger current), have made this topology also available in medium and high voltage applications. In this context, this topology has the main drawbacks of high voltage derivatives (*dv*/*dt*), and larger switching losses produced by high switching frequency. To solve this, special modulation techniques have been proposed in the literature.

Finally, it should be remarked that multi-phase converters are built adding new paralleled inverter legs to this topology. Multi-phase system for variable speed drives have become very attractive in some applications (locomotive, military, electric ship propulsion among others) due to higher power capability and improved reliability (fault-tolerant systems) [15].

2.3 Two-level ZS dc/ac converter topologies

VSIs can just operate in buck mode and, in PV applications among others, voltage boost operation requires an additional dc/dc boost converter in the input stage, which makes the overall system more costly and harder to control. To obtain buck and boost performance the focus is turned into a ZSI and qZSI in this section. The ZSI and qZSI were firstly introduced in [8] and [9] respectively. Both topologies can buck and boost dc-link voltage in a single stage without additional power switches.

The ZSI/qZSI can boost the input voltage in a single stage, by introducing a special ST switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the dc-link capacitors. However, the ZSI/qZSI has excellent immunity against the cross conduction of top and bottom-side inverter switches. The possibility of using ST eliminates the need for dead-times without having the risk of damaging the inverter circuit. The input voltage is regulated only by adjusting the ST duty cycle (D_s). In addition, the qZSI has a continuous conduction mode (CCM) in the input current (input current never drops to zero), which makes it especially suitable for renewable energy sources (e.g. fuel cells, solar energy, wind energy, etc.).

The basic ZSN and qZSN are composed by two inductor (L_1 and L_2), two capacitors (C_1 and C_2) and one diode (D_1), which decouple the dc-link, as Fig. 2.8 a) and b) depict respectively.

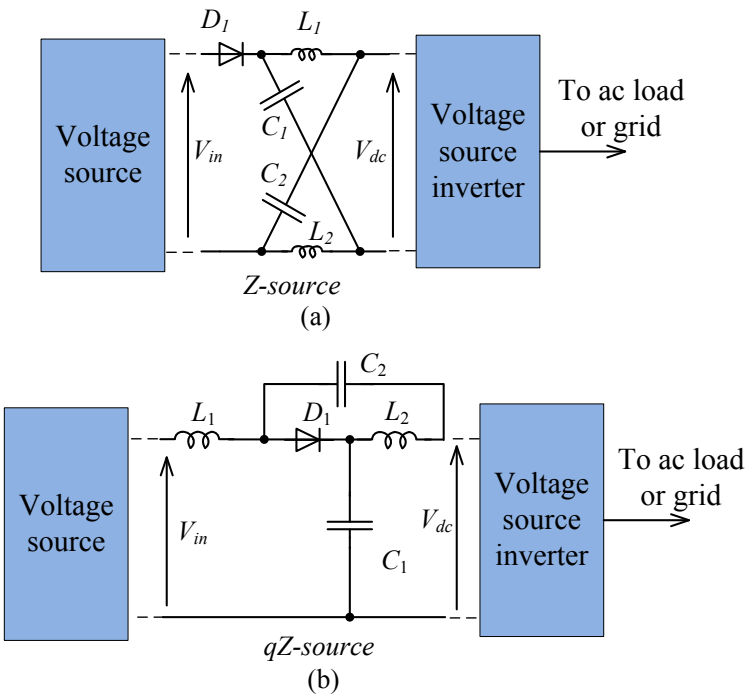


Fig. 2.8. General representation of a) ZSI and b) qZSI.

Fig. 2.9 shows the equivalent circuits during non ST states ((a) and (c)), where the inverter operates as a traditional one, with six active states and two zero states (for the two-level three-phase VSI) (the diode is conducting during those switching pattern signals). As shown in ((b) and (d)), during the shoot-through, the diode is switch off.

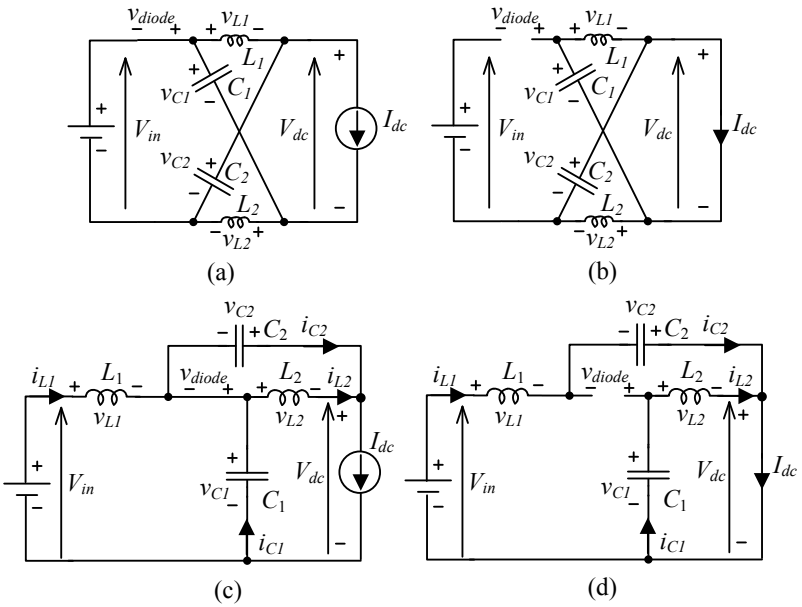


Fig. 2.9. Equivalent circuits during nonshoot-through state a) ZSI, c) qZSI; and during shoot-through state b) ZSI and d) qZSI.

As aforementioned, qZSI enables further improvements of the predecessor ZSI. Besides the advantages inherited from the ZSI, the qZSI have merits such as reduced passive component ratings, continuous input current and a common dc rail between the source and the inverter. qZSIs suit very well for renewable energy systems [16]-[22] because of excellent performance and availability of all the requirements, in particular for the PV systems. These inverters are capable of performing MPPT and inversion with no need for an extra dc/dc converter. Furthermore, continuous input current makes them especially suitable for fuel cell applications [16].

Due to the remarkable features of ZSI/qZSI, researchers have paid a lot of attention on new derived Z network. The majority of them are devoted to increase the voltage gain. Fig. 2.10 shows different derived topologies.

Fig. 2.10 a) and b) represent two different capacitor-assisted extended-boost qZSIs [23]. The first extension in Fig. 2.10 a) is a series of capacitor or diode connections to the basic qZSN. The second extension has one more stage of series inductor and capacitors (Fig. 2.10 b)). The inductor L_2 in qZSN is replaced by two inductors and three diodes, as Fig. 2.10 c) shows, forming a so-called switched-inductor qZSN (SL-qZSN) [24]-[25]. By converting two separate inductors in a qZSN into coupled inductors with the turns ratio (n) higher than one, as shown in d), the trans-qZSN improves the voltage gain [26]. Finally, Fig. 2.10 e) shows the inductor-capacitor-capacitor-transformer

qZSN (LCCT-qZSN) [27]-[29]. It combines L_2 and C_1 into a unique two-port network of high-frequency transformers (two coupled inductors L_{T1} and L_{T2}) and a blocking capacitor C_1.

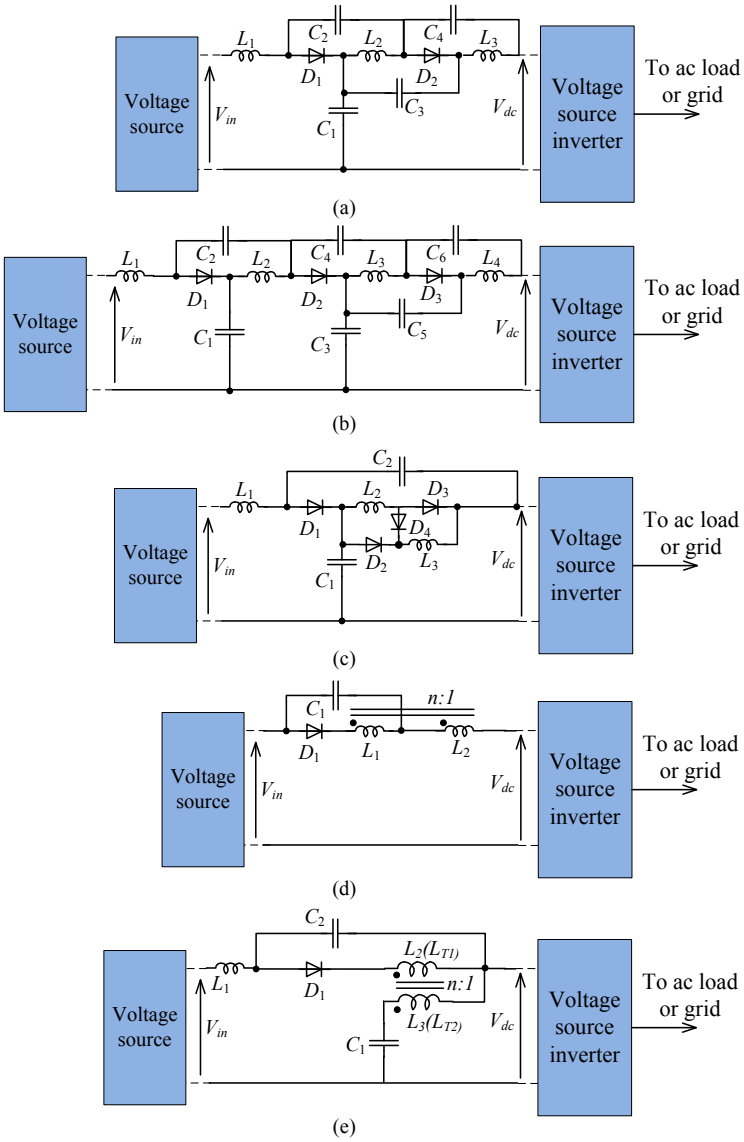


Fig. 2.10. Some derived qZS inverters. a) First extension of the capacitor-assisted EB-qZSN, b) Second extension of the capacitor-assisted EB-qZSN, c) SL-qZSN, d) trans-qZSN (n≥1), e) LCCT-qZSN (n≥1).

2.4 Multilevel dc/ac converter topologies

Several applications demand higher amount of power in different environments. To reach high power levels, VSIs require an increase in their voltage operation above the rated one, imposed by the semiconductor technology. The series connection of devices can increase such voltage rating but, at the expense of higher *dv/dt's*. Instead of connecting several power switches in series, multilevel inverter (MLI) arranges the semiconductors with additional dc-link capacitors to divide the total converter voltage to the blocking limit of power switches. This operation procedure connects the voltage to the load in sequences, improving the quality of the voltage waveform. Other advantages of this configuration are: higher voltage operation (above classic switch limits), reduced *dv*/*dt* and lower common mode voltage [30].

The *dv/dt* is reduced in a 1/ (*k*-1) fraction when using a multilevel structure, where *k* is the number of output voltage levels. This also means that the voltage rating can be increased (*k*-1) times for a specific semiconductor blocking limit, with the subsequent increase of the power level.

These outstanding features make multilevel converters very attractive for high-power applications (1-50 MW) that reach the medium-voltage level (2.3-10 kV). This section presents a brief summary of some of the most common multilevel converter topologies [11]. There is a number of multilevel converter topologies reported in the literature (Fig. 2.11), but some of them are highlighted in industry: neutral-point-clamped (NPC) or diode clamped, cascaded H-bridge (CHB) and flying capacitor (FC). They have been successfully introduced as commercial products.

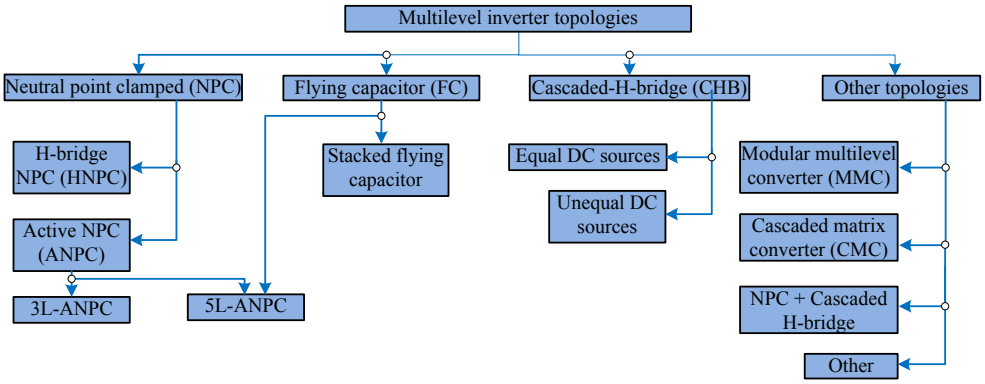


Fig. 2.11. Multilevel inverter classification.

The NPC multilevel inverter [31] (a version of three-phase three-level NPC is depicted in Fig. 2.12) is based on a modification of the classical two-level inverter where each power switch blocks a voltage equal to V_{dc}. By adding two extra switches per phase and two clamping diodes, it is possible to block $V_{dc}/2$ per switching device, hence the converter will handle double nominal power. This topology can be extended to any

number of levels with additional capacitors in the dc-link, additional switches and clamping diodes.

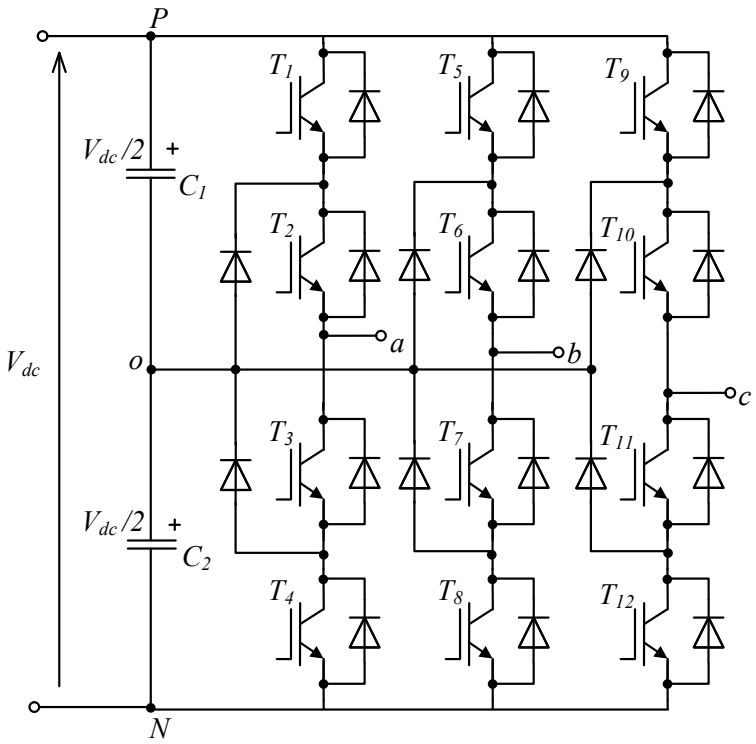


Fig. 2.12. Three-phase three-level NPC inverter.

However, the NPC topology presents an unequal distribution of the losses among power switches (the inner ones switch more times than the outer ones). This reason led to develop the active NPC (ANPC) inverter [32] (Fig. 2.13). This topology replaces the clamping diodes by clamping switches (IGCT in the figure) that allow the possibility to equalize the losses between them. It improves the reliability among other features.

Instead of using clamping diodes to share the voltage stress among devices, the multilevel FC inverter topology [33] uses several floating capacitors (Fig. 2.14 represents the three-phase three-level version). Flying capacitor is also called the multicell converter in order to show its high modularity (Fig. 2.15), where each cell is composed by two switches and one capacitor (connected each pair of cells in series). It is easily derived that each switch of a power cell is controlled in a complementary way.

In this topology, the voltage in the floating capacitors can be symmetrical or asymmetrical. This last case is not recommended since the voltage balancing of the capacitors is more difficult and imposes different blocking voltage among the devices.

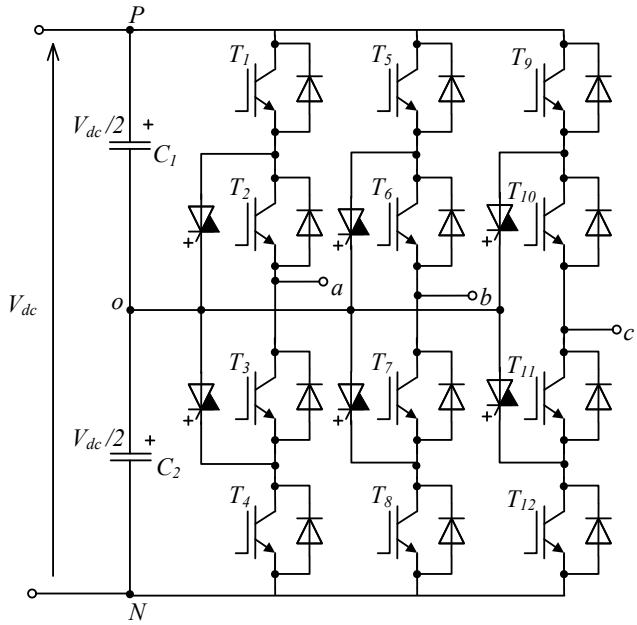


Fig. 2.13. Three-phase three-level ANPC inverter.

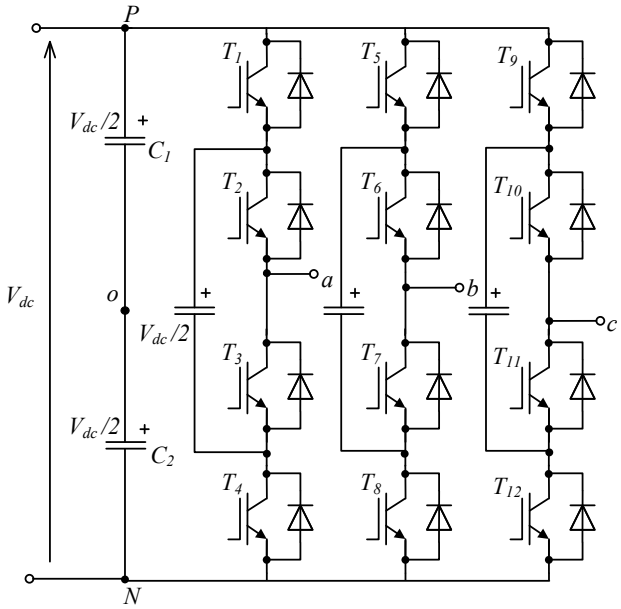


Fig. 2.14. Three-phase three-level FC inverter.

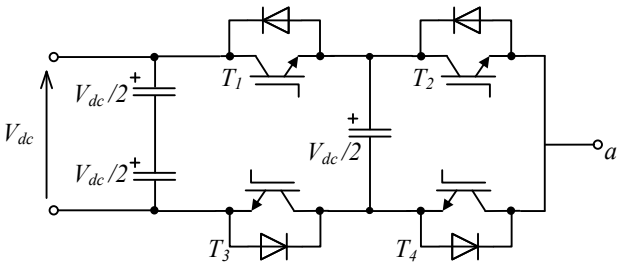


Fig. 2.15. Two-cell FC topology.

Other possible way to build a multilevel inverter is through the series connection of several H-bridges [34] with their corresponding independent voltage sources, considered as the basic cell. This configuration is called as cascaded H-bridge (CHB). This system presents a high modularity because the voltage is shared among different cells and semiconductor devices.

Each cell requires and independent voltage source, which can be equal or unequal. In the first case and considering two-cell cascaded H-bridges (Fig. 2.16), five output voltage levels are obtained. Unequal voltage increases the number of voltage levels, at the expense of reducing both the redundancy states and the system modularity.

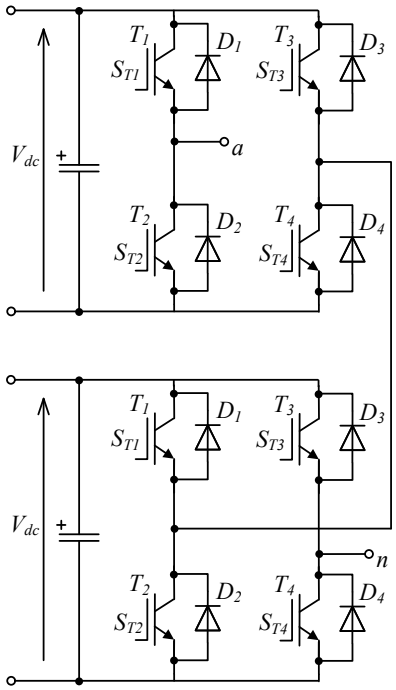


Fig. 2.16. Two-cell CHB inverter.

Another topology which is the current focus of industrial trends is the Modular Multi-level Converter (MMC) [35] (see Fig. 2.17), mainly for HVDC systems. It is similar to the CHB but, in this case, the series connection is between half-bridge structures with floating dc-link capacitors. Inductors are connected at the end of each leg to prevent undesirable transients. It is important to remark that voltage sensors are required for balancing floating capacitors.

Other developed topologies are: the cascade matrix converter (CMC), the hybrid between the three-level NPC and single-phase H-bridge cells [36] (NPC-CHB) and the hybrid between NPC and the H-bridge (H-NPC). This last configuration consists of the connection in parallel of two three-level NPC legs which forms an H-bridge in each phase of the system, with isolated dc sources.

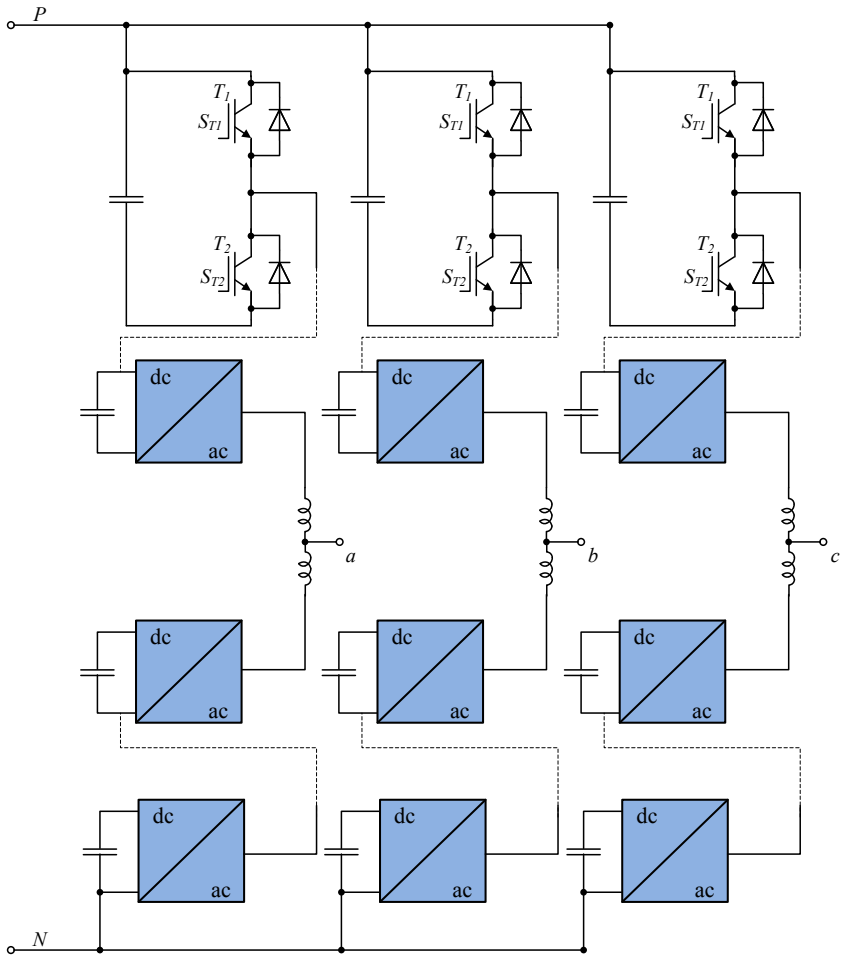


Fig. 2.17. MMC inverter.

2.5 ZS multilevel dc/ac converter topologies

2.5.1 State of the art

It has been explained that some of the benefits of ZSN and its derived network are the reduction of the energy conversion stages in some specific applications and that the advantages of multilevel bridges are a reduced voltage stress that allows to use fast semiconductors and smaller size of output filters among others. Because of that, recent solutions based on the combination of both solutions are collected in this section as previous stage to present our new solution.

Fig. 2.18 shows different three-level three-phase NPC topologies based on ZSN with Discontinuous Conduction Mode (DCM) of the input current. The first single-stage buck-boost MLI (Fig. 2.18 a)) was proposed in [37] as the logical extension of the two-level inverter and ZSI. This configuration uses two ZSNs for boosting their input voltage to a higher dc-link voltage. It is easy to observe that this one is not the best solution from the economical point of view, since it uses two isolated input voltage sources and a number of passive elements, which can increase the cost, size and weight of the inverter. To decrease the number of passive components, the Z-source NPC inverter with a single ZSN was proposed in [38]. However, this topology must also be supplied from two input voltage sources (Fig. 2.18 b). In those topologies, the voltage boost is expressed as

$$\mathrm{V}_{dc} = \frac{1}{1 - 2 \cdot D_S} \cdot \mathrm{V}_{IN} , \tag{2.4}$$

Where V_{IN} is a dc input voltage.

By the introduction of the high-frequency transformer and two additional capacitors the Z-source NPC inverter with a single ZSN could be supplied from a single input voltage source (Fig. 2.18 c) [39]-[42]. Fig. 2.18 d) shows a similar solution with a double transformer and separated input voltage dc sources. The main difference lies in the boost expression

$$\mathrm{V}_{dc} = \frac{1}{1 - (1 + n) D_S} \cdot \mathrm{V}_{IN} . \tag{2.5}$$

Using a transformer with n different from 1:1, an input voltage gain higher than that with the traditional ZSN can be achieved.

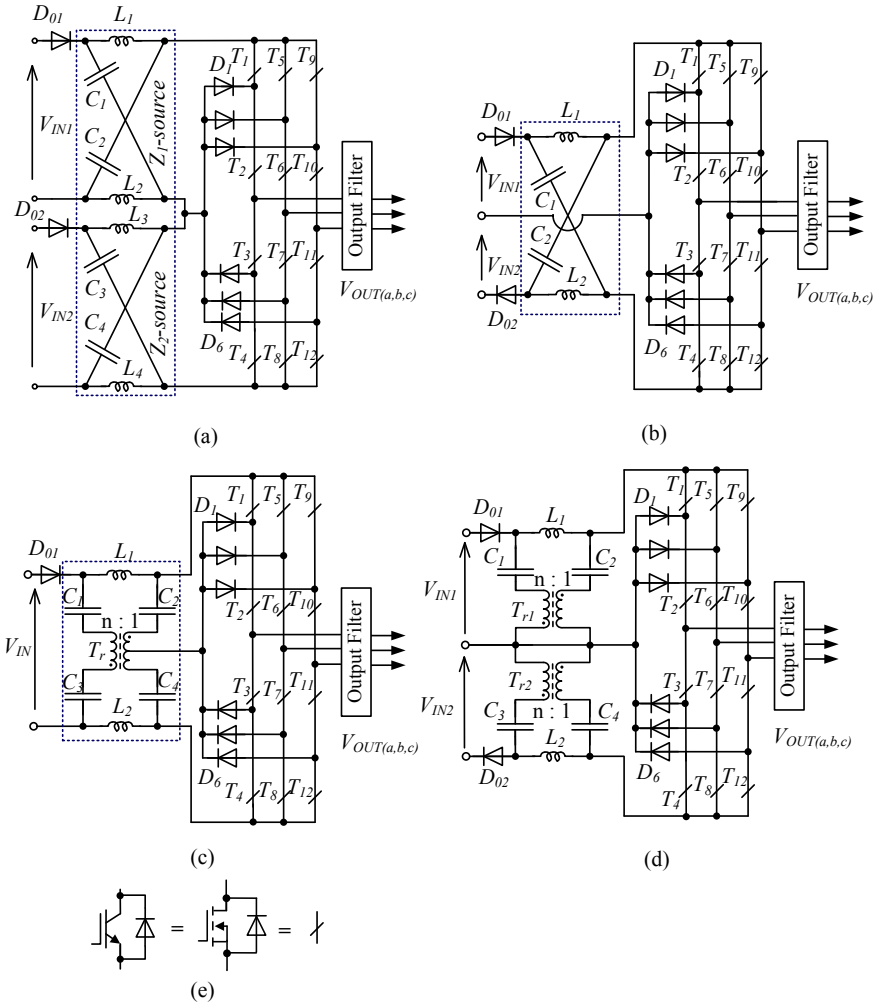


Fig. 2.18. 3L three-phase NPC topologies based on different ZSN. a) With two and separate Z-source network and input voltage sources, b) With single ZSN and separate input voltage source, c) Transformer Z-source NPC with single input voltage source, d) Transformer Z-source NPC inverter with separate input voltage sources, e) Generalization of power switch.

Fig. 2.19 a) shows a buck/boost four-level inverter. In this case each input power source is distributed among several ZSNs. The idea was presented in [39] and it is an example of extension of any ZSN to MLI based on the diode clamped configuration. Because of the possibility to separately regulate the output voltage in each Z-source, such MLIs are suitable to be applied in supply systems with locally dispersed energy sources. Fig. 2.19 b) illustrates multiple dc-link sources as further extension of the idea of the multilevel diode clamped topology [43] including just two ZSN.

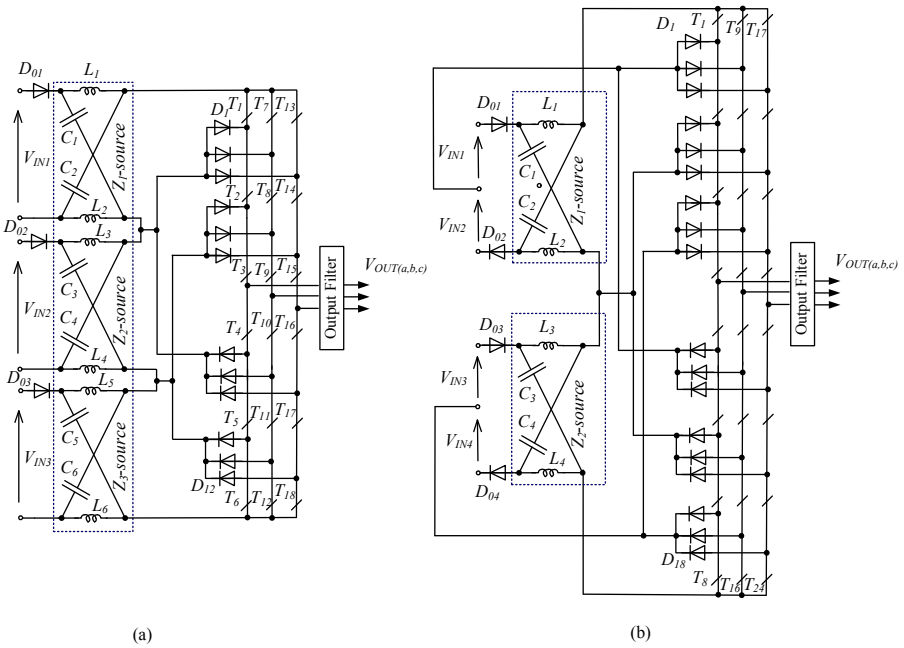


Fig. 2.19. a) Four-level Z-source inverter of Diode Clamped type. b) Five-level Z-source inverter of Diode Clamped type.

Fig. 2.20 shows several modifications of the previous buck/boost MLI. Fig. 2.20 a) shows the three-phase three-level DC-Link Cascaded (DCLC) inverter [44], where the passive elements are the same as in NPC with two ZSN. The only difference between the 3L NPC inverter and DCLC inverter consists in the asymmetrical blocking voltage on the transistors and the absence of the clamping diodes. A variation based on dual configuration is presented [44] in Fig. 2.20 b) and c), with two and single ZSN respectively. Their dc-link voltage can be twice lower in the case of a *n* equal to 2. The main difference between the dual solution with separated and single ZSN consists of the power flow. In the second case, the number of passive components is a half, but their size is larger.

Cascaded solutions based on the Z-source networks have already been presented [45]-[46]. Simple cascading is described in [46]. Two ZSNs, two isolated input voltage sources and two two-level full bridge (FB) inverters provide five-level output voltage per single phase.

Fig. 2.21 shows the general structure of the most complex cascading of the hybrid-sourced network in the 3L NPC [45]. Seven level Z-source based inverter is carried out by means of cascading traditional, embedded and dc-link embedded voltage-type Z-source that were proposed in [47]. This configuration requires three isolated input voltage sources and *N* networks.

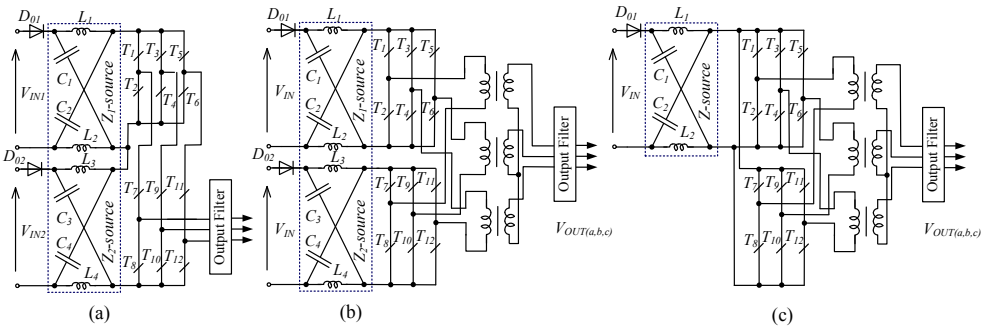


Fig. 2.20. Modifications of the 3L Z-source based inverters: a) 3L DCLC inverter with two Z-source networks, b) 3L dual inverter with two Z-source networks, c) 3L dual inverter with single Z-source network.

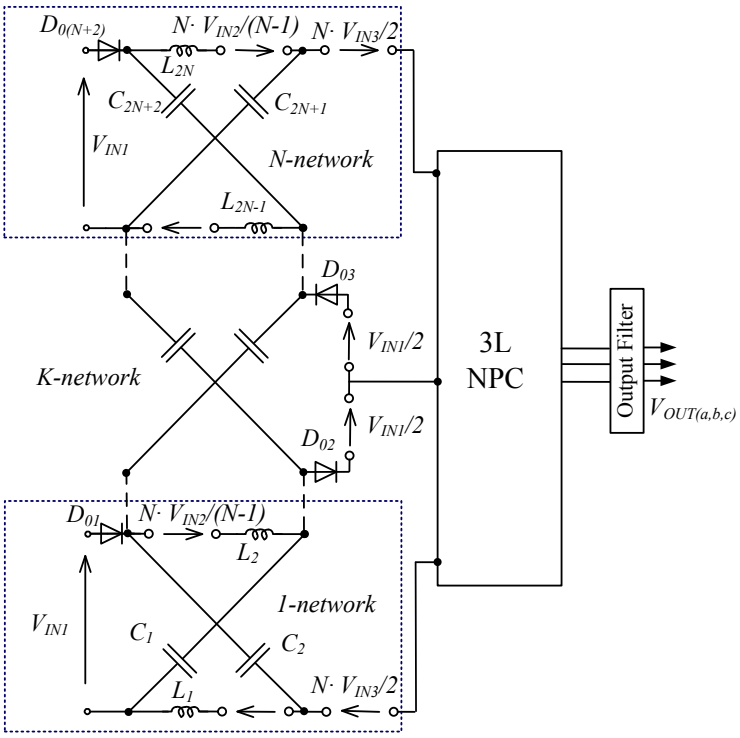


Fig. 2.21 Seven-level Z-source based inverter.

The total boost of this converter is:

$$V_{dc} = \frac{1}{1-(1+N)D_S} \cdot V_{IN} \,, \tag{2.6}$$

where $V_{IN}=V_{IN1}+V_{IN2}+V_{IN3}$.

This method requires that the number of N cascaded networks must always be odd with the middle network notated as

$$K = \frac{N+1}{2}. \tag{2.7}$$

Other proposed cascaded configuration in [45] is based on N-1 additional capacitors and 2(N-1) additional diodes for connecting N ZSN together at their respective dc-links. This so called dc-link cascaded solution achieves very high boost performance

$$\mathrm{V}_{dc} = \frac{1}{(1-2\cdot D_S)^{\frac{N+1}{2}}} \cdot \mathrm{V}_{IN}. \tag{2.8}$$

Paper [48] presents the description of a new inverter topology based on a mixture of cascaded basic units and one FB (Fig. 2.22). The basic unit includes one ZSN, one input dc voltage source and two switches generating two voltage levels. The basic unit can operate in three modes: zero, active and ST states. In the ST state, both switches S_1 and S_2 are conducting and the output voltage is zero. The active state is generating, when only S_1 is conducting. Zero state corresponds to the S_2 conduction. In this solution, the overall number of power semiconductor switches is reduced with respect to the traditional MLIs. This configuration allows that any N-level topology is achievable due to the above described principle and also can be extended to three-phase systems.

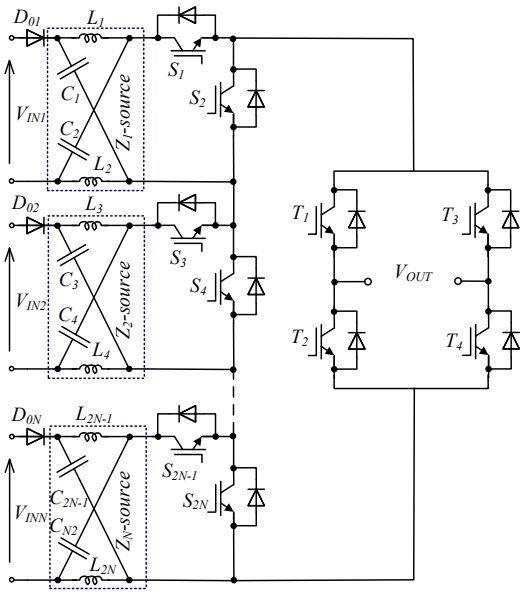


Fig. 2.22. Z-source-based MLI with reduction of switches.

Further development of the ZSN based buck-boost MLIs is by involving the trans-ZS and trans-qZS inverters. In particular, Fig. 2.23 shows two 3L NPC solutions [49].The circuit configuration of the trans-Z-source NPC inverter is shown in Fig. 2.23 a) and Fig. 2.23 b) shows the circuit configuration with the trans-quasi-Z-source NPC inverter, where the only difference is the location of the input voltage source. Both of them consist of a transformer to replace the two inductors in the original ZSN and removing one capacitor from it. This can enhance the boosting capability of the ZSN and reduce one passive component, with lower size and cost of system consequently.

The main difference between the first and second approach consists in the input current waveform, which corresponds to a CCM in the second case.

Recently another trans-Z-source NPC inverter was proposed in [50] and depicted in Fig. 2.24 a). Fig. 2.24 b) shows the Γ-source inverter that was proposed in the same paper. Input voltage boost for the first topology is equal to (2.4) but, for the second one:

$$V_{dc} = \frac{1}{1 - \frac{n}{n-1} \cdot D_S} \cdot V_{IN} \,. \tag{2.9}$$

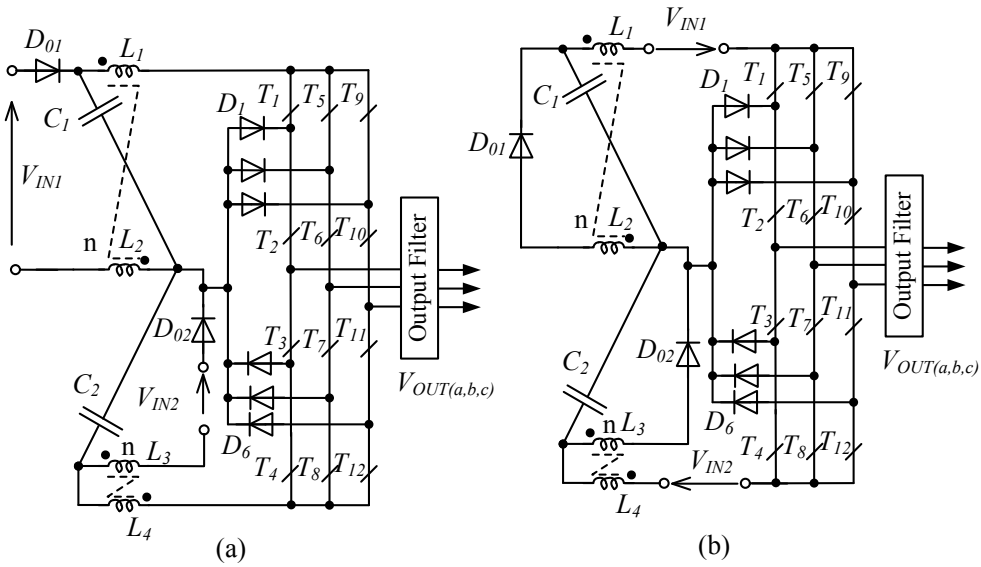
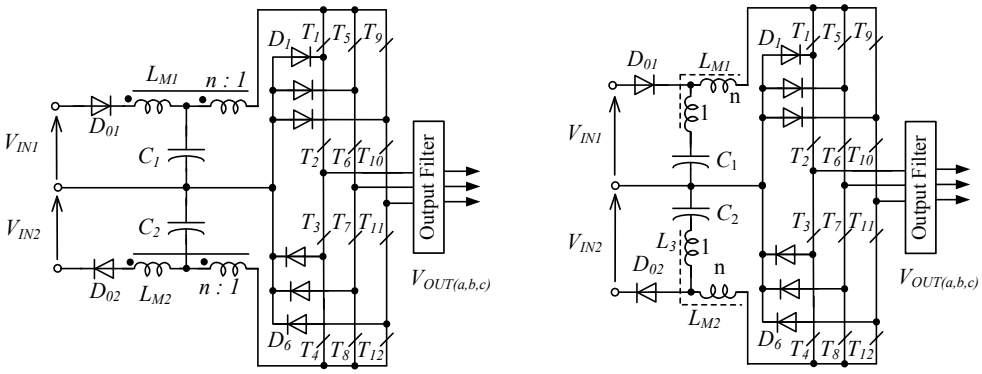


Fig. 2.23. a) 3L NPC trans-Z-source inverter and b) 3L NPC trans-quasi-Z-source inverter.



(a) (b)

Fig. 2.24 a) Other 3L NPC trans-Z-source inverter and b) 3L NPC - Γ source inverter.

2.5.2 Proposed three-level neutral-point-clamped qZS dc/ac converter topology

This section presents the novel three-level neutral-point-clamped quasi-Z-source inverter as a new member of the single-stage buck-boost multilevel inverter family [**d**], [**e**] and [**f**]. The topology is derived by combining the properties of the qZS with those of a three-level NPC inverter. To summarize:

Advantages of qZN:

- single-stage buck-boost power conversion
- continuous input current
- reduced passive component ratings
- common dc rail between the source and the inverter
- short-circuit immunity
- eliminates the need for dead-times
- better THD
- wider input voltage regulation range.

Advantages of 3L NPC:

- lower semiconductor voltage stress
- lower required blocking voltage capability
- decreased *dv*/*dt*
- better harmonic performance
- soft switching possibilities
- higher switching frequency.

This solution inherits both previous intrinsic advantages. In PV applications, a continuous input current is required to reduce the stress of the input voltage source (PV panel) and usually a voltage boost by means of a dc-dc boost converter with wide range of input voltage regulation (due to irradiance and temperature influences) is needed as

well. This new configuration presents availability of all these requirements. The core idea is to combine two symmetrical qZS networks with a NPC ML bridge. The twice lower voltage stress on the semiconductors allows fast switches (e.g. MOSFETs) to be used, which leads to high switching frequency and better power density. Moreover, the power source can be single or separated by means of the neutral point.

Single-phase version

This section summarizes the operation principle of the system of a single-phase 3L-NPC-qZSI (Fig. 2.25). It consists of two complementary switch pairs for every leg and four clamping diodes. Two identical qZSNs have a common node between the capacitors C_2 and C_3, forming the neutral point of the topology.

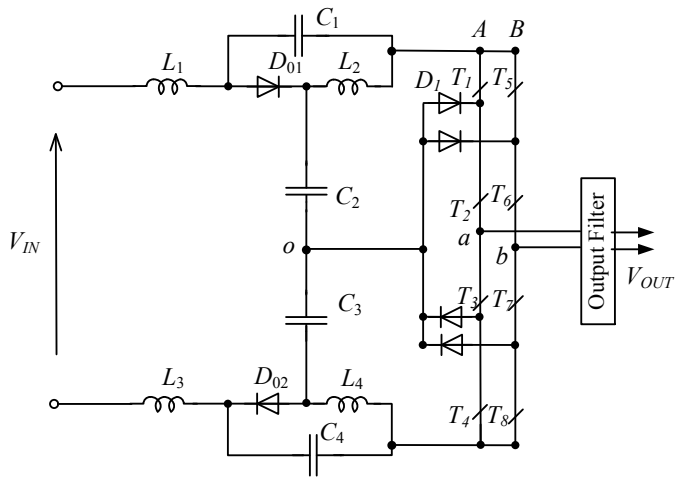


Fig. 2.25. New proposed quasi-Z source NPC inverter: single phase case study system.

The different switching states per branch in qZS NPC inverter are summarized in Fig. 2.26. The fundamental period in the single phase system can be divided into eight time intervals, separated in three modes: active states, zero states and ST states. To estimate the component values, the steady state analysis is performed by means of voltage balance across the inductors and current balance across the capacitors:

$$\frac{1}{T}\int_{t}^{t+T} v_{Li}(t)\,dt = 0 \text{ and } \frac{1}{T}\int_{t}^{t+T} i_{Ci}(t)\,dt = 0\,. \tag{2.10}$$

Where v_{Li} is the instantaneous voltage across an inductance i, i_{Ci} is the instantaneous current across a capacitor i and T is the fundamental period.

In the CCM, the full switching period is expressed as

$$\frac{t_A}{T} + \frac{t_Z}{T} + \frac{t_S}{T} = D_A + D_Z + D_S = 1 \tag{2.11}$$

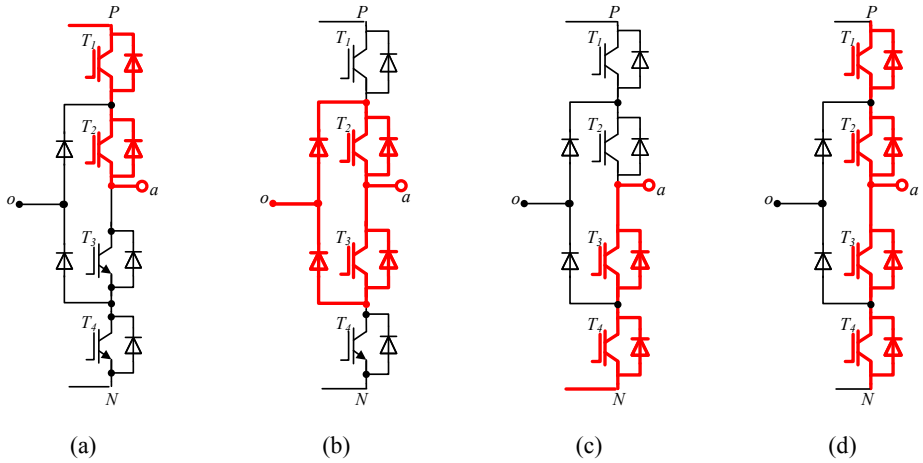


Fig. 2.26. Different switching states per branch in the qZS NPC inverter. a) $u_{ao} = B\,(V_{dc}/2)$. b) $u_{ao} = 0$. c) $u_{ao} = -\,B\,(V_{dc}/2)$. d) ST state.

where t_A, t_Z and t_S are the time duration of the active, zero and ST states respectively and D_A is the duty cycle of the active state, D_Z is the duty cycle of the zero state and D_S is the duty cycle of *ST*.

The sum of the capacitors voltages defines the peak value of the dc-link voltage

$$V_{dc} = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{2.12}$$

where V_{Ci} defines the average voltage across the capacitors over one fundamental period (considered as constant).

Assuming that the qZSN is symmetrical, we obtain

$$L_1 = L_3, \qquad L_2 = L_4 \tag{2.13}$$

$$C_1 = C_4, \qquad C_2 = C_3. \tag{2.14}$$

Correspondingly, the voltage values are

$$v_{L1} = v_{L3}, \qquad v_{L2} = v_{L4}, \tag{2.15}$$

$$V_{C1} = V_{C4}, \qquad V_{C2} = V_{C3}. \tag{2.16}$$

The capacitors voltage values are obtained from assuming $V_{Li} = 0$ (2.10)

$$V_{L1} = \frac{1}{T}\int v_{L1}(t)dt = \frac{1}{T}((V_{C2} - \frac{V_{in}}{2})t_A - (V_{C1} + \frac{V_{in}}{2})t_S) = (V_{C2} - \frac{V_{in}}{2})D_A - (V_{C1} + \frac{V_{in}}{2})D_S = 0\,. \tag{2.17}$$

$$V_{L2} = \frac{1}{T}\int v_{L2}(t)\,dt = \frac{1}{T}(V_{C1}\,t_A - V_{C2}\,t_S) = V_{C1}\,D_A - V_{C2}\,D_S = 0\,. \tag{2.18}$$

Taking into account the conditions presented above, we obtain the voltage across the capacitors:

$$V_{C1} = V_{C4} = \frac{D_S\,V_{in}}{2 - 4D_S} \tag{2.19}$$

$$V_{C2} = V_{C3} = \frac{V_{in}\left(1 - D_S\right)}{2 - 4D_S}\,. \tag{2.20}$$

The final equation for the boost factor can be expressed as follows

$$B = \frac{V_{dc}}{V_{in}} = \frac{V_{C1} + V_{C2} + V_{C3} + V_{C4}}{V_{in}} = \frac{1}{1 - 2D_s}\,. \tag{2.21}$$

More detailed mathematical foundations along the equivalent circuits in each time interval are exposed in paper [**d**] and [**f**] in appendix.

For dimensioning the passive components of the qZSN, it is necessary to take into account the low frequency pulsation (at 100 Hz) of single phase systems in the dc side along the high switching frequency ripples. Low frequency fluctuations are produced by the instantaneous value of the output power (Fig. 2.27 a)). The high frequency ripples are mostly caused by the high frequency generation of the ST states (Fig. 2.27). CCM will be also assumed.

In a simplified approach, high switching frequency is neglected to estimate low frequency ripples. In this case the output current is represented as an ideal ac current (i_{DC}~) source equal to the fundamental component of the dc-link current.

$$i_{DC\sim} = I_{C\_Max}\sin(4\pi\frac{1}{T}t - \frac{\pi}{2}) = \frac{\sqrt{2}\,4}{3\pi}\frac{P_{OUT}}{V_{OUT}}\sin(4\pi\frac{1}{T}t - \frac{\pi}{2}), \tag{2.22}$$

where P_{OUT} and V_{OUT} are the output power and voltage respectively. Assuming that the CCM is achieved and the qZSN is symmetrical, we can represent the converter behaviour by a simple equivalent circuit (Fig. 2.27 c)) for an ac component.

In a general case, in the conditions above, we can define the ac component of the input current (i_{L1}~) as

$$i_{L1\sim} = I_{DC\_Max}\sin\left(4\pi\frac{1}{T}t - \frac{\pi}{2}\right)\left|\frac{X_{C2}}{X_{C2} + X_{L1} + R}\right| = \frac{\sqrt{2}\,4P_{OUT}T^2\sin(4\pi\frac{1}{T}t - \frac{\pi}{2})}{3\pi V_{OUT}\sqrt{16\pi^2C_2^2R^2 + (16\pi^2C_2L_1 - T^2)^2}}\,. \tag{2.23}$$

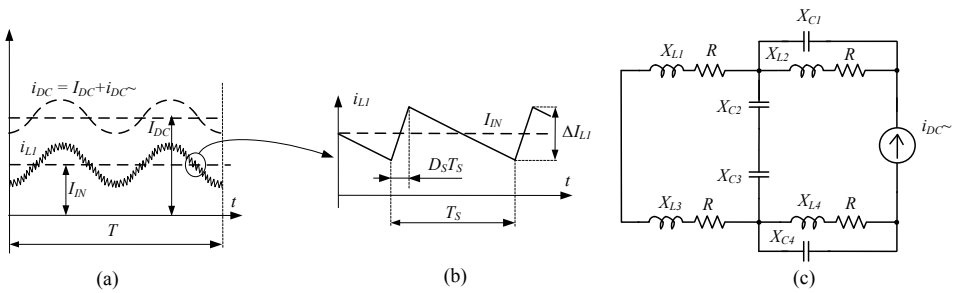


Fig. 2.27. a) Idealised operating waveforms at low frequency view. b) At high frequency. c) Equivalent circuit.

It should be noted that R represents the resistive part of each inductance of the qZSNs. Equal values of resistance are assumed to simplify the equations.

The average input current is obtained by means of power balance, where we assume that P_{OUT} is approximately equal to the input power (P_{IN}):

$$P_{IN} = \mathrm{V}_{IN} I_{IN} \approx P_{OUT} . \tag{2.24}$$

Low frequency input current ripple factor (K_{LL1}) can be calculated as

$$K_{LL1} = \frac{\hat{i}_{L1\sim}}{I_{IN}} \approx \frac{\hat{i}_{L1\sim} V_{IN}}{P_{OUT}} \approx \frac{8(1-2D_S)T^2}{3\pi(1-D_S)\sqrt{16\pi^2 C_2^2 R^2 + (16\pi^2 C_2 L_1 - T^2)^2}} . \tag{2.25}$$

The ac voltage component of the capacitors C_1 and C_4 can be expressed similarly as

$$v_{C1\sim} \quad {}_{2\sim} \cdot \left| \frac{(X_{L2}+R)X_{C1}}{X_{C1}+X_{L2}+R} \right| = i_{DC\sim} \cdot \frac{(4\pi T L_2 + RT^2)}{\sqrt{16\pi^2 C_1^2 \cdot R^2 + (16\pi^2 C_1 L_2 - T^2)^2}} . \tag{2.26}$$

Low frequency voltage ripple factor (K_{CL1}) for capacitors C_1 and C_4 can be obtained from eqs. (2.18) and (2.25)

$$K_{CL1} = \frac{\hat{v}_{C1\sim}}{V_{C1}} = \frac{8\, P_{OUT}\,(1-D_S)(4\pi T L_2 + R \cdot T^2)}{3\pi V_{OUT}^2 D_S \sqrt{16\pi^2 C_1^2 R^2 + (16\pi^2 C_1 L_2 - T^2)^2}} . \tag{2.27}$$

Voltage ripple factor for capacitors C_2 and C_3 (K_{CL2}) as well as the current ripple factor for inductors L_2 and L_4 (K_{LL2}) can be derived in a similar way. The final expressions are as follows

$$K_{LL2} = \frac{\hat{i}_{L2\sim}}{I_{IN}} \approx \frac{8(1-2D_S)T^2}{3\pi(1-D_S)\sqrt{16\pi^2 C_1^2 R^2 + (16\pi^2 C_1 L_2 - T^2)^2}} . \tag{2.28}$$

$$K_{CL2} = \frac{\hat{v}_{C2\sim}}{V_{C2}} = \frac{8 \cdot P_{OUT}\,(4\pi T L_1 + RT^2)}{3\pi V_{OUT}^2 \sqrt{16\pi^2 C_2^2 R^2 + (16\pi^2 C_2 L_1 - T^2)^2}} . \tag{2.29}$$

Those previous expressions allow to calculate the values of passive elements taking into account the predefined low frequency ripples (100 Hz) of voltage and currents.

To determine the values of passive elements taking into account the high frequency ripples it is necessary to study the ST interval.

$$\Delta I_{L1} = \int_0^{T_{sw}D_S} \frac{di_{L1}}{dt} dt = \int_0^{T_{sw}D_S} \left(\frac{V_{IN} + V_{C1} + V_{C4}}{2L_1}\right) \cdot dt = \left(\frac{V_{IN} + V_{C1} + V_{C4}}{2L_1}\right) T_{sw} D_S, \quad (2.30)$$

where T_{sw} is the switching period.

We can express the high switching frequency current ripple factor K_{LH1} as

$$K_{LH1} = \frac{\Delta I_{L1}}{2 I_{IN}} \approx \frac{V^2{}_{OUT}(1-2D_S)}{2\cdot(1-D_S) L_1 P_{OUT}} T_S \cdot D_S, \quad (2.31)$$

to finally achieve

$$L_1 \geq \frac{V^2{}_{OUT}(1-2D_S)}{2\cdot(1-D_S) K_{LH1} P_{OUT}} T_S D_S. \quad (2.32)$$

From the last equation we can estimate the minimum inductance value to maintain high switching frequency ripples in the input current, that is a condition of the CCM operation. The sum of low and high frequency input current ripples should be smaller than the average input current I_{IN}. The obtained value is used for each L_i as generalization.

More detailed mathematical equations related to the passive element sizing are revealed in paper [**d**] and [**f**] in appendix.

Three-phase version

The three-phase version of the proposed topology is depicted in Fig. 2.28. The configuration is based on two symmetrical qZSN with a common node between the capacitors C_2 and C_3, forming the neutral point of the topology as in the previous case. Inverter bridge is extended with the parallel connection of one more branch.

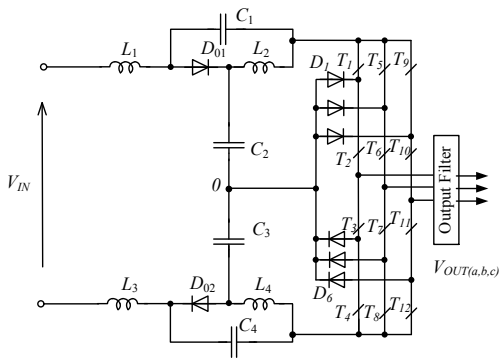


Fig. 2.28. New proposed quasi-Z source NPC inverter: Three phase case study system.

The possible voltage levels or switching states per branch are the same than in the previous case. Now, due to the three branches we have 3^3=27 possible switching states and the ST. All of them can be classified in active states, zero states and ST states as well. These states are generalized in equivalent circuits of Fig. 2.29.

The same approach as before is done since the equivalent phase-to-neutral circuit matches with the single phase version. The analysis of the steady state by means of voltage balance across the inductors and current balance across the capacitors is similar, where we obtained expressions (2.18) to (2.20) to define the voltage in capacitors and *B*.

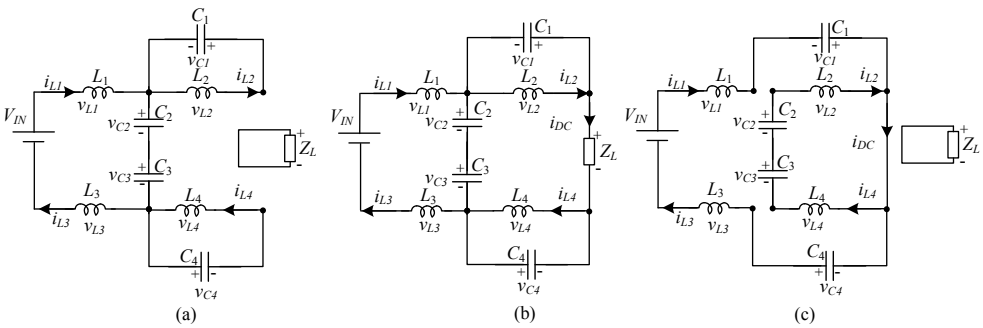


Fig. 2.29. Equivalent circuits. a) Zero states. b) Active states. c) ST states.

Anyway, the steady state analysis of three-phase case is detailed in paper e) in appendix.

To estimate the value of passive components of qZN we do not take into account the low frequency ripple at 100 Hz at the dc side in this case. Just the high frequency ripple connected related to the ST states will be the criteria for dimensioning such elements.

As in equation (2.29) for dimensioning the single phase inverter, we can obtain an expression to obtain the minimum value of the inductance in order to guarantee a ripple in the inductor current to maintain the CCM operation, once defined a predefined ripple (K_L). It is:

$$L \geq \frac{4V^2_{OUT}(1-2D_S)}{(1-D_S)K_L P_{OUT}} T_S D_S \,. \tag{2.33}$$

The inductance value condition obtained is assumed for each L_i. Similar high frequency ripple basis for capacitors can be derived. Calculating the capacitor voltage ripples (ΔV_{c1} and ΔV_{c2}) and maintaining a desired voltage ripple factors (K_{C1} and K_{C2}), the final equations are

$$C_1 = C_4 \geq \frac{T_S P_{OUT}\left(1-D_S\right)^2}{4K_{C1}V^2_{OUT}\left(1-2D_S\right)} \text{ and} \tag{2.34}$$

$$C_2 = C_3 \geq \frac{T_S P_{OUT}\left(1 - D_S\right) D_S}{4K_{C2} V_{OUT}^2 \left(1 - 2D_S\right)}. \tag{2.35}$$

More details about calculating of passive elements of three-phase system are available in paper [**e**] of the appendix.

Output filter design

In this section the method to estimate the value of components that make up the output filter of the proposed 3L-NPC-qZI will be summarized. First of all some approaches well known in the literature [51]-[76] will be introduced.

L-filter is the simplest solution [51]-[55]. The main drawbacks of the *L*-filter are its large size inductor and low output voltage quality in open-loop control mode. Overall size can be reduced using an *LC* or *LCL*-output filter. A general scheme of a grid-connected PV system and configurations of different output filters are represented in Fig. 2.30 a), b), c) and d) respectively.

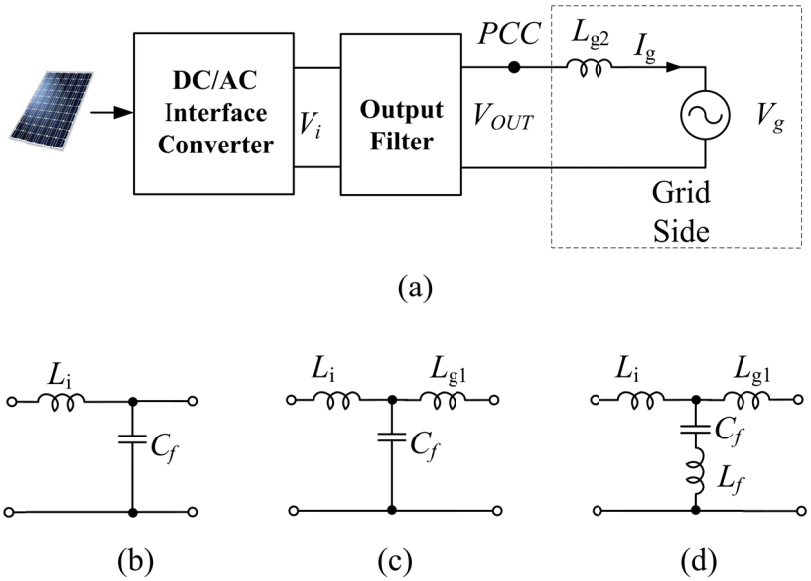
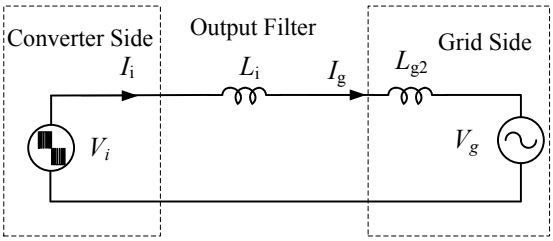


Fig. 2.30. a) General scheme of a grid-connected PV system. b) *LC*-filter. c) *LCL*-filter and d) *LLCL*-filter.

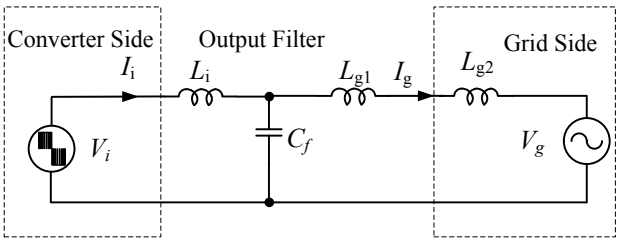
LC-filter is also a possible solution but it is mainly used in off-grid systems [55]-[60]. Moreover, any grid has its own internal inductance L_g, therefore an *LC*-filter cannot be considered for use in a grid-connected system as it is. *LCL*-filter satisfies the grid inter-connection standards with a significantly smaller size and cost, but it might be more difficult to keep the system stable [61]-[74]. In contrast to the *LCL*-filter, the *LLCL*-filter [75]-[76] has nearly zero impedance at the switching frequency and can strongly

attenuate the harmonic currents around the switching frequency. To avoid stability problems in high order filters in the closed-loop control mode, damping methods are used. These methods are classified as passive or active. In the first case, generally, a resistor is added in series to the capacitor or in parallel to the grid inductor. The active damping method is based on the modification of the control system for resonance mitigation [68]-[71].

A criterion to design a *L* or *LCL*-filter is based on the current ripple at the switching frequency, considering that the inverter is a harmonic generator and the grid is a short-circuit [52],[60] and [62]. Their equivalent schemes are represented in Fig. 2.31 a) and b).



(a)



(b)

Fig. 2.31. Equivalent circuit of a) *L*-filter and b) *LCL*-filter.

Obtaining the transfer function in the frequency domain of the circuit in Fig. 2.31 a), and assuming that the power factor is equal to 1, it is easily derived that the minimum inductance value that satisfy a certain current Total Harmonic Distortion (THD_I) is

$$L_i \geq \frac{V_i(h_{sw}) \cdot V_g}{\omega_1 \cdot h_{sw} \cdot P \cdot THD_I}, \tag{2.36}$$

where V_i (h_{sw}) is the RMS output voltage component at the switching frequency, V_g is the RMS grid voltage value, ω_1 is the fundamental pulsation, h_{sw} is the switching harmonic order, P is the rated power and THD_I is the total current harmonic distortion.

By solving the equivalent circuit of Fig. 2.31 b) it is possible to obtain the third-order transfer function of the grid-connected inverter with *LCL-filter*, assuming that $L_g = L_{g1} + L_{g2}$. It is also necessary to ensure that the resonance frequency f_{res} will within a range between ten times the line frequency f_1 and half the switching frequency f_{sw} in order to avoid resonance problems [60]-[62]

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_g + L_i}{L_g \cdot L_i \cdot C_f}} \text{ and} \tag{2.37}$$

$$10 \cdot f_1 \le f_{res} \le \frac{f_{sw}}{2}. \tag{2.38}$$

We can determine L_g as a function of L_i, using the index r for the relation between both inductances [61]-[63]

$$L_g = r \cdot L_i. \tag{2.39}$$

Assuming that f_{res} is determined and that the capacitor value (C_f) is limited to decrease the capacitive reactive power, it is possible to determine a quadratic expression for index r as (L represents a weighted inductance)

$$\begin{aligned} &r^2(L^2\omega_1^2 h_{sw}^2 C_f - L) - (L^2\omega_1^2 h_{sw}^2 C_f + L) + \\ &+r(2L^2\omega_1^2 h_{sw}^2 C_f - 2L - \frac{V_i(h_{SW}) \cdot V_g}{P \cdot THD_I \omega_1 h_{sw}}) = 0. \end{aligned} \tag{2.40}$$

According to that approach, we can define the value of the capacitor and the index r, which provides a complete definition of the output filter. More details about the traditional mathematical foundations for calculating L or *LCL*-output filter are available in section II of paper [**c**] attached in appendix.

This aforementioned methodology is mainly based on the high frequency current ripple. The new approach assumes that, at any moment, the waveform of the injected current is defined by the voltage difference between the inverter side and the grid side. In the case of an ideal grid with negligibly low impedance, the voltage waveform in PCC is sinusoidal (Fig. 2.32 a). In the case of an off-grid system with a resistive load, the waveform of the output voltage has a fundamental component and high frequency ripple similar to the output current waveform (Fig. 2.32 b). Assuming that high frequency ripple is relatively low and that the output voltage on the resistor has pure sinusoidal waveform, the current will be the same as in the case of the grid-connected inverter and we can use the voltage approach for the grid-connected system as well. Therefore we can represent the grid side as an equivalent inductance in series with a passive resistor that corresponds to the nominal power (Fig. 2.32 c).

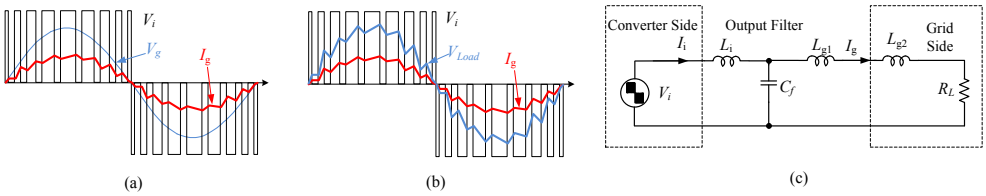


Fig. 2.32. a) Voltage and current waveforms of the grid-connected, b) islanding mode system and c) equivalent grid-connected converter with output filter at rated power.

In this method the goal is to maintain the Total Harmonic Distortion of the Voltage (THD_U) in a desired value and the analysis is based on the first-order and third-order voltage transfer functions in the frequency domain ($K_L(s)$ and $K_{LCL}(s)$). A similar approach is revealed in [57] but with different optimization criteria.

The minimum inductance value based on this new methodology is given by

$$L_i \geq \frac{R_L \sqrt{V_i^2 (h_{sw}) - V_g^2 \, THD_U^2}}{V_g \, THD_U \, \omega_1 \, h_{sw}} . \tag{2.41}$$

Where R_L is the resistance that corresponds to the rated power. Note that L_f is considered the sum of L_i and L_g.

Similarly to the current transfer function design approach in *LCL* sizing procedure, it is possible to obtain an expression to determine both the L_g and L_i as a function of r.

$$K_{LCL}(h_{sw}) = \frac{1}{(1 - \omega_1^2 h_{SW}^2 \frac{1+r}{r} L C_f) \sqrt{1 + \omega_1^2 h_{SW}^2 \frac{(1+r)^2 L^2}{R_L^2}}} . \tag{2.42}$$

Mathematical basis and calculations for this new proposed methodology both in *L*-filter and *LCL*-filter cases are well described in paper [**c**] of the appendix.

Semiconductor selections

The voltage and current stresses across the components are the key parameters for dimensioning semiconductors. In our multilevel configuration, voltage stress on the transistors, as well as on the diodes, is equal to half the dc-link voltage as previously justified.

Two different technologies for semiconductors are selected for the single-phase topology and three-phase respectively. For the single phase version, high switching frequency MOSFETs with fast body diodes and hyper fast qZS diodes allow the switching frequency to be raised up to 100 kHz, so reducing the size of the passive components and increasing the power density of the converter.

For the three-phase system we have as main difference the double dc-link voltage. For normalized voltages, to generate 325 V as peak value it is usually required 650 V in the dc-link (this value can be reduced by injecting third harmonic). As dimensioning criteria, in order to provide an input voltage range regulation from 300 V up to 800 V (boost and buck mode), semiconductors must withstand the dc-link voltage in a range of 650 V - 1000 V approximately. In the worst case, it means that the maximum voltage stress on the transistors and on all the diodes is equal to 500 V (half the maximum dc-link voltage). There are several appropriate semiconductor solutions. Classical IGBT can be used. The main advantage of this solution is its reliability. The drawback lies in a low switching frequency that forces the use of larger passive elements. Recently, MOSFETs based on SiC have appeared as a new family of fast high-voltage switches. Derived from experimental investigations of the dc-dc and dc-ac converters based on the qZS network [77]-[78], it can be concluded that among every solutions for the qZS diode, only Shottky diodes suit. Because of relatively high voltage, SiC based Shottky diodes can be used.

Prototype assembling

The control system of both prototypes (single-phase and three-phase) is based on FPGA. FPGA makes it easier to implement the ST mode that is important for the given topology. The structure of the converters consists of four main PCB boards (qZSN, inverter, measurement and control board) and external output filter in each case, finally assembled in a 3U box. Such structure has very high flexibility and repairability.

Full parameters for the single-phase case that guarantee full CCM in the defined operating range, according to previous sections are summarized in Table 2.4.

Table 2.4. System parameters of single-phase prototype.

Element	**Value or type**
Control Unit (FPGA)	Cyclone II EP2C5T144C8
Transistor Driver Chip	ACPL-H312
Transistors	SPW24N60C3
qZS and NPC diodes	8ETH06PBF
Input DC voltage	220-325 V
Output AC RMS voltage	230 V
Output power	1 kW
Capacitance value of the capacitors C_1 and C_4	1.2 mF
Capacitance value of the capacitors C_2 and C_3	0.94 mF
Inductance value of the inductors L_1 ... L_4	180 µH
Inductance of the filter inductor	2.2 mH
Capacitance of the filter capacitor	0.47 µF
Switching frequency	100 kHz

For the three-phase system, it is necessary to point out that is based on SiC semiconductor technology. Because of that, we explain with more details its components. The first board is a 3-phase 3-level NPC inverter. Transistors along with clamping diodes are located close to the radiator. Since the losses are very low, radiators are small and additional fans are not required. Drivers (ACPL H342) of the transistors are located on the top side of the board.

The second board consist of the qZS capacitors (EZPE50117MTA) and qZS diodes, which compose the qZN.

Measurement board is made up with current (LTS 15-NP) and voltage sensors (LV25-P) by LEM. Operational amplifiers (LT1492CS8) and AD converters (LTC1864) by Linear Technologies that send data to the control board are also included there.

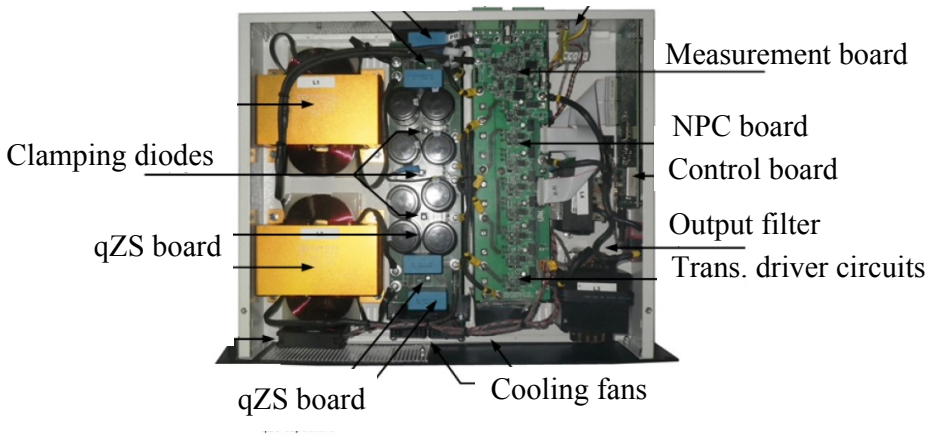
The FPGA (located in the control board) is responsible for all the control algorithms while the microcontroller is responsible for the communication capabilities of the converter.

Full parameters for the three-phase case that guarantee full CCM in the defined operating range, according to previous sections are summarized in Table 2.5.

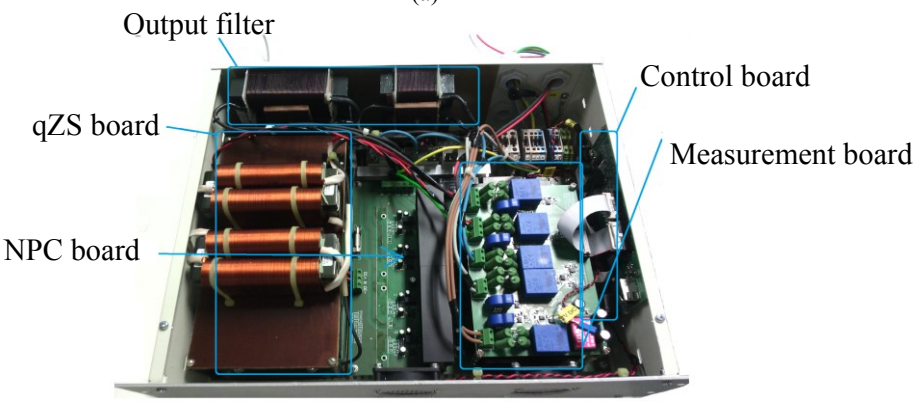
Table 2.5. System parameters of three-phase prototype.

Element	**Value or type**
Control Unit (FPGA)	Cyclon IV EP4CE22E22C8
Transistors Driver Chip	ACPL-H342
Transistors	SiC C2M0080120D
qZS and NPC diodes	SiC C3D10065A
Input dc voltage	300-800 V
Output ac RMS voltage	230 V
Output power	5 kW
THD_U	< 8%
Capacitance value of the capacitors C_1 and C_4	200 µF
Capacitance value of the capacitors C_2 and C_3	200 µF
Inductance value of the inductors L_1 ... L_4	0.9 mH
Inductance of the filter inductor	0.5/0.2 mH
Capacitance of the filter capacitor	0.47 µF
Switching frequency	100 kHz

Pictures of both prototypes (single and three-phase) assembled are represented in Fig. 2.33 a) and Fig. 2.33 b) respectively.



(a)



(b)

Fig. 2.33. Pictures of the final prototypes of 3L-NPC-qZSI. a) Single-phase system. b) Three-phase system.

Chapter 3
Modulation Techniques for Three-Level Neutral-Point-Clamped qZS Inverter

3.1 Introduction

As presented in the previous chapter, VSIs produce several constant output voltage levels. Therefore, in order to build an arbitrary voltage waveform, the inverter has to be controlled alternating the different voltage levels in such a way that the time average (in a switching period) of the switched voltage waveform, or its fundamental component, approximates the desired voltage reference. This procedure is known as modulation, and over the years many different methods have been proposed and used both in industrial and in academia applications. They have different operating principles, implementation schemes and performance and the selection of a specific one is in direct relation to the type of application, its power range, and its dynamic requirements.

3.2 Two-level modulation techniques

The square-wave operation is the most basic and easy to implement modulation scheme for the VSI [79]. As its name suggests, the core idea is to generate an ac square output waveform with the desired frequency. This is achieved by a very simple control strategy based on the comparison between the reference and zero. Note that the square-waveform operation can be used for the single-phase half-bridge, the single-phase H-bridge and a three-phase two-level VSI. Both single-phase solutions have even worse THD_U than the three-phase solution and have little practical use: the low power quality is the price to pay for implementation simplicity and efficiency, since devices switch at fundamental switching frequency.

Sinusoidal pulse-width modulation (PWM), also known as carrier-based modulation methods are the most widely applied modulation schemes for power converters. The main reasons are their simple implementation and good power quality. On the weak side is the need of higher switching frequencies that affect the system efficiency by introducing higher switching losses. On the other hand, if the switching frequency is low, the size, volume and cost of passive elements increase, hence, a trade-off between the power losses and the passive element design cost has to be done. The core idea behind PWM, is to alternate between the different switching states of the inverter in such a way that the time average of the switched voltage waveform equals the desired reference. The modulation is performed by changing the width of the pulses, also known as duty cycle.

Single phase sinusoidal PWM can be classified into categories: bipolar, unipolar and hybrid. For the first one, the output voltage switches between the negative and positive output voltage, while in unipolar the output voltage switches between zero and the positive or the negative output voltage of the inverter. Bipolar PWM techniques can be seen in different applications of single-phase half-bridge and H-bridge topologies while unipolar PWM requires an H-bridge solution. Fig. 3.1 represents the implementation schemes and basic waveforms of a) bipolar, b) unipolar and c) hybrid PWM techniques for H-bridge solution.

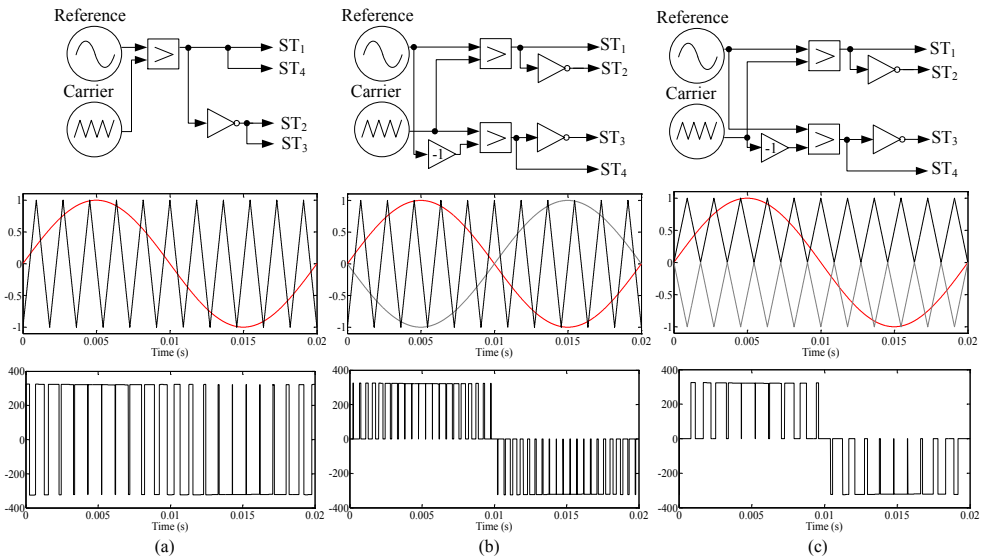


Fig. 3.1. Sinusoidal PWM for H-bridge topology: a) Bipolar PWM, b) Unipolar PWM, c) Hybrid PWM.

The intuitive extension of the same bipolar PWM for single-phase half-bridge will provide the switching pattern for the two-level three-phase VSI, where three reference

signals are phase shifted in 120^0 among each other to obtain a balanced system. Fig. 3.2 illustrates the arranged control signals of the current case.

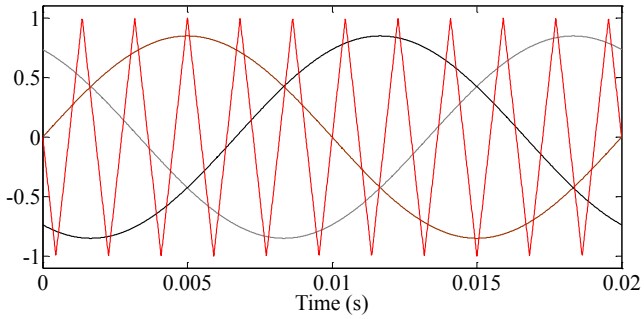


Fig. 3.2. Control signals involved in the modulation for two-level three-phase inverter.

Assuming that in two-level three-phase VSI, six active and two zero-sequence voltage vectors can be generated and that in most three-phase applications, the neutral point is isolated and no neutral current path exists, then any zero-sequence signal can be injected to the reference signals. Recognizing these properties, many researchers have been investigating the zero-sequence signal injections and their proper selection to get different advantages. Depending on the form of the zero sequence voltage added, there are different methods of interest. Those methods can be listed into continuous PWM (CPWM) and discontinuous PWM (DPWM). In the first group the modulation waves are always within the triangle peak boundaries and within every carrier cycle triangle and modulation waves intersect, and, therefore, on and off switching occur. In the second group, the modulation wave of a phase has at least one segment which is clamped to the positive or negative dc rail for at most a total of 120°, therefore, within such intervals the corresponding inverter branch presents discontinuous modulation. Since no modulation implies null switching losses, the switching loss characteristics of CPWM and DPWM methods are different.

Sinusoidal PWM with the third harmonic injection (THIPWM) allows increasing the range of linear operation and decreasing the switching losses. If the third harmonic is 17% [81] of the fundamental one, the maximal linear range is obtained (THIPWM1/6) and, if it is 25% [82] (THIPWM1/4), the minimal current harmonic content is achieved. This technique is obviously into CPWM group and is represented in Fig. 3.3 a).

Other type of CPWM is as follows. The zero-sequence signal of space vector modulation (SVPWM) [83] (Fig. 3.3 b)) compares the magnitudes of the three reference signals and selects the signal with minimum magnitude. Scaling this signal by 0.5, the zero-sequence signal of SVPWM is found. This procedure also allows minimal current harmonic contents as well as symmetrical placement of the zero vectors in the sampling time.

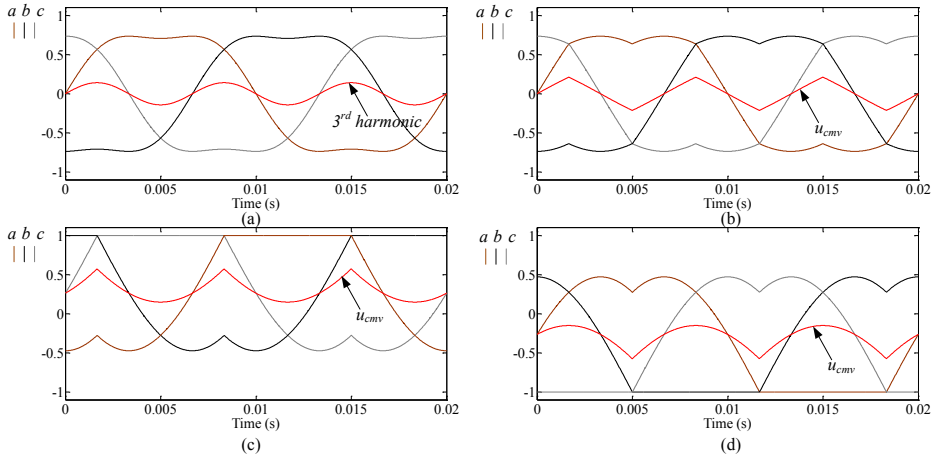


Fig. 3.3. Modulation waveforms of different PWM methods with zero sequence voltage addition (u_{cmv}). a) THIPWM, b) SVPWM, c) DPWMMAX and d) DPWMMIN.

120° DPWM is characterized by a reduction in the number of switching by 25%, but at the expense of having nonuniform thermal stress on the semiconductor devices. Depending on which signal defines the zero sequence (maximum or minimum), it is possible to have DPWMMAX [84] and DPWMMIN respectively (Fig. 3.3 c) and d)). The increased stress, due to 120° conduction of a switch, can be reduced by changing between DPWMMAX and DPWMMIN every 30°. It this way, four special and different 30° DPWM are highlighted, called DPWM0 [85], DPWM1 [86], DPWM2 [87] and DPWM3 [88]. Fig. 3.4 a), b), c) and d) illustrate the main waveforms in each of these zero-sequence signal generation methods respectively.

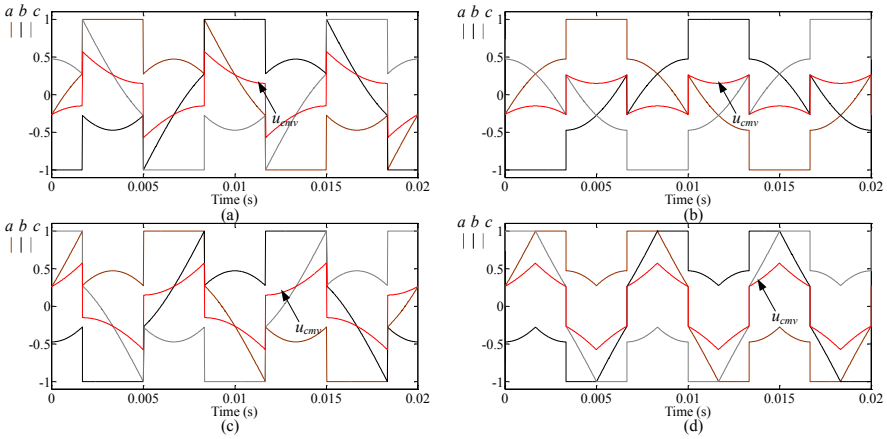


Fig. 3.4. Modulation waveforms of different PWM methods. Continuation. a) DPWM0, b) DPWM1, c) DPWM2 and d) DPWM3.

3.3 Multilevel modulation techniques

The modulation techniques for two-level inverter have been extended for switching of multilevel inverters. They can be classified according to switching frequency [11], as Fig. 3.5 shows. In industrial applications and for high switching frequency, the sinusoidal PWM is very popular [89]-[91]. Here, instead of one triangular carrier, different triangular carriers are used. In level shifted PWM, there are (*k-1*) identical carriers for an *k-level* inverter. The carriers are vertically disposed so that they occupy adjacent vertical bands but, at the same time, those carriers are arranged into the next categories: alternative phase opposition disposition (APOD) [92], phase opposition disposition (POD) and phase disposition (PD). In APOD, each carrier is phase shifted by 180° from its adjacent carrier. In POD, the carriers above the sinusoidal reference zero point are 180° out of phase with those below the zero point. Finally, in PD, all carriers are in phase. A depth review about these methods is found in [93].

When the carriers are not level shifted but phase shifted, it is because in some multilevel topologies this procedure balances the capacitor voltage, mitigates input current harmonic and improves the output voltage spectra.

The SVPWM switching for multilevel inverters also follows the same principle as for two-level. The space vector diagram of a multilevel inverter consists of a number of identical hexagons which are placed in the α-β vector plane at different distances from the centre. The strategy of switching in a multilevel SVPWM involves performing "origin shifting" from outer hexagons, and then using the volt-second balance concept of a two-level SVPWM [94]. Fig. 3.6 represents this procedure, where the reference phasor is shifted to the effective reference phasor and two-level principles are useful. Some triangles (1a, 1b, 2a, 2b and 3) are also highlighted for further explanation.

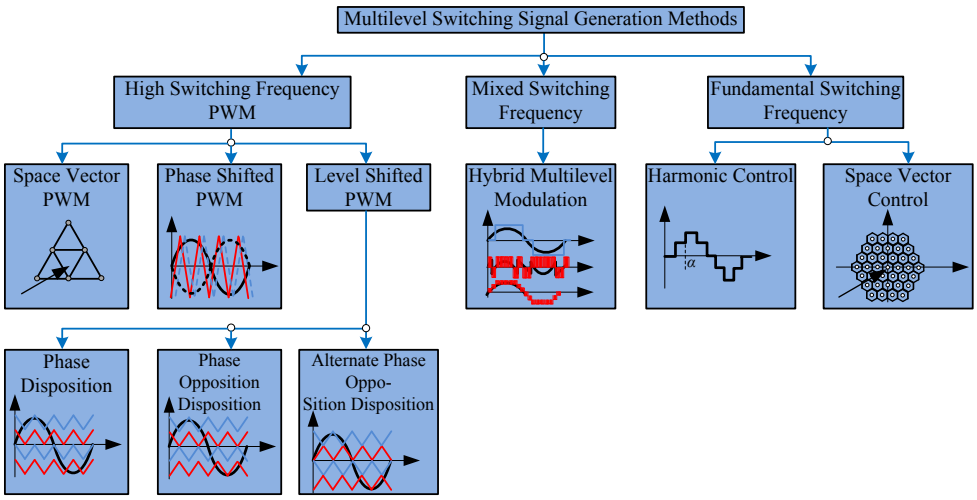


Fig. 3.5. Classification of multilevel modulation methods according to switching frequency.

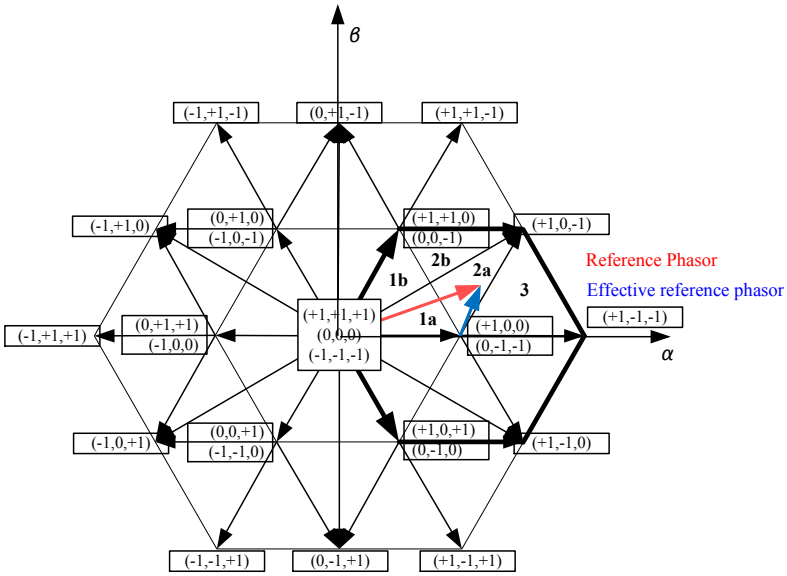


Fig. 3.6. Vectorial representation of states in a NPC inverter.

Hybrid modulation is in part a PWM-based method for some specific multilevel topologies [95]. The basic idea is to take advantage of the different power rates among the cells of the converters to reduce switching losses and improve the converter efficiency. This is achieved by controlling the high-power cells at a fundamental switching frequency by turning on and off each switch of each cell only once a cycle, while the low-power cell is controlled at high frequency.

Although SVPWM and multicarrier PWM are widely accepted and have reached a high level of maturity for multilevel applications, other algorithms have been developed to satisfy particular needs of different applications. Selective harmonic elimination (SHE) [96], for example, has been extended to the multilevel case for high-power applications due to the strong reduction in the switching losses. Moreover, multilevel space vector control (SVC) [97] takes advantage of the high number of voltage vectors generated by a converter with a high number of levels by approximating the reference to the closest generable vector.

3.4 Existing modulation techniques oriented to two-level ZS dc/ac converters

As it was introduced in section 2.3, ZSI family has as main particular feature an additional zero state, the shoot-through state. How to insert this shoot-through state becomes the key point of the PWM control methods for the ZSI. In this section, the equations describing the dc voltage boost factor, the modulation index and the voltage gain

of the two-level three-phase ZSI in the different control method are presented and compared with a particular example by simulation for a better understanding.

3.4.1 Simple boost control

Simple Boost Control (SBC) [8] uses two straight envelope lines equal to or greater than the peak value of the three phase references ($v_{a,ref}$, $v_{b,ref}$ and $v_{c,ref}$) to control D_s. When the carrier triangle wave is greater than the upper shoot-through envelope (v_p) or lower than the bottom shoot-through envelope (v_n), the inverter is turned to a ST. In between, the inverter switches ($T_1, \ldots, T_6$) operate in the same way as in the traditional carrier based PWM control (Fig. 3.7 a)).

In this control method, the voltage gain (G) of the ZSI can be expressed as

$$\frac{\hat{v}_{ac}}{V_{dc}/2} = G = M \cdot B, \tag{3.1}$$

where ^ is the peak value of the fundamental component of the phase-to-neutral output voltage and M is the modulation index. B is determined by

$$B = \frac{1}{1-(2D_s)} \geq 1. \tag{3.2}$$

D_s is equal to (T_0/T_{sw}), where T_0 is the ST time interval over a switching cycle (T_{sw}). For this SBC method, the obtainable D_s decreases with the increase of M, being limited to (1-M), in order to avoid overmodulation phenomena. As a result, in order to produce an output voltage that requires a high voltage gain, a low M has to be used. As analyzed in [8], the voltage stress across the switches is BV_{dc}. From (3.2) and taking into account the aforementioned limitation for D_s, B of this modulation method is given by

$$B = \frac{1}{2M-1}. \tag{3.3}$$

Therefore for any desired B, M can be determined as

$$M = \frac{B+1}{2B}. \tag{3.4}$$

From (3.1) and (3.4), the voltage gain is described as

$$G = M \cdot B = \frac{\hat{v}_{ac}}{V_{dc}/2} = \frac{B+1}{2}. \tag{3.5}$$

As Fig. 3.7 b) shows, using the simple boost control method, the switched output waveform is unchanged in comparison with the voltage source traditional converter (Fig. 3.7 a) but, as desired, its amplitude has increased to a higher value V_s.

3.4.2 Maximum boost control

This technique [99] is graphically explained in Fig. 3.7 c). It is evident that is quite similar to the traditional carrier-based PWM (Fig. 3.7 a)) but turning all zero sates into ST states. Hence maximum D_S and B are obtained for any given M as well as without distorting the output waveforms.

As it can be seen from Fig. 3.7 c), the circuit is in ST state when the triangular carrier wave is either greater than the maximum curve of the references ($v_{a,ref}$, $v_{b,ref}$ and $v_{c,ref}$) or smaller than the minimum of them. As a consequence, D_s varies each cycle. This fact introduces a low frequency ripples in the input current (i_{in}) and dc-link voltage, so a higher size of the passive components is required when the output frequency is low [98].

Due to the inconstant D_s along a time interval and in order to get the voltage gain, it is necessary to determine the average D_s ($\bar{D}_s$). The shoot-through state repeats periodically every $\pi/3$ radians. Assuming that the switching frequency is much higher than the modulation frequency, the D_s (θ) over one switching period in the interval ($\pi/6$, $\pi/2$) can be expressed as

$$D_s(\theta) = \frac{2-(M\,sen\,\theta - M\,sen(\theta - \frac{2\pi}{3}))}{2} \quad . \tag{3.6}$$

The average $\bar{D}_s$ is finally obtained by integrating (3.6) in the analysed period

$$\begin{aligned} \bar{D}_s &= \frac{1}{T}\int_{\pi/6}^{\pi/2} \frac{2-(M\,sen\,\theta - M\,sen(\theta - \frac{2\pi}{3}))}{2}\, d\theta \\ &= \frac{2\pi - 3\sqrt{3}M}{2\pi}. \end{aligned} \tag{3.7}$$

With (3.2) and (3.7), the boost factor with this modulation approach is obtained as

$$B = \frac{1}{1-(2\bar{D}_s)} = \frac{\pi}{3\sqrt{3}M - \pi}, \tag{3.8}$$

and for a given B, now the M is

$$M = \frac{\pi(B+1)}{3\sqrt{3}\,B}. \tag{3.9}$$

Finally, the voltage gain is obtained as

$$G = M \cdot B = \frac{\hat{v}_{ac}}{V_{dc}/2} = \frac{\pi(B+1)}{3\sqrt{3}}. \tag{3.10}$$

For a given B, M in this case is higher than in simple boost control hence the inverter can be operated to obtain a higher voltage gain. As shown in Fig. 3.7 c), the switched voltage waveform is the same than in the voltage source traditional converter but its amplitude has increased to V_s again. As an advantage in comparison with SBC, in Maximum Boost Control (MBC) the voltage stress is reduced since it requires a lower input voltage.

3.4.3 Maximum constant boost control

Fig. 3.7 d) shows the different signals involved in this technique to generate the switching pattern. This achieves the maximum voltage gain while keeping the D_s constant. This fact avoids the undesired effects which were previously mentioned in MBC approach. There are five modulation curves in this control method [100]: three reference signals, $v_{a,ref}$, $v_{b,ref}$ and $v_{c,ref}$, and two shoot-through envelope signals, v_p and v_n. The operation and comparison between signals is similar to the previous cases: when the carrier triangle wave is greater than the upper shoot-through envelope or lower than the bottom shoot-through envelope, inverter is turned to a shoot-through state. In between, the inverter switches in the same way as in the traditional approach.

The upper and lower envelope curves are periodical and have three times the output frequency. There are two half-periods for both curves in a cycle. For the first half-period, $(0, \pi/3)$, the upper and lower envelope curves can be expressed respectively by

$$v_{p1} = \sqrt{3}M + M\sin(\theta - \frac{2\pi}{3}), \qquad \text{for } 0 < \theta < \pi/3 \tag{3.11}$$

$$v_{n1} = M\sin(\theta - \frac{2\pi}{3}), \qquad \text{for } 0 < \theta < \pi/3. \tag{3.12}$$

For the second half-period, $(\pi/3, 2\pi/3)$ both curves are defined as

$$v_{p2} = M\sin(\theta), \qquad \text{for } \pi/3 < \theta < 2\pi/3 \tag{3.13}$$

$$v_{n2} = M\sin(\theta) - \sqrt{3}M, \qquad \text{for } \pi/3 < \theta < 2\pi/3. \tag{3.14}$$

The distance between these curves defines the D_s. For a given M, that distance is $\sqrt{3}\,M$, therefore, D_s is constant and can be expressed as

$$D_s = \frac{2-\sqrt{3}M}{2} = 1 - \frac{\sqrt{3}M}{2}. \tag{3.15}$$

B with this modulation technique can be calculated as follows

$$B = \frac{1}{1-2D_s} = \frac{1}{\sqrt{3}M-1}, \tag{3.16}$$

and M and voltage gain in this case, are calculated according the following expressions

$$M = \frac{B+1}{\sqrt{3}\,B} \qquad \text{and} \tag{3.17}$$

$$G = M \cdot B = \frac{\hat{v}_{ac}}{V_{dc}/2} = \frac{B+1}{\sqrt{3}}\ . \tag{3.18}$$

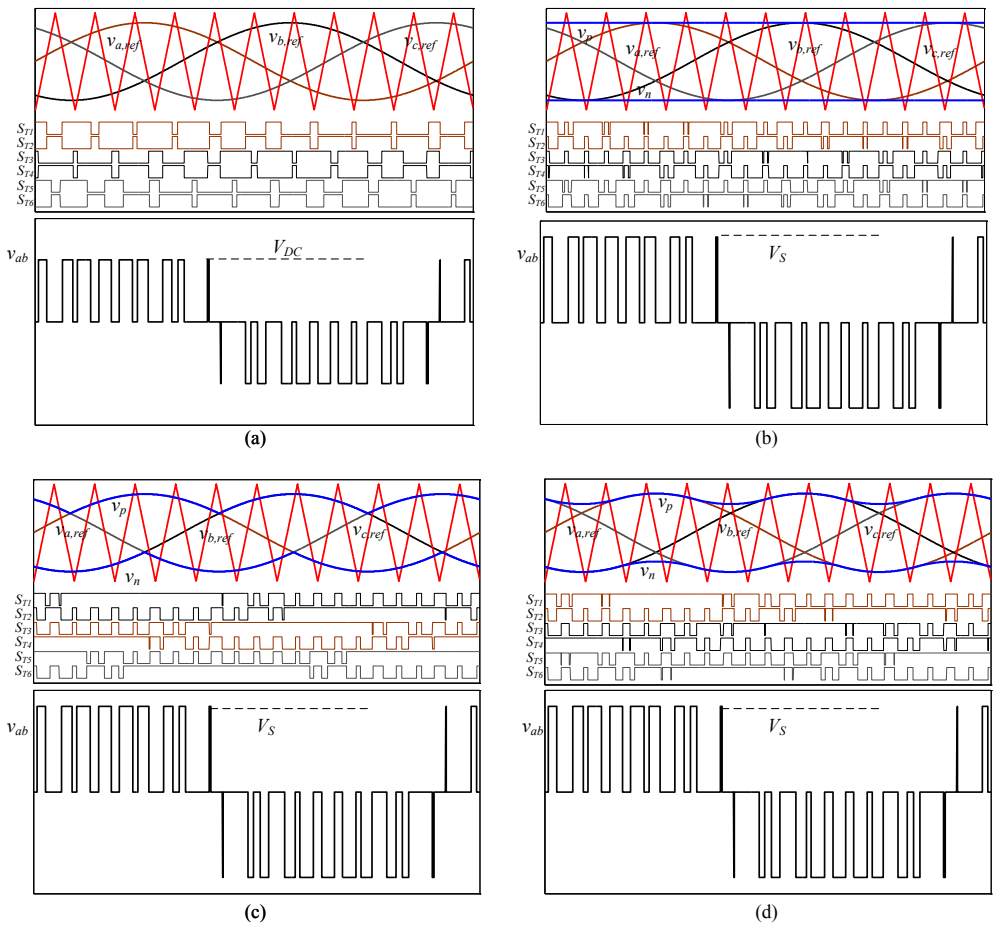


Fig. 3.7. a) Traditional carrier-based PWM. b) Simple boost control method. c) Maximum boost control method. d) Maximum constant boost control method.

Table 3.1 summarizes the equations that define D_s, B and G in each modulation method but, in this case, M is the variable. Finally in Fig. 3.8, the relationship between B and M for each case are represented.

Table 3.1. Summary of different PWM control method expressions as function of M.

Parameter	**SBC**	**MBC**	**MCBC**
D_s	$1-M$	$\frac{2\pi-3\sqrt{3}M}{2\pi}$	$\frac{2-\sqrt{3}M}{2}$
B	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{1}{\sqrt{3}M-1}$
G	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{M}{\sqrt{3}M-1}$

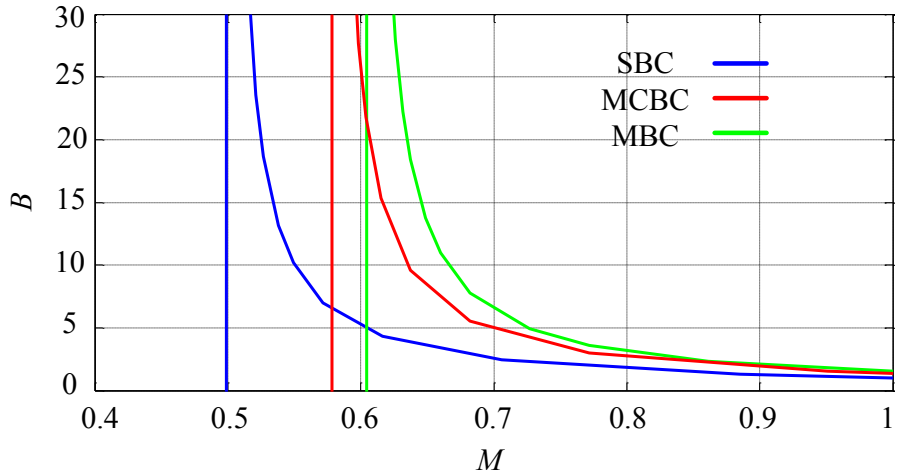


Fig. 3.8. Relationship between B and M in each modulation method.

3.4.4 Analytical comparison

For a better understanding of the aforementioned modulation methods, they are implemented and simulated in a two-level three-phase ZSI. The main purpose is to achieve a B=3 in each control method. Parameters of the simulated system are: V_{dc}=150 V, L_1=L_2=100 μH, C_1=C_2=1200 μF (Z network parameters), the switching frequency is 10 kHz and the R-L load is 6 Ω and 5 mH respectively.

To keep as reference, Fig. 3.9 a) shows the switched line-to-line voltage waveform of the traditional voltage source inverter. The amplitude of the line-to-line switched voltage is equal to the input dc voltage, thus the output line voltage after filtering is (M=0.85) 78 V rms.

The voltage stress across the semiconductors (V_s) and D_s are calculated for the particular case

$$V_s = BV_{dc} = 3x150V = 450V \quad \text{and} \tag{3.19}$$

$$B = \frac{1}{1-2D_s} = 3 \Rightarrow D_s = 0.33\,. \tag{3.20}$$

For the SBC method (Fig. 3.9 b)), it is easy to obtain that M= 0.666 and G= 2. In this case, the amplitude of the switched line-to-line voltage has increased up to 450 V and the output line voltage after filtering, is in this case, 185 V rms.

M and G of the Z-source inverter in the MBC (Fig. 3.9 c)) method are M= 0.806 and G= 2.4 respectively. This technique produces a higher voltage gain than the SBC. This fact is illustrated with the output-line-to-line voltage after filtering, with rms value equal to 222 V.

In the last modulation method (Fig. 3.9 d)), where a MCBC is used, M= 0.769 and G= 2.3 are obtained.

According to the THD of the output current, it can be observed that using the MBC, the power quality is sacrificed since the unequal distribution of D_s produces low frequency ripples in the dc side (Fig. 3.9 c).

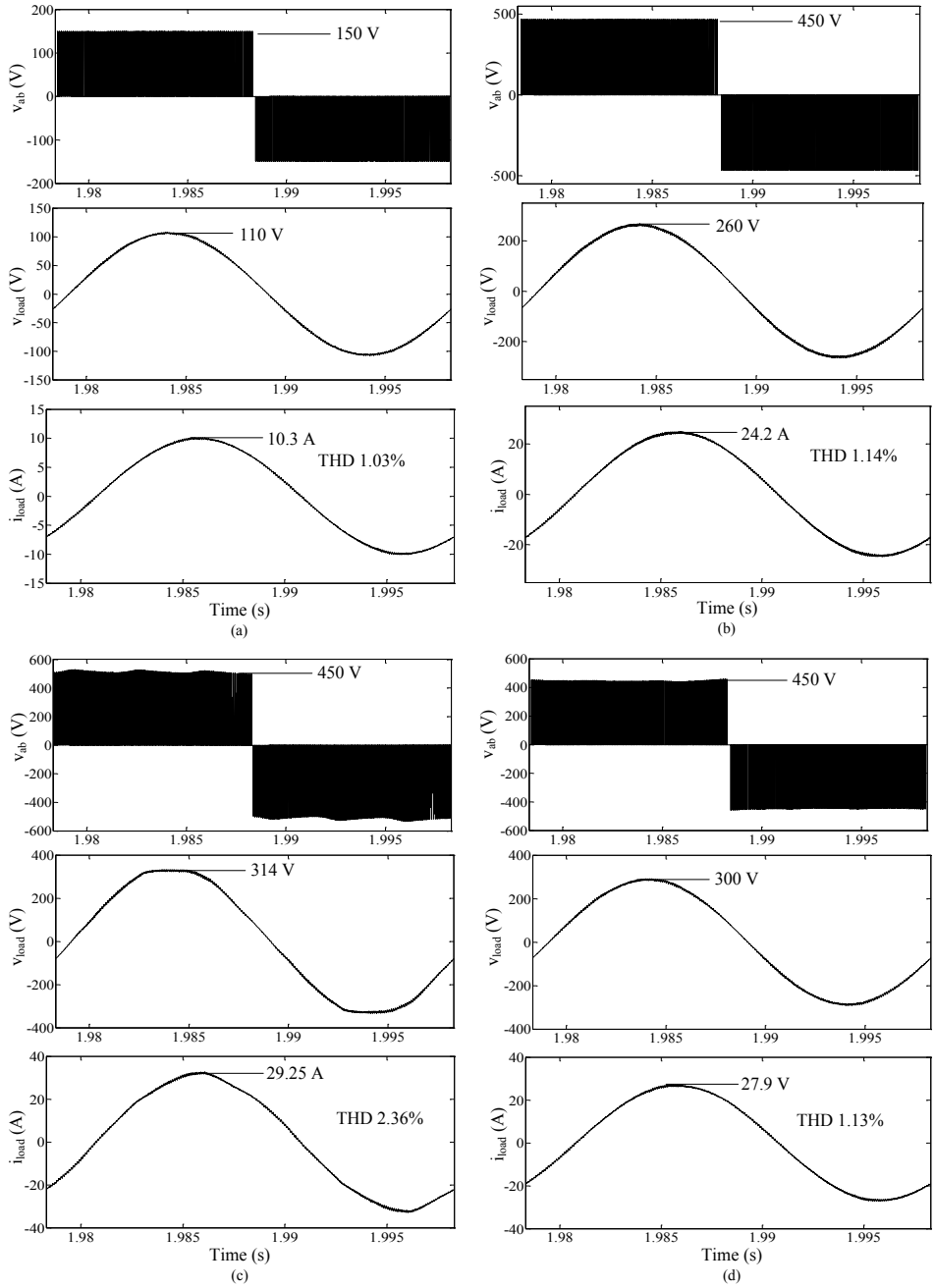


Fig. 3.9. Simulation waveforms of: a) VSC with traditional sinusoidal PWM, b) ZSI with simple boost control, c) ZSI with maximum boost control, d) ZSI with maximum constant boost control.

3.5 Modulation techniques for ZS multilevel dc/ac converters

3.5.1 State of the art

When an appropriate modulation technique is being designed for this kind of power converter, the following common requirements are set to carefully embed the shoot-through states into the conventional switching signals:

- no violation of normalized volt-second balance in the output voltages during the fundamental period
- minimum number of extra-commutations in the switches
- lower semiconductor stress
- minimum total harmonic distortion
- maximum voltage-boost
- minimum complexity of implementation.

The initial work that deals with the development of switching signal generations for this family of inverters is found in [37], being devoted to the topology shown in the Fig. 2.18 a). First PWM approach is derived from the optimized PWM sequences of a conventional two-level ZSI and the Nearest Three Vectors (NTV) modulation principle in a conventional NPC inverter. The arrangement of reference and carrier signals is depicted in Fig. 3.10 a) and, as main feature, the resulting switching pattern avoids extra device switching signals (six per half switching period). Each impedance network (upper and lower) is short-circuited sequentially with equal time intervals (half the total shoot-through duration) in order to avoid dc voltage unbalance. In this strategy, as a core idea, the maximum and minimum voltage reference signals (in each switching period) are modified with an offset (MR_1 and MR_2) and then compared with the set of carriers to generate the upper and lower ST states (just one phase-leg, A, B or C is shooted- through). Operating in this way, the volt-second average per switching cycle is maintained and a minimum harmonic distortion is obtained. To enhance the boost factor, the injection of third harmonic offset [101] is also added to the reference signals.

Fig. 3.10 b) shows a vectorial analysis when the two-level effective voltage reference phasor is located in a certain triangle of the SV representation (triangle *2a* in Fig. 3.6) and the shoot-through interval ($T_0/2$) becomes longer than the active state {0,0,-1}. It is interesting to remark that the intermediate located reference signal ($Ref,_b$ in the illustrated case) does not trigger any shoot-through, hence it is a difference with the two-level Z-source PWM formulation. This PWM scheme is also valid for a trans-Z-Source NPC inverter (Fig. 2.23 a) and b)) [49] and for topologies shown in (Fig. 2.24 a) and b)) [50].

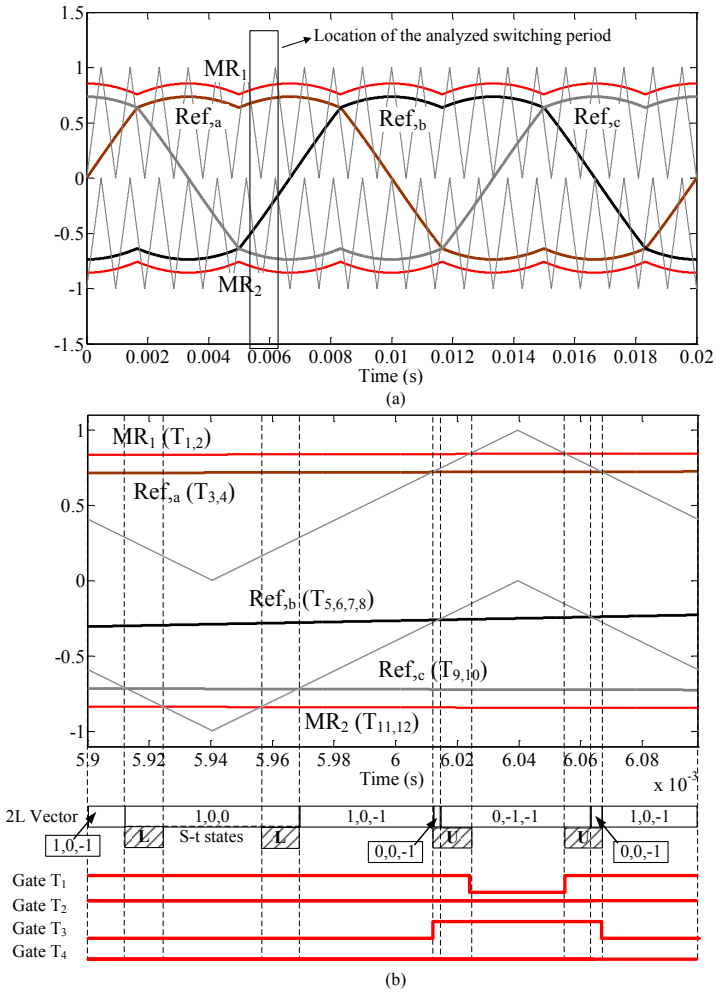


Fig. 3.10. NTV/MR PWM scheme. a) Reference and carrier arrangement. b) Vectorial analysis of a switching period.

The second proposed principle from aforementioned references (Fig. 3.11) is devoted to eliminate the common-mode voltage (if the reference grounding point is chosen between both ZSNs). This switching pattern is created by a proper logical mapping between the two-level Z-source sequence and the seven states of the Reduced Common-Mode (RCM) three-level vector diagram. Both the upper and lower Z-source networks are short-circuited simultaneously since the dead time delays are not needed. The arrangement of reference and carrier signals is depicted in Fig. 3.11 a). Fig. 3.11 b) shows the vectorial analysis when the two-level effective voltage reference phasor is located in triangle *2a* (Fig. 3.6) as well.

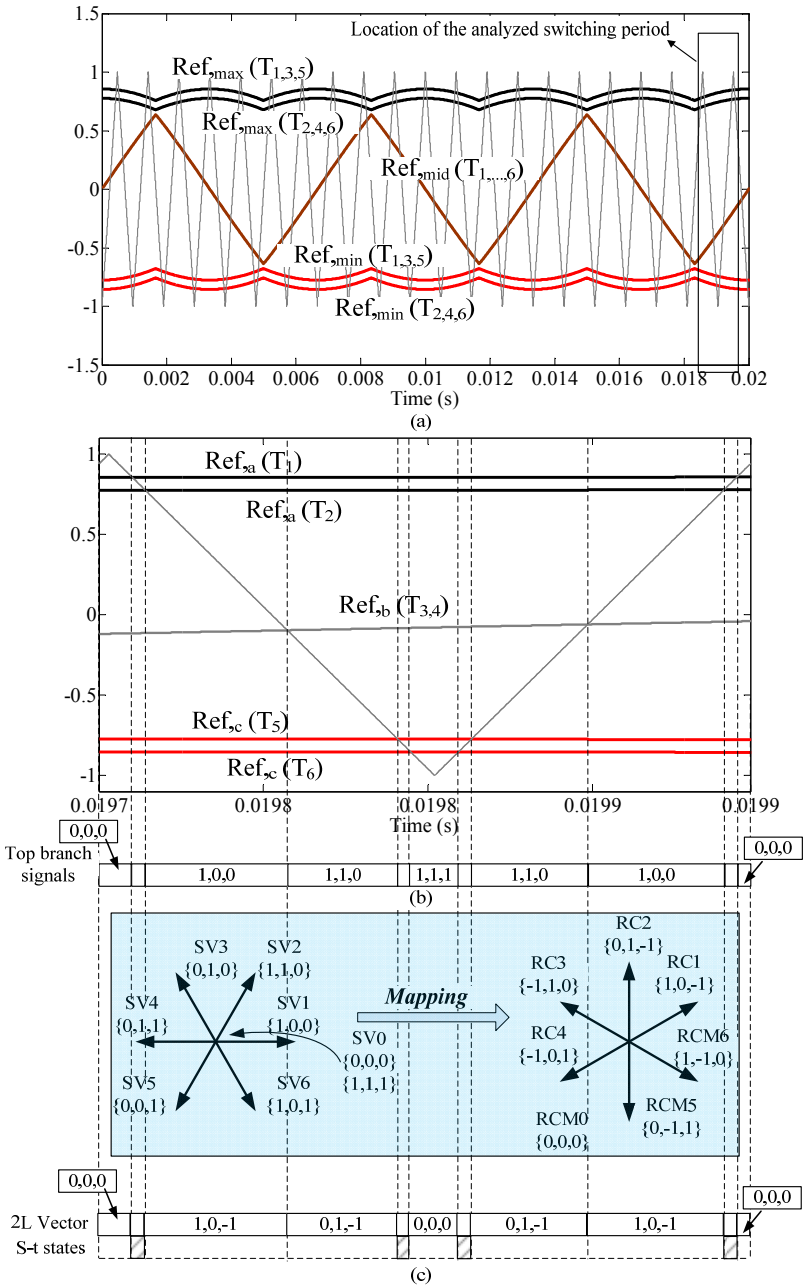


Fig. 3.11. RCM PWM scheme. a) Reference and carrier arrangement for two-level (2L) formulation. b) Vectorial analysis for 2L formulation in a switching period. c) Logic mapping from 2L to RCM 3L.

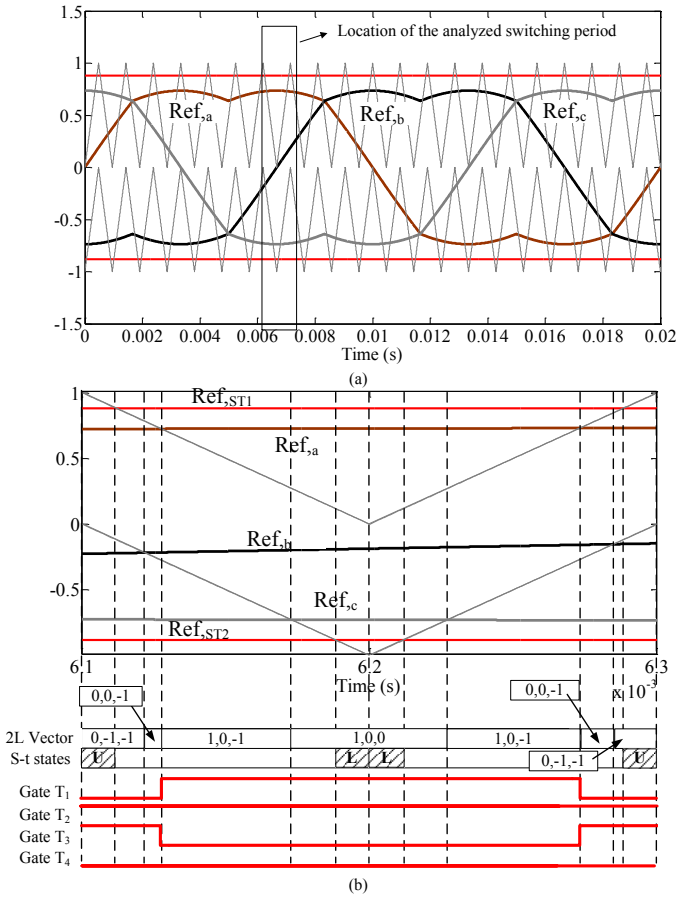


Fig. 3.12. EI scheme. a) Reference and carrier arrangement. b) Vectorial analysis of a switching period.

In references [102]-[103] the aforementioned concepts are extended and clarified, proposing a number of continuous and discontinuous PWM schemes for the same topology. Continuous Edge Insertion (EI) (Fig. 3.12 a) and b) show the arrangement of references and carriers and the vectorial analysis respectively) PWM with symmetrical voltage boost is very similar to NTV derived technique, but getting fixed ST state positions into zero states and equal durations regardless of the sextant which the reference voltage is in. This fact minimizes the current ripple flowing across the Z-source network but at the expense of eight device commutations.

The so called continuous Modified Reference (MR) PWM is the same than the first presented (NTV, Fig. 3.10) but it is much better clarified how it is needed to shift some active states (in some particular triangles of Fig. 3.6) to compensate the zero output

voltage generated by ST states, keeping the normalized volt-second average. In order to reduce the number of state transitions, a new ST modulation strategy was derived based on the conventional 60º discontinuous PWM and the MR PWM. The modification included over MR PWM is just in the reference offsets, because these ones have to be changed periodically (which increase the complexity). Also it is reported problematic because just one Z-source network per 60º sextant is short-circuited (which limits its application). The same reference signals but with triple offset is proposed in [104] and with the equal alternation of reference offsets to generate the ST, the common mode voltage is limited. Discontinuous schemes are not recommended since they give rise to a large current ripple. If the optimization of control algorithm is the priority, a good solution is found in [105], where the SVPWM and triangular-comparison PWM approaches are combined for controlling the converter operation.

For the topology drawn in Fig. 2.18 b), its modulation principle is summarized briefly in [38] (also useful for DCLC inverter topology). The APOD with 180º arrangement (Fig. 3.13 a) and b) show the arrangement of references and carriers and the vectorial analysis respectively) is considered for carriers because it creates multiple null intervals for ST insertion, which is generated with the aim of looking for the minimum losses. ST is achieved by a proper synchronization of turning on switches from two selected phase legs, instead of turning on all switches from the same phase-leg simultaneously. Additional references can be programmed with the offset (T_0/T) to the maximum and minimum reference in each switching period. As this technique is not based on NTV, it has higher THD values. To solve this undesired result, the application of PD technique (as Fig. 3.10 shows) is studied in [106] (this topology is called Reduced Element Count (REC)). A similar approach of this PWM based on NTV is detailed in [107] and derived from SVPWM for a simpler implementation and improved harmonic performance [108]. Basically, duty ratios of the nearest three vectors to be applied by the converter in any SVPWM triangle are calculated. After this, a new methodology is proposed, which generates a new switching sequence in comparison with the previous one, to insert the ST states while the volt-second balance and minimal commutation count are maintained.

For the DCLC with two ZSNs (Fig. 2.20), a ST method is presented in [44] for each (upper and lower) networks sequentially to avoid volt-second balance violation, which is equal to the proposed technique presented in [37] (NTV) and [103] (MR PWM) for 3L-NPC-ZSI. This modulation design has constrains since no redundant switching states within a phase leg are available to equalize the losses.

Modulations for topologies depicted in Fig. 2.20 b) and c) are also explored in [44] and, in those cases, there are some redundant states and, as a result, additional modulation approaches can be designed to equalize the losses. In the case that two Z-networks are involved, the PWM scheme can be the same as for the case of DCLC just modifying the comparisons between reference and carriers (Fig. 3.10) but, it would give a

poor utilization of the redundant switching states. As an alternative, a derived method is proposed from the phase-shifted-carrier (PSC).

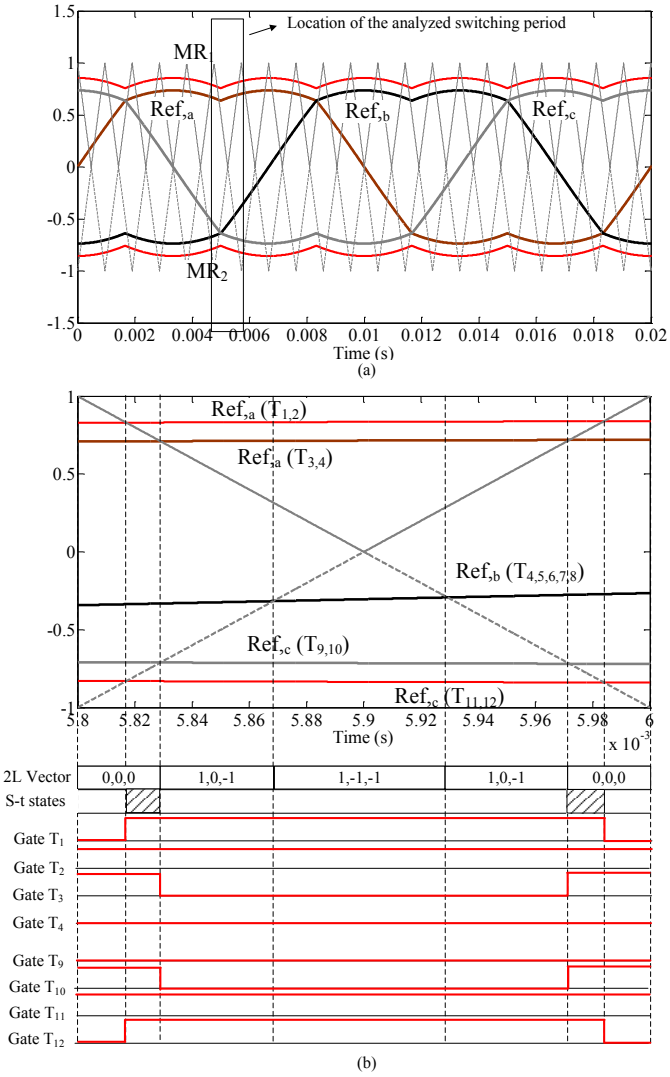


Fig. 3.13. APOD scheme. a) Reference and carrier arrangement. b) Vectorial analysis of a switching period.

The reference voltage signals (with or without the triple offset) and their negations are compared with a common triangle carrier to generate the switching pattern for the upper and lower inverter bridge. It is interestingly demonstrated that shoot-though produces a simultaneous boosting (when offset of SVPWM is used) of the two Z-sources

(one phase from the upper bridge and other phase from the lower one), which allows the replacement from two Z-networks to one. This last reason makes the PSC better for the dual Z-source inverter control even though its THD_U is higher in comparison with PD of carriers. It is justified because the NTV modulation principle cannot longer be used. A simplification for this methodology was also done in the same work, by using three sinusoidal references, two linear references (for inserting the ST) and a carrier, but at the expense of two additional device commutations. Modification of these schemes are found in [109], including a slight modification in the PWM sequence, the Dual Z-source inverter with one or two impedance network can work with RCM and perform bidirectional power conversion. A methodology based on generating the switching pattern for the upper 2L inverter (similar to Fig. 3.11) and then, by a bit-shifting technique, to generate the pattern for the bottom 2L inverter is proposed. Besides the operation of this topology is studied under semiconductor failures and a reconfiguration of the gating signals is proposed. The RCM performance is still maintained when the two input sources are involved.

If the inverter circuitry is built with four legs [110], the reference signals have to be regenerated according to the unbalanced or balanced load conditions. In the case of having two Z-source networks, the offset (required for 4 legs operation) added to the reference signals for optimal switching is expressed in [111] before being compared with two PD arranged carrier. The ST states are inserted by an appropriate interleaving (one ST per network and switching period) which allows a balanced voltage boosting between upper and lower network and minimal commutation counts. It is done by a similar technique than in Fig. 3.10 (MR/NTV derived). A greater number of ST per switching period by a proper modulation technique would derive in a different distributed energy between the Z networks and in a more complex algorithm. If just one Z-network is presented as input stage of the four-leg multilevel bridge, the modulation principle based on APOD carrier arrangement [38] (similar to Fig. 3.13 but with four references) is proposed, in order to obtain absolute null (zero line voltage) states, which result in a worse THD. For five legs in the inverter bridge, the fifth harmonic injection optimizes the harmonic performance and increases the modulation index and, PD or APOD carrier arrangement are used again for two Z-network or one respectively in a similar sketch than previously presented.

In [112], a new phase shifted PWM devoted to qZ source CMC is proposed. Its scheme is composed by two sets of three reference signals (for the left and right leg respectively) and one set of three carriers, one per module (each layer of the modules has the same carrier). The most particular feature of this method is that the carriers change their amplitudes according to the envelopes of the references. To embed the ST states, the SBC is included. As main achievement, a power loss reduction is remarked. In [113] a SVPWM for a single phase qZS-CMC can be found, where the total ST duration is equally distributed into the zero states. The extension of this SVM derived technique to the three phase system is explained in [114] and [115].

Modulation of 5L Z-source inverter (Fig. 2.19 b)) was experimentally validated in [43]. The PWM arrangement is very similar to MR in [103] but, in this case, 4 PD carrier waves are required as well as a different triple offset for the references [116].

3.5.2 Proposed modulation techniques for three-level neutral-point-clamped qZS inverter

This section explains and summarizes the main contributions and novelties in this field. Once the previous concepts and the existing spectrum of modulation techniques for this family of power converter were reviewed, different modulation schemes were developed both in single phase system (Fig. 2.25) and in three-phase system (Fig. 2.28) based on three-level NPC qZ source inverter.

Fig. 3.14 shows a sketch of the proposed modulation technique for the single phase topology in its first approach.

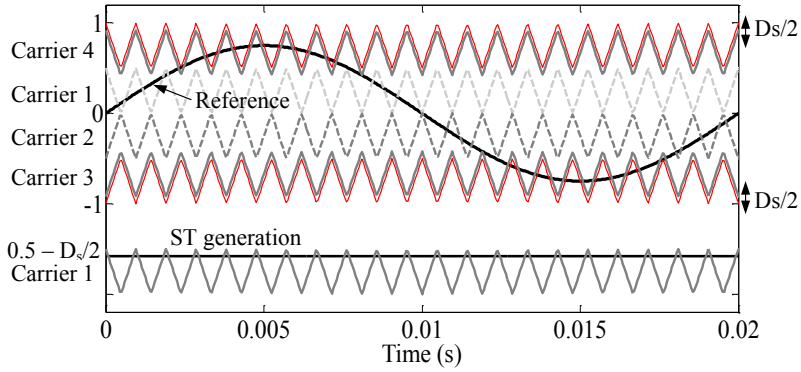


Fig. 3.14. Sketch of the proposed modulation technique with uniformly distributed shoot-through states and constant width.

One reference modulating sinusoidal wave and four triangular carriers (Ci) are compared to obtain the different states of T_1, T_2, T_5 and T_6 and T_3, T_4, T_7 and T_8 have the complementary state of the other one respectively (Fig. 3.15).

Carrier 1 is used to generate the ST states in comparison with a constant value that includes the desired D_s value. Operating in this way, uniformly distributed shoot-through states with constant width during the whole output voltage period can be achieved.

In order to compensate the average output voltage (V_{ab}) when the ST states are applied, leg B must solve this situation through the change of the voltage v_{bo} (voltage between middle point of the branch and neutral point). Fig. 3.14 and Fig. 3.15 show how we can obtain this compensation. During the positive semi-cycle, leg B has to produce $v_{bo} = -V_{dc}/2$ more times to restore the average voltage V_{ab}. This is produced through carrier 4

displacement that generates the pulses of T_6. During the negative semi-cycle the same situation is produced. Leg B has to produce $V_{BO} = +V_{dc}/2$ more times to restore the average voltage V_{AB}. This is produced through carrier 3 displacement that controls the pulses of T_5.

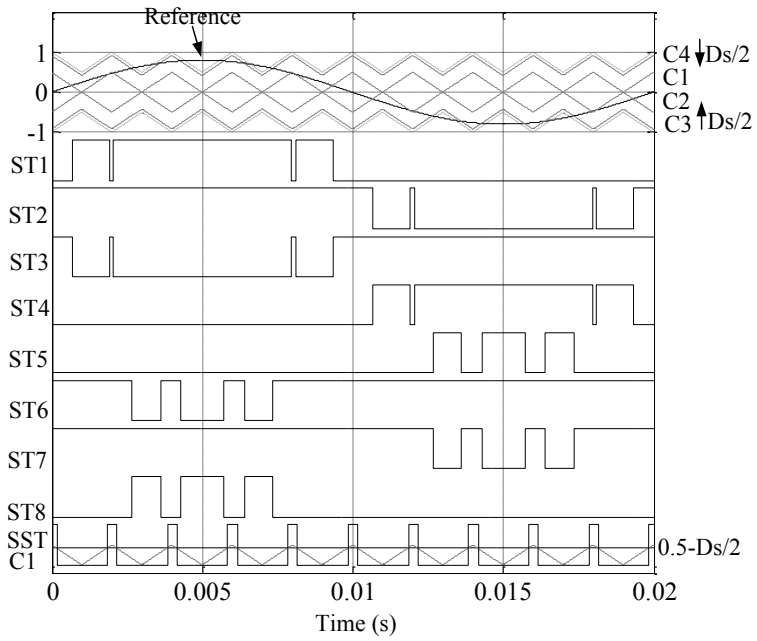


Fig. 3.15. Switching pattern of the first proposed modulation technique.

This modulation technique has been implemented and used in different works with success (papers [**d**] and [**g**] in appendix). But, at the same time, it is observed that switching signals and duty cycles (directly connected with power losses) of switches are quite unbalanced inside of each branch. This phenomenon can be observed in Fig. 3.15.

Second modulation technique improved for single-phase system

To solve such undesired situation, a second version of the modulation technique is proposed (Fig. 3.16). In this case, it is possible to balance the power losses between branches and even between switches of each branch. Those power losses are produced during switching states (switching losses) and also during on states (conduction states) in each power switch. Both losses must be taken into account in order to distribute them among branches of the converter. In this way different rates of the converter are improved such as: Mean Time to Failures (MTTF) and Mean Time between Failures (MTBF). As a consequence, the reliability and the useful life of the converter will increase.

Two modulating sinusoidal waves (Ref_a and Ref_b, one per branch) are compared to two level shifted triangular carriers in phase disposition. The result of this operation is obtaining the normal states of T_1, T_2, T_5 and T_6. T_3, T_4, T_7 and T_8 have the complementary states of the other ones, respectively. It is easy to detect in Fig. 3.17 that switching states of analogous switches are the same in both branches hence power losses will be also the same.

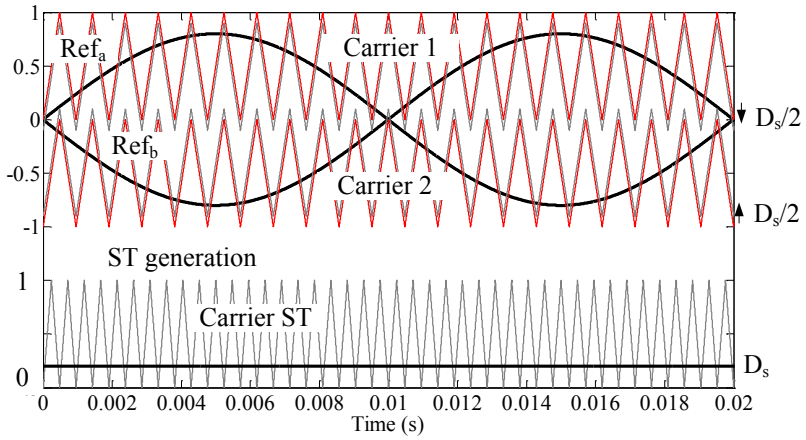


Fig. 3.16. Sketch of the proposed modulation technique with balanced power losses.

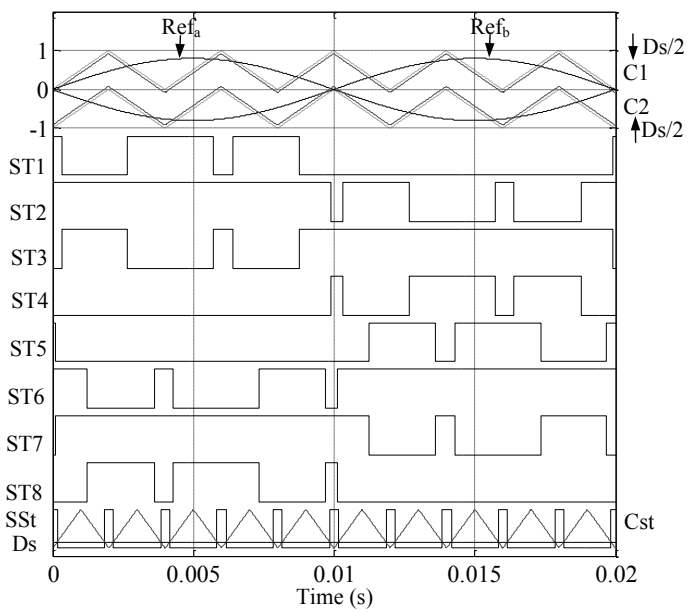


Fig. 3.17. Switching signals generation of the second proposed modulation technique.

The generation of the ST states is done by means of the comparison between D_s and one triangular carrier (C_{st}) with double frequency than the other carriers. Operating in this way, the symmetry of the output voltage is maintained. At the same time it is required to compensate the average output voltage (V_{AB}) when the ST states are applied. It is done by shifting C_1 and C_2 quantities $-D_s/2$ and $D_s/2$ respectively. Fig. 3.18 illustrates the implementation sketch of the new proposed modulation technique.

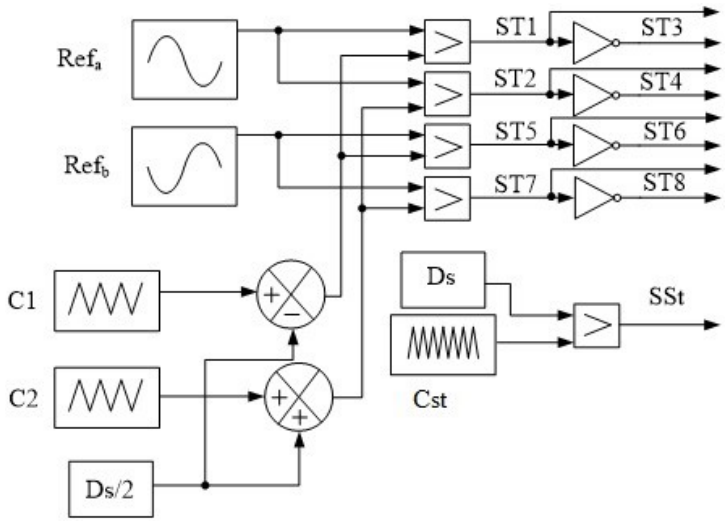


Fig. 3.18. Sketch of the implementation of the second modulation technique.

Both approaches are analytically compared by simulations to validate the predictions according to different criteria.

First of all, the number of switching transitions (times) per switch during one fundamental period (defined at 50 Hz) was analysed in both modulation techniques. This number or parameter is related to the switching losses and is represented in Fig. 3.19 a) and Fig. 3.19 b) for each modulation technique as a function of modulation frequency index (m_f) respectively (D_s is equal to 0.16).

Secondly, the duty cycle of each switch was calculated. This value is related to the conduction losses and is represented in Fig. 3.19 c) and d). Branch B has a high level of conduction unbalance between its switches (T_6 and T_7 conduct 2.6 times more than T_5 and T_8) and also a different duty cycle to the analogous switch from branch A. New proposed PWM provides the same conduction time (T_{on}) of each analogous pairs of switches between branches and less unbalance within the branch.

We can conclude that by using the second proposed modulation technique, both branches are symmetrically balanced from the point of view of switching and conduction losses. Also this balanced situation is inherited by the clamped diodes. Therefore, rates as MTTF, MTBF and reliability of the converter are improved [**b**].

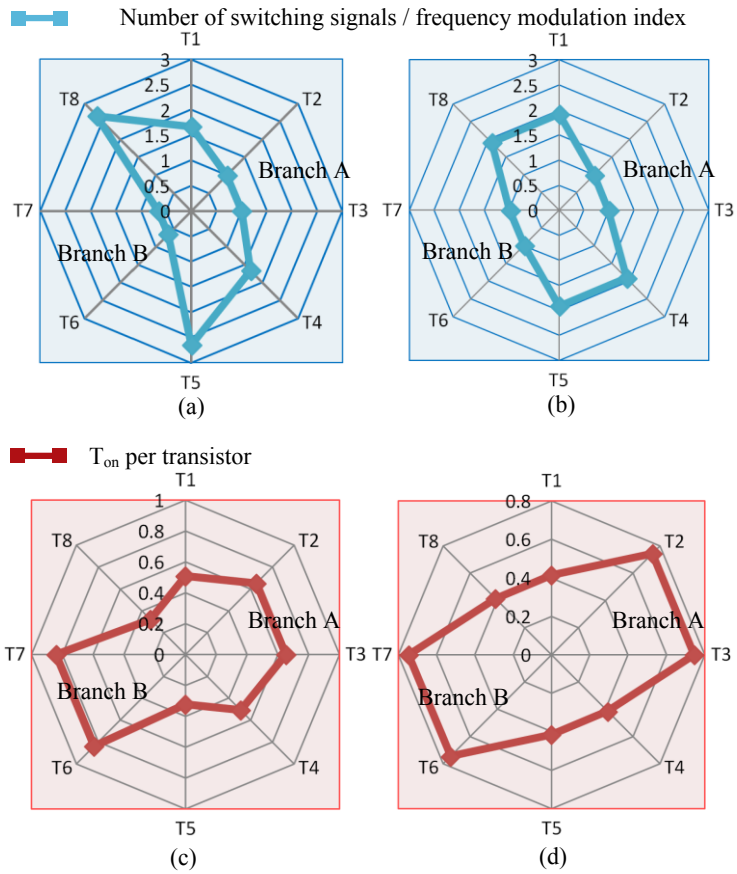


Fig. 3.19. Number of switching signals per switch/m_f in one fundamental period. a) First modulation technique. b) Second proposed modulation technique. T_{on} per switch during one fundamental period. c) First modulation technique. (d) Second proposed modulation technique.

Modulation technique for three-phase system

The second proposed modulation technique for the single-phase inverter was extended to propose a new one for the three-phase topology (Fig. 2.28). Fig. 3.20 shows a sketch of the PWM signals. Three modulating waves (one per phase) and two triangular carriers (upper between 0 and 1 and lower between -1 and 0) are compared in order to obtain the different normal states of T_1, T_2, T_5, T_6, T_9 and T_{10}, while T_3, T_4, T_7, T_8, T_{11} and T_{12} have the complementary state of the other ones, respectively.

Third harmonic injection is used to increase M and as consequence, G is also increased at the same proportion.

Expressions for reference voltages are

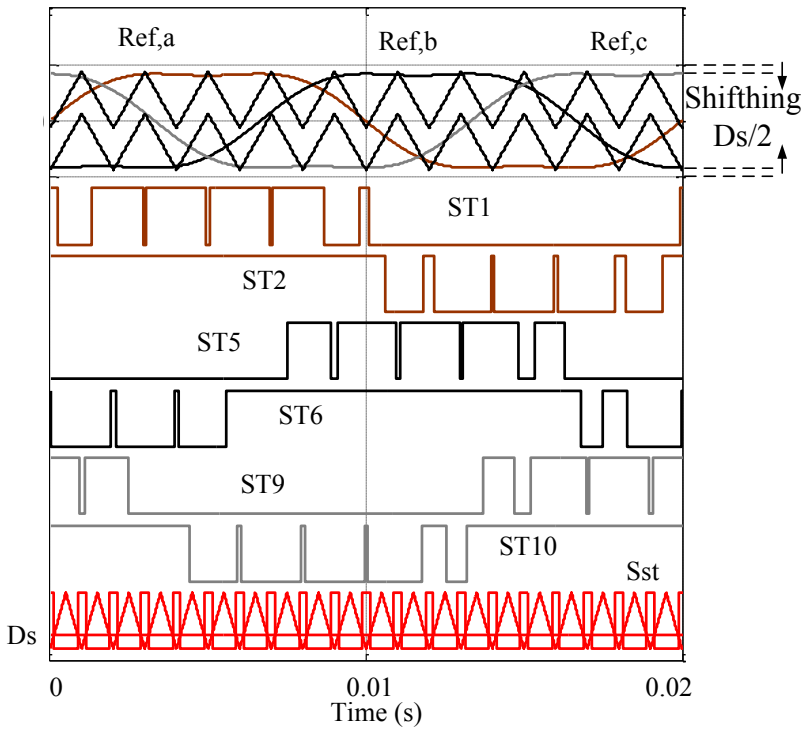


Fig. 3.20. Sketch of the proposed three-phase PWM technique.

$$\mathrm{Ref}_i = 1.15\,M\,sin(\omega t+\varphi_i)+0.19\,M\,sin(3\omega t)\Big|_{\substack{i=phase\,a,\,phase\,b\\ and\ phase\,c.}} \cdot \tag{3.21}$$

Another carrier signal ($\in$ [0,1]), but at double frequency, is used to generate the ST states by means of comparison with the constant value of D_s. Operating in this way, uniformly distributed ST states with constant width during the whole output voltage period are achieved.

Due to the insertion of shoot-through, the output average phase-to-neutral voltage values are modified and it is necessary to restore the normalized value. In order to maintain constant output average voltages, upper and lower carriers are displaced $D_s/2$ down and up respectively and the reference value will be ensured. Fig. 3.21 shows the implementation sketch of proposed modulation technique.

More details about these new proposed modulation techniques are found in papers [**b**], [**d**], [**e**] and [**g**] in appendix.

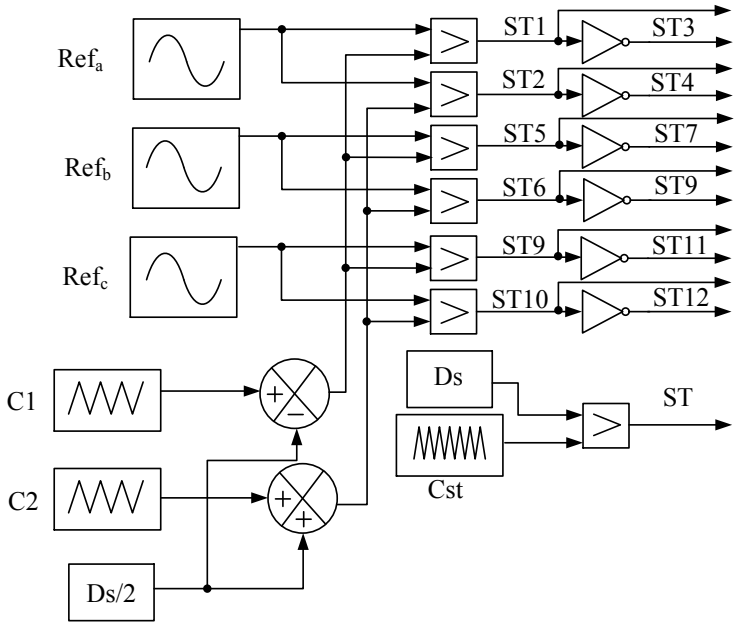


Fig. 3.21. Implementation sketch of the proposed three-phase PWM technique.

3.5.3 Experimental results

In order to prove all theoretical assumption, the experimental investigation was carried out for the single phase prototype explained in section (2.5.2). This first test was performed under 800 W output power and switching frequency at 100 kHz. The first goal is to demonstrate the differences between both modulation techniques approaches [**b**] and [**d**].

In Fig. 3.22 a) and Fig. 3.22 b) the gate-source switching signals of the first modulation technique without and with ST are illustrated respectively. It is evident that each transistor is working in a different way. In all subfigures from up to down the switching signals of transistors correspond to T_1, T_2, T_5 and T_6. Fig. 3.22 c) and Fig. 3.22 d) show the similar switching signals for second modulation technique. In this case the switching signals of both branches are balanced.

Fig. 3.23 a) and b) show the thermal pictures of the power board where driver circuits along with transistor terminals are located. These pictures show the gate resistors (R_G) of the transistors T_1, T_5 under first and second modulation strategies respectively. Higher temperature of the gate resistors T5 confirms higher switching numbers of this transistor in the first modulation. Fig. 3.23 c) and d) illustrate the temperatures of the transistor chips that are located under the board on the radiators. In the first modulation (Fig. 3.23 c)) a difference between the temperatures of the different branches is presented. This difference is mitigated under second modulation strategy (Fig. 3.23 d)).

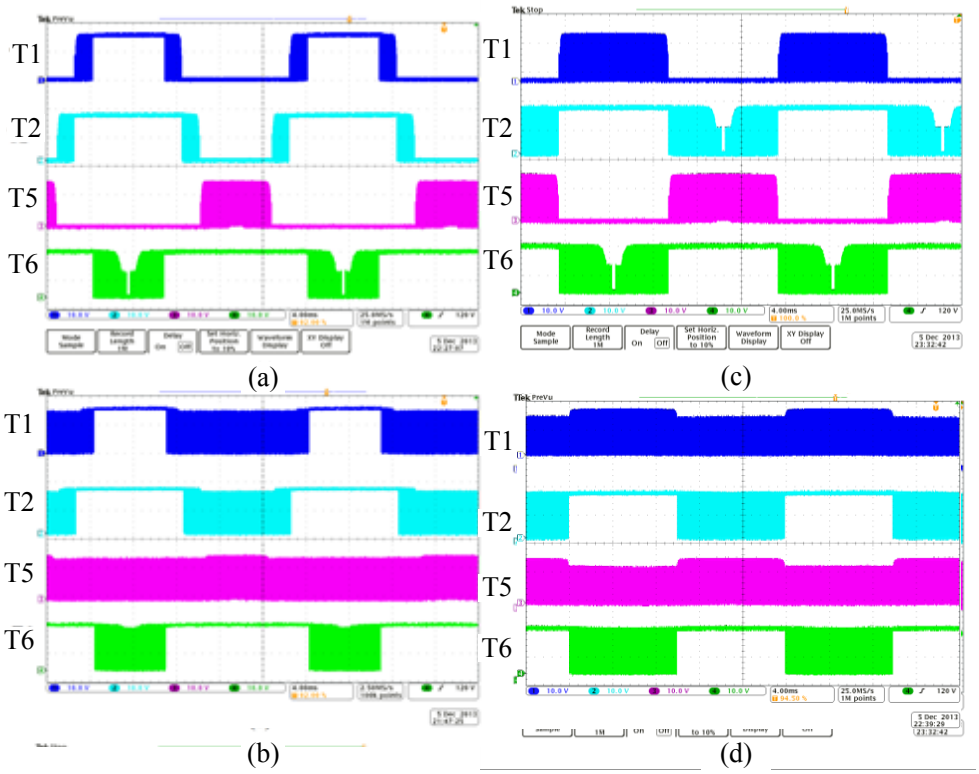


Fig. 3.22. Gate-source switching signals of the first (a, b) and second (c, d) modulation techniques without (a, c) and with (b, d) ST states.

To analyse the operation and to observe the main operation waveforms, now the test that was carried out is explained. A passive resistor was used as load. The regulated dc power supply was used as input voltage source. All measurements were made by digital oscilloscope Tektronix DPO7254, current probes Tektronix TCP0030, and voltage probes Tektronix TPA-BNC.

Fig. 3.24 a) and b) represent the experimental results without and with the ST states. It can be seen that i_{in} is in CCM. The voltage of the capacitor C_1 is near zero in the first case. The capacitors C_3, C_4 have identical voltage waveforms. It reveals that the capacitors provide a stable dc-link voltage. In the first test point, the input voltage was set to 325 V that corresponds to the VSI mode where ST states are not required. It can be seen that the output LC-filter is sufficient in order to provide acceptable output voltage quality (THD_U lower than 5%).

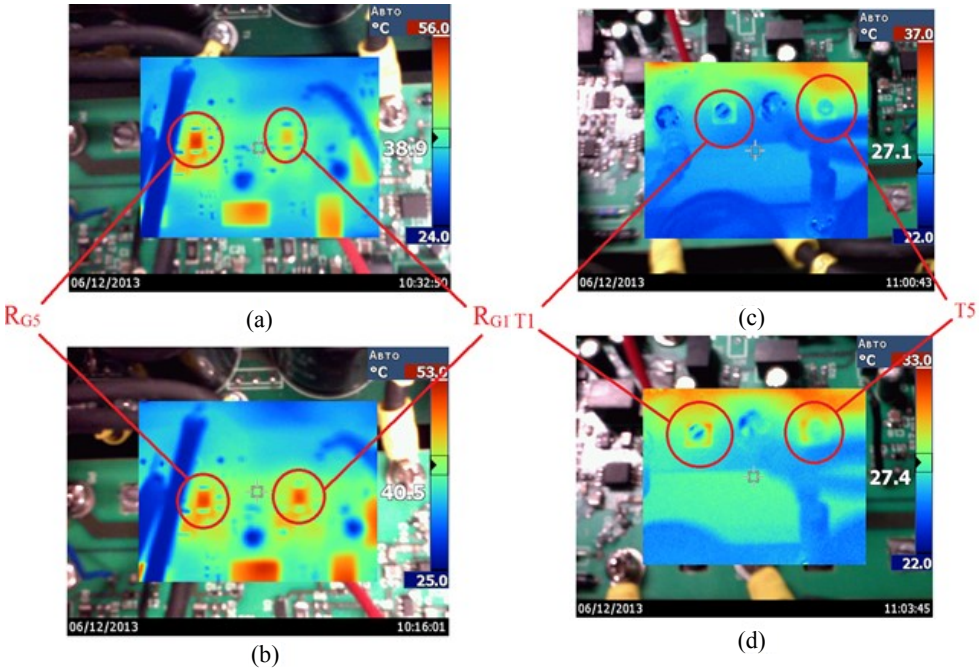


Fig. 3.23. Thermal pictures of the gate resistors of the transistors T1 and T5 under a) first modulation and b) second modulation technique. Thermal pictures of the transistor chips T1 and T5 under c) first and d) second modulation technique.

Fig. 3.24 b) presents similar results with D_s=0.16. The main idea is to maintain the constant output ac voltage during variable dc input voltage. In the second test point, the input voltage is decreased from 325 to 265 V. As can be seen, the inverter operates in the CCM. As it can be checked, input voltage has been boosted to maintain the nominal value in the output by means of ST states. They are revealed by comparing V_{ab} from a) and b). In the second case, V_{ab} goes to zero during whole operation period.

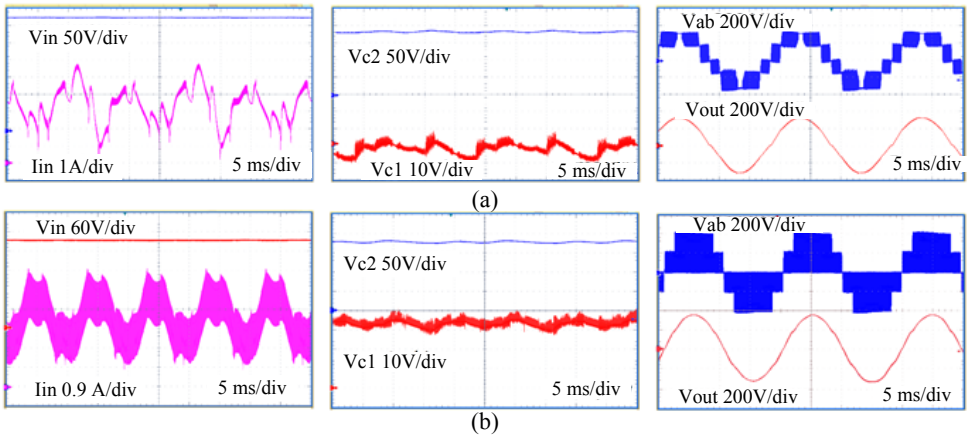


Fig. 3.24. Experimental results of the single-phase 3L-NPC-qZSI. a) Without ST. b) With ST.

Fig. 3.25 summarizes the experimental study of the *G*, the efficiency and the THD of the output voltage. The experimental *G* (Fig. 3.25 a)) is close to that mathematically predicted, which proves the quality of the obtained mathematical expressions. The efficiency of the experimental prototype was in the range 90-94% (Fig. 3.25 b). This parameter was measured with YOKOGAWA DL850 V equipment. The maximum efficiency corresponds to the mode without the ST states and *M* equal to 1. Introduction of the ST states decreases the efficiency. Fig. 3.25 c) shows the dependence of the THD of the output voltage and the D_s cycle. It can be seen that the presence of ST states slightly deteriorates the quality of the output voltage but, because of high switching frequency, this influence is negligibly low.

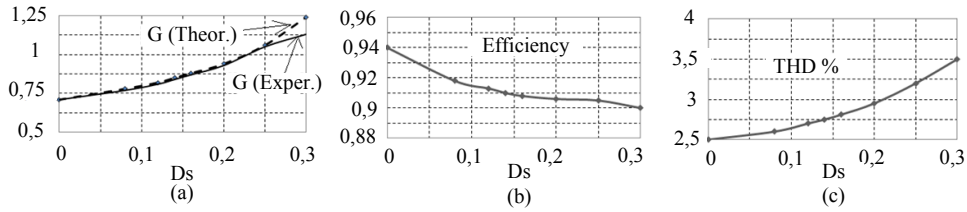


Fig. 3.25. Experimental measurements of the single-phase converter. a) Comparison of the gain factors obtained analytically (dashed line) and experimentally (solid line) versus D_s, b) Dependence of efficiency with the D_s and c) THD of the output voltage with different D_s.

The test bench for the three-phase prototype (section 2.5.2) is composed by a real PV installation. A PV installation of 18 serial panels [117] is the voltage source for the converter. Table 3.2 shows the main parameters of the PV panel used during the tests. Fig. 3.26 shows the resulting input PV curves where the different tested working points are marked. Data of the selected working points are summarized in

Table 3.3.

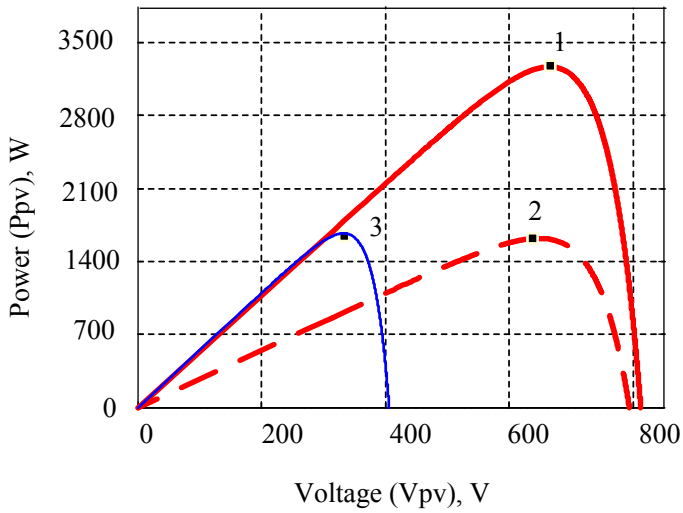


Fig. 3.26. Cases of study in the three-phase system.

Table 3.2. Main parameter from the panel datasheet.

Parameter	**Value and unit**
Nominal output power (Pmax)	185 W
Voltage at P_{MPP}	36.9 V
Current at P_{MPP}	5.02 A
Open circuit voltage (V_{oc})	45.1 V
Short circuit current (I_{sc})	5.48 A

Table 3.3. Values in each selected operation point.

Parameter	**Point 1**	**Point 2**	**Point 3**
Irradiance (W/m^2)	1000	500	1000
Vpv (V)	650	565	325
Ppv (W)	3333	1534	1666
M	≈ 1	1	0.7
% third harmonic	0	19	19
D_s	0	0	0.3

Low but equally distributed solar irradiation does not require extremely high boost (point 2 in Fig. 3.26). High boost capabilities are demanded in a partly shadowed mode where only half of the panels in the array have no irradiation (point 3). It can be seen that MPP with maximum irradiation corresponds to the buck mode (point 1).

Fig. 3.27 shows several waveforms for the first working point. Input voltage is equal to 650 V (≈ 18x36.9 V) hence no boost function is required. It is represented input current and voltage (a), capacitor voltages (b), dc-link voltage (c) and output voltage (d). It can be seen that no ripples are presented in the input current or the dc-link voltage because ST switching states are unactivated.

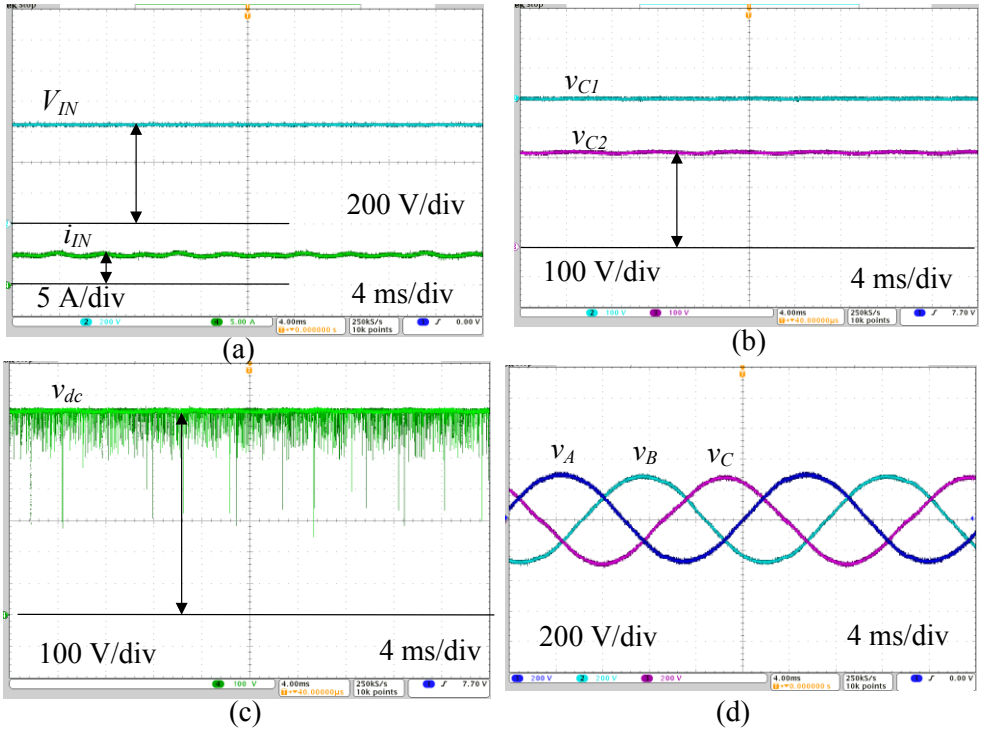


Fig. 3.27. Experimental waveforms for the first point in buck mode without third harmonic injection. a) Input current and voltage. b) Capacitor voltages. c) dc-link voltage. d) Output voltage.

Fig. 3.28 illustrates the experimental results for the second operation point. In this case the input voltage is 565 V which requires third harmonic injection without ST generation. It is represented input current and voltage (a), capacitor voltages (b), dc-link voltage (c) and output voltage (d). All of them are quite similar than in the previous case.

Fig. 3.29 represents the third operation point where input voltage is 325 V hence boost function is required. Boosted voltage is obtained from the input voltage to the capacitor

voltages thanks to the ST states, which are uniformly distributed (c). The output voltage has very good quality.

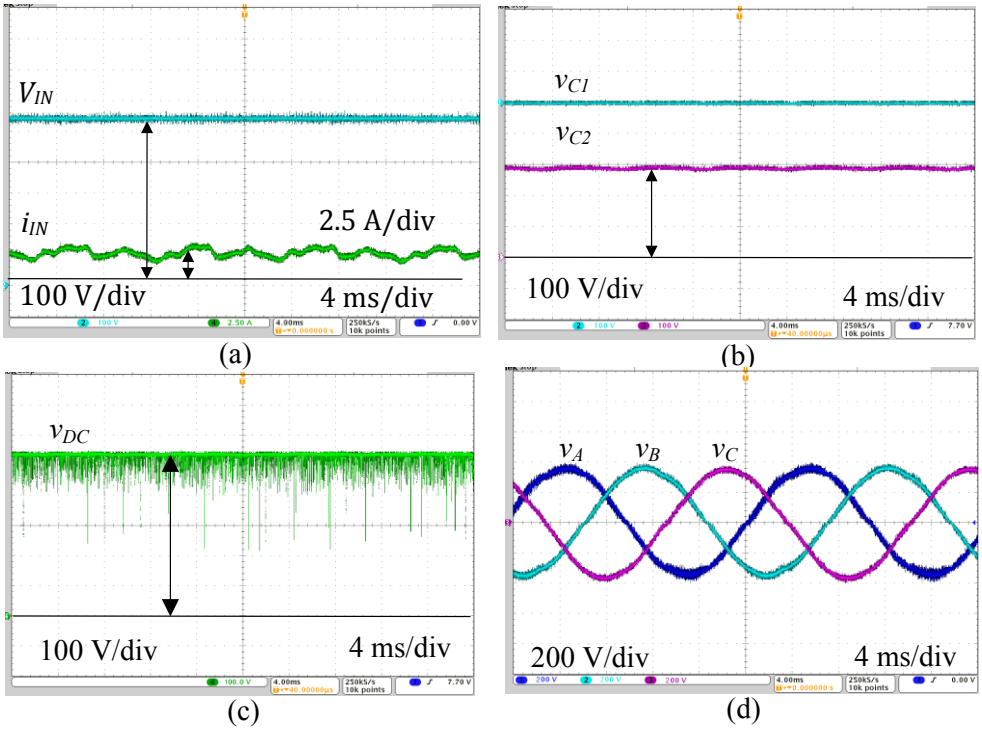


Fig. 3.28. Experimental waveforms for the second point in buck mode with third harmonic injection. a) Input current and voltage. b) Capacitor voltages. c) dc-link voltage. d) Output voltage.

Experimental results and set-up description devoted to the single-phase inverter are available in papers [**b**], [**d**] and [**e**] of the appendix. Details of the experimental tests for the three-phase case along efficiency and power losses studies are available in paper [**e**]. In this last paper, a new case with light load and several simulations are described as well.

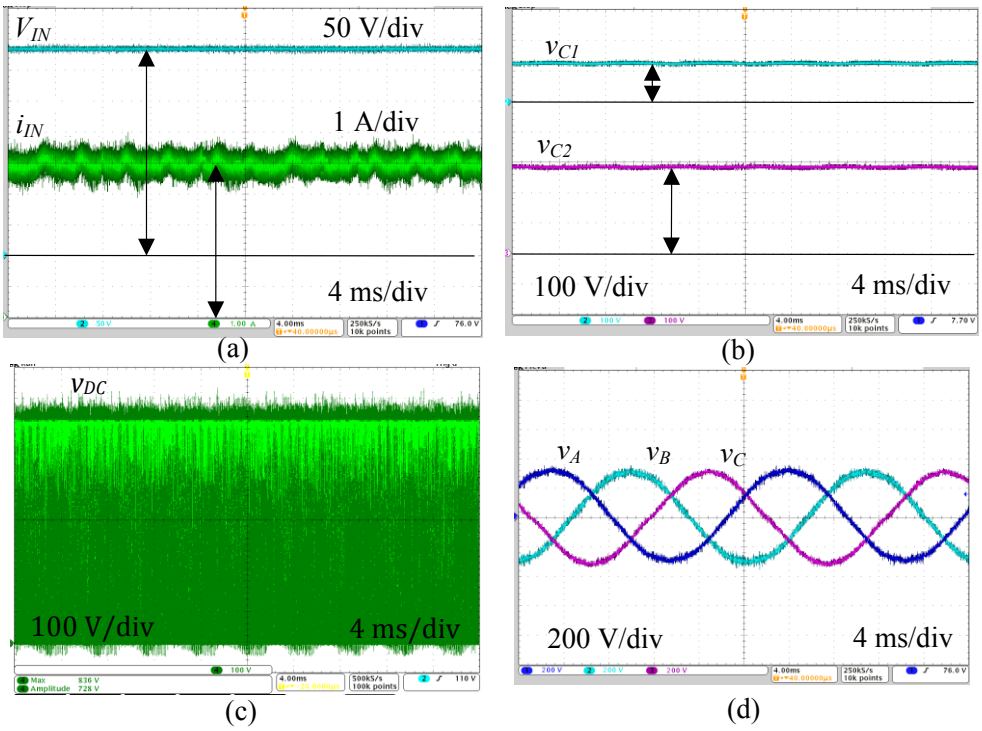


Fig. 3.29. Experimental waveforms for the third point in boost mode with third harmonic injection. a) Input current and voltage. b) Capacitor voltages. c) dc-link voltage. d) Output voltage.

Chapter 4
Operation Strategies for Performing Grid-Connected Inverter Active Functions

4.1 Introduction

High-penetration level of distributed inverters in the electrical distribution grid presents changes and possibilities in its management [118]. Those inverters mainly interact with RESs, for instance, PV panels. For long years, they just extracted the maximum power from the PV panels and injected it into the grid [2] with the reference of unitary power factor. New trends about controlling photovoltaic inverters propose to integrate to them active functions [119]. In this way, inverters will become active devices in the electrical grid; ensuring local support, quality warranties and security of supply. Some of these new demanded active functions (even some of them by regulation [120]) are: active power (P) and reactive power (Q) flow control, PCC voltage level control, active filtering capabilities [121], integration with the energy resource (MPP tracking, energy storage [6],[122]-[123] ,…) and communication compatibilities among others [7].

Controlling the power flow by inverters is one of those main issues, in both transient (e.g., during voltage sags) and steady conditions [124] (e.g., restoring the voltage level at the PCC). The extra-capacity of inverters [118] and, in the case of PV distributed plants, the limitation of active energy production, can be used as solutions for this requirement. In this way, inverters can generate or consume reactive power providing the local support and control required.

In the case of the proposed topology in this research, new approaches are required to implement such kind of active functionalities. Basically, there must be a coexistence of three elements: an operation strategy of the inverter, a dc-link voltage control method (to regulate the D_s) and special modulation techniques to embed the ST states.

For the first key element, it is possible to design an operation strategy based on traditional approaches, depending on the applications (PV inverters [125], DG, Vehicle to Grid (V2G) [126], excitation field for synchronous machines [127], Energy Storage Systems (ESS) [128], Uninterruptible Power Supply (UPS) and Active Power Filtering (APF) among others). To distinguish grid-connected PV applications, operation strategies based on *d-q* synchronous reference frame seem to be the most popular [125], [129].

In the second aspect, previous works divide the dc-link voltage control for ZSIs or qZSIs (or D_s regulation) in direct or indirect control [130], depending on whether the dc-link voltage is sensed or not respectively (see Fig. 4.1 a) and b), for the case of ZSI).

The last key element was explained in the previous chapter (3.5.2).

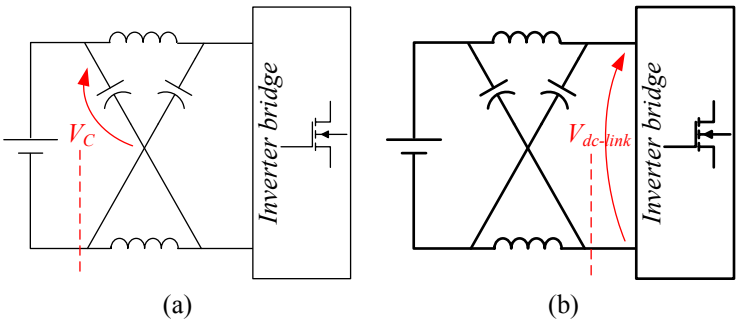


Fig. 4.1. Control methods of dc-link voltage. a) Indirect. b) Direct.

4.2 Maximum power point tracking algorithm for three-level neutral-point-clamped qZS inverter

Tracking the Maximum Power Point (MPP) of a PV array is necessary due to the high cost of solar panels and the dependence of power with irradiance and temperature [131], being an essential task of PV inverters. In this way, several MPPT algorithms have been proposed in the literature [132]. Those methods vary in complexity of implementation, sensors required, convergence speed, cost, range of effectiveness and hardware implementation among others. Three traditional MPPT algorithms are highlighted due to their capabilities: Perturb and Observe (P&O), Incremental Conductance (InC) and the method based on dP/dV or dP/dI feedback.

These traditional MPPT methods have been studied and adapted for the 3L-NPC-qZSI topology [**a**]. All of them work by using the D_s as a control variable to track the MPP

in dynamic irradiance conditions. With these methods, active power reference (P^*) can be calculated. For reactive power reference (Q^*) there are several approaches in the literature [133]. In our case, the maximum capability of the inverter (S_N, defined by the rated current of semiconductors) is considered and expressed by the equation highlighted in Fig. 4.2.

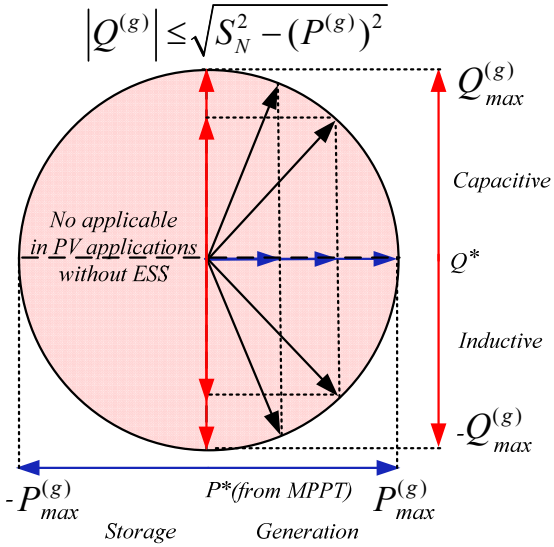


Fig. 4.2. PV inverter regulation capacity.

One way to achieve the MPP operation is to calculate the slope (dP/dV) [134]-[138] of the PV array power curve and feed it back to the converter with any control method to drive such slope to zero. The slope can be computed in different ways. In our case, a proportional-integral (PI) controller that adjusts the D_s is used to drive the slope to zero. Fig. 4.3 shows the implementation scheme of the MPPT algorithm based on dP/dV feedback for the 3L-NPC-qZSI using the D_s as a control variable.

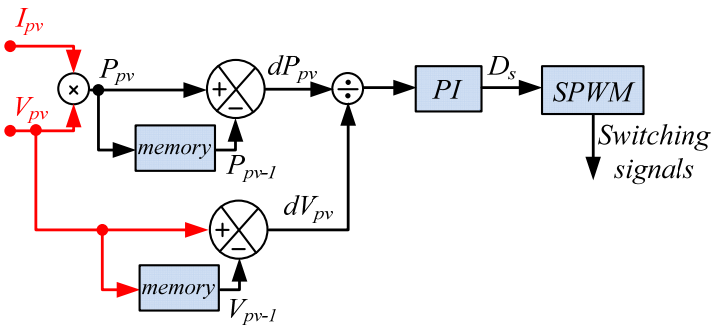


Fig. 4.3. Implementation scheme of dP/dV MPPT method.

The second proposed method is based on P&O [139]-[140]. The process of this method can be summarized in Table 4.1. The sketch of the implementation is represented in Fig. 4.4. To produce the perturbation in the voltage of the PV array, perturbations in the D_s are inserted. The perturbation is fixed and stablished in 0.005 since this value corresponds approximately to 1% of the V_{pv} (according to equation 2.4). This value has resulted in a good system dynamic response and the MPP is reached in a fast way. By means of this process the system oscillates around the MPP.

Table 4.1. Summary of MPPT algorithm based on P&O.

Perturbation	**Change in Power**	**Next Perturbation**
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

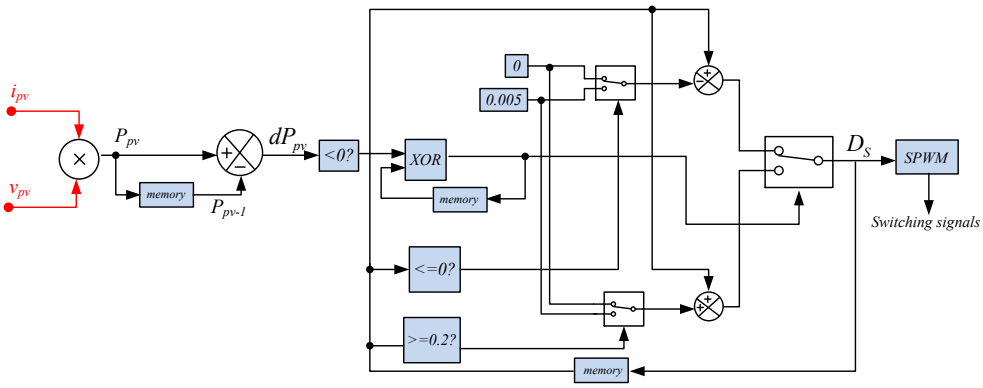


Fig. 4.4. Implementation scheme of the P&O method.

The InC method analyzes the slope of the PV array power curve. This slope is zero at the MPP, positive on the left of the MPP and negative on the right. Thus

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \cong I + V\frac{\Delta I}{\Delta V} \ , \tag{4.1}$$

and as a consequence, the incremental conductance ΔI/ΔV is equal, higher than or lower than –I/V at the MPP, on the left of the MPP and on the right of the MPP, respectively. The MPP can be tracked by comparing the instantaneous conductance (I/V) with the incremental conductance ($\Delta I/\Delta V$) as the flowchart in Fig. 4.5 shows. In our case by changing D_s, with fixed step and equal to 0.005, the PV voltage (V_{pv}) where the PV array is forced to operate is changed, trying to find the MPP ($\Delta I/\Delta V = -I/V$).

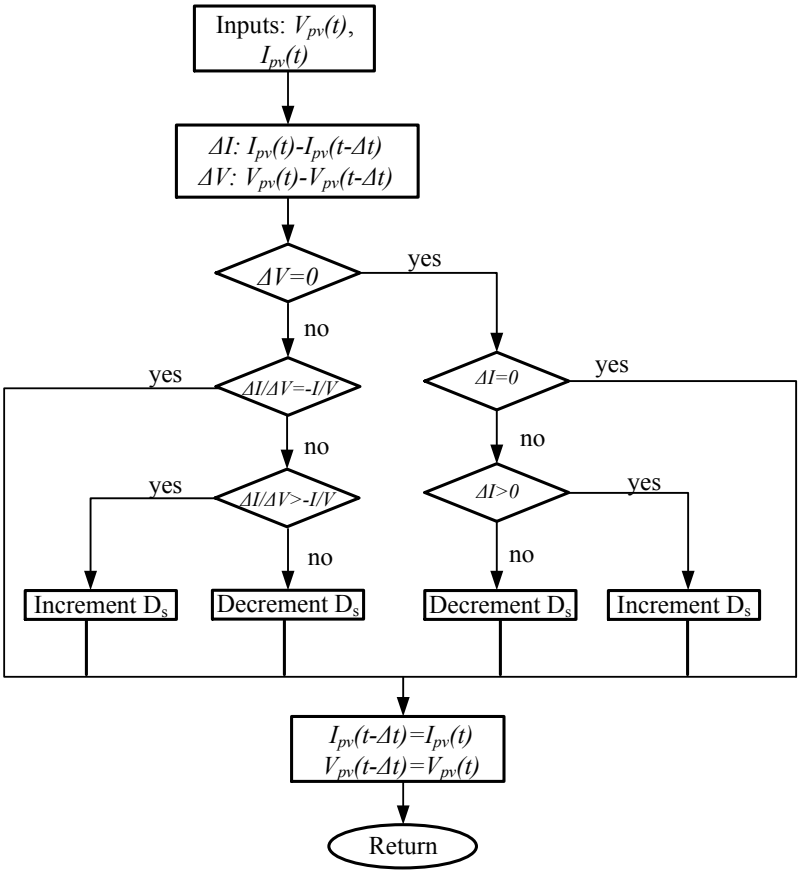


Fig. 4.5. Incremental conductance flowchart.

4.2.1 Simulation study

In order to verify the previous adapted traditional MPPT algorithms, a comprehensive simulation study is performed in SimPowerSystems of Matlab/Simulink. Parameters of the simulation are described in Table 4.2. Parameters of the PI controller for *dP*/*dV* feedback method are selecting by trial and error method. The PV array is modelled by means of model based on PV panel specifications in [141]. The case of study is based on the single-phase topology (section 2.5.2).

To analyze the transferred power to the load and the effectiveness of each MPPT method, a smooth step in the irradiance from 1000 W/m^2 to 900 W/m^2 in second eight up to sixteen was made while the temperature was maintained constant (25 ^{o}C). This action emulates the shadow phenomena. Fig. 4.6 shows the evolution of the transferred power from the PV array to the load and the evolution of the control variable (D_s) in dynamic conditions by using each MPPT algorithm.

Table 4.2. Simulation parameters.

Parameter	Description and unit	Value
V_{oc}	Open circuit voltage (V)	43.4
I_{sc}	Short circuit current (A)	4.8
I_{MPP}	Maximum power point current (A)	4.4
V_{MPP}	Maximum power point voltage (V)	34
N_s	Series connected panel	7
N_p	Parallel connected panel	1
K_p	Proportional constant of PI controller	0.001
T_i	Integral time of PI controller	0.01
P&O	Perturbation size in D_s	0.005
InC	Perturbation size in D_s	0.005

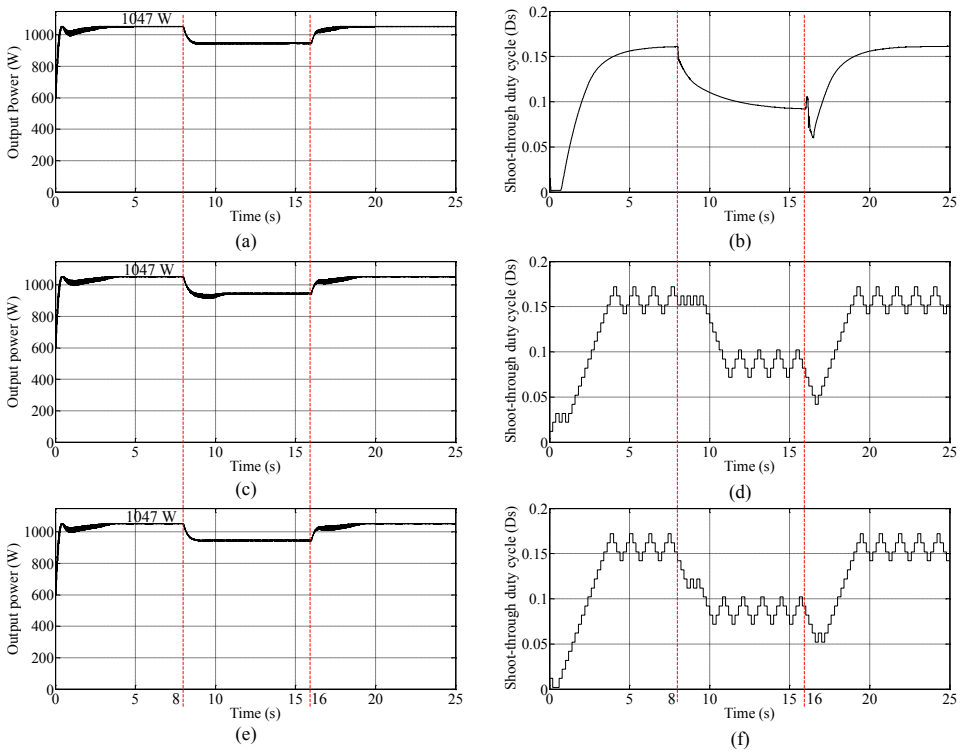


Fig. 4.6. Evolution of transferred power and D_s during a step in irradiance. a) and b) *dP*/*dV* method. c) and d) P&O method. e) and f) InC method.

As we can see in Fig. 4.6 the MPP is tracked with accuracy in each case. In paper [**a**] in appendix it is possible to see the analytical comparison, where their advantages and disadvantages are discussed. As main conclusion, method based on P&O was chosen due to its simplicity and robustness.

4.2.2 Experimental results

P&O adapted method was implemented in the single-phase prototype (section 2.5.2) and tested with a solar array. Two strings of 7 panels connected in series were connected in parallel (2x7 configuration) to obtain a proper input voltage range. The output power is transferred to a pure resistive load.

Fig. 4.7 shows the obtained results after reaching the maximum power point operation: output current (I_{OUT}), V_{OUT}, V_{PV} and input PV current (I_{PV}). Output magnitudes have a high level of quality. Measured THD_U with YOKOGAWA DL850 V equipment is 1.5 %. Input PV voltage presents a low frequency ripple at 100 Hz as commonly happens in single phase systems. Input PV current presents this low frequency ripple and also ripple at high frequencies due to the switching frequency. More details about MPP for the 3L-NPC-qZSI can be found in paper [**a**] in appendix.

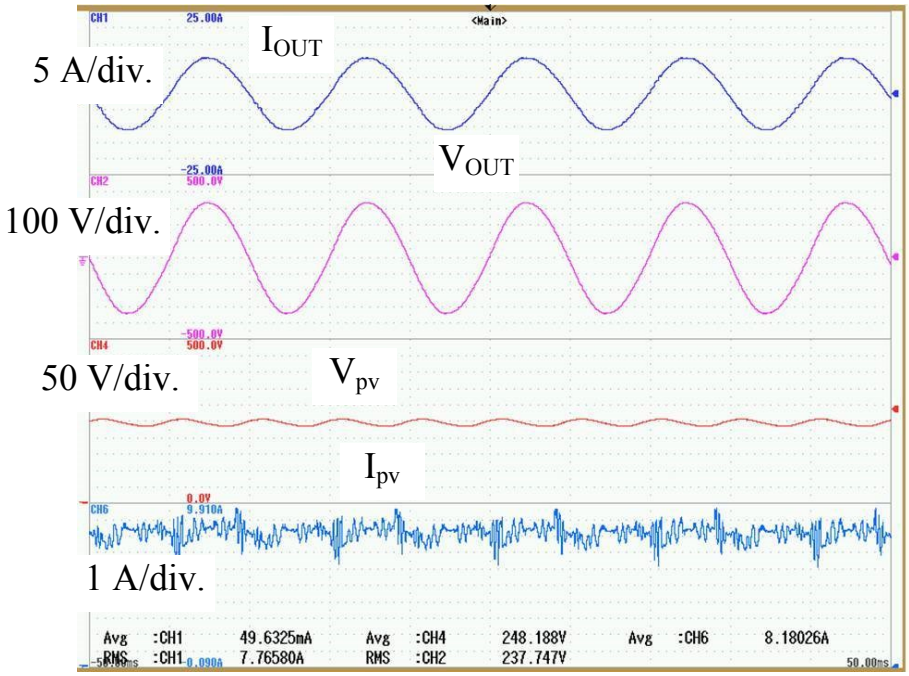


Fig. 4.7. Experimental results at the MPP operation. From top to bottom: output current, output voltage, input PV voltage and input PV current.

4.3 *P* and *Q* regulation

As aforementioned, it is possible to design the operation strategies for the new three-level NPC-qZSI both in single-phase and in three-phase configuration based on traditional approaches, depending on the target and application. In subsection 4.3.1 some well-known operation strategies to regulate *P* and *Q* in traditional inverters (section 2.2) are summarized, to subsequently explain their modifications and adaptations to be used in the new proposed topologies.

4.3.1 P and Q operation strategies for traditional inverter topologies

In a balanced three-phase system, if $v_{gen}(t)$ and $v_{pcc}(t)$ are the instantaneous generator and PCC voltages respectively, then the generated average active power ($P^{(g)}$), apparent power (S) and the generated average reactive power ($Q^{(g)}$) are given as

$$P^{(g)} = \frac{V_{pcc} V_{gen}}{X_{gen}} \sin\delta \ , \tag{4.2}$$

$$S = V_{pcc} I_{grid} = \frac{V_{pcc}}{X_{gen}} \sqrt{V_{pcc}^2 + V_{gen}^2 - 2V_{pcc} V_{gen} \cos\delta} \text{ and} \tag{4.3}$$

$$Q^{(g)} = \sqrt{S^2 - P^{(g)^2}} = \frac{V_{pcc}}{X_{gen}} (V_{gen} \cos\delta - V_{pcc}) \ . \tag{4.4}$$

where:

- $i_{grid}(t)$ is the instantaneous injected current.
- V_{pcc} is the line to neutral RMS PCC voltage.
- V_{gen} is the line to neutral RMS generator voltage.
- δ is the angle between V_{gen} and V_{pcc}.
- X_{gen} is the impedance of the generator (pure inductive is considered).

Assuming that δ is small, equations (4.2) and (4.4) can be approximated by the first term of the Taylor series as

$$P^{(g)} \approx \frac{V_{pcc} V_{gen}}{X_{gen}} \delta \quad \text{and} \tag{4.5}$$

$$Q^{(g)} \approx \frac{(V_{pcc} V_{gen} - V_{pcc}^2)}{X_{gen}} \ . \tag{4.6}$$

These equations are widely used in traditional power systems to control high power synchronous generators. The manipulated variables are

$$P^{(g)} = (V_{gen}, \delta) \quad \text{and} \tag{4.7}$$

$$Q_{gen} = (V_{gen}) \ . \tag{4.8}$$

It is also possible to make an analogy between previous equations and the equation that governs the RMS output voltage of a three-phase inverter

$$V_{inv} = M \frac{V_{dc}}{2\sqrt{2}} \ , \tag{4.9}$$

where:

- V_{inv} is the RMS fundamental component line-to-neutral inverter voltage.

In the case on the inverter, the manipulated variable is

$$V_{inv} = V_{inv}(M). \tag{4.10}$$

Combining equations from (4.7) to (4.10) we have the following relationships

$$P^{(g)} = (M, \delta) \ \text{and} \tag{4.11}$$

$$Q^{(g)} = (M) \ , \tag{4.12}$$

where δ is in this case the angle between V_{inv} and V_{pcc}. Therefore, manipulating δ and M it is possible to regulate $P^{(g)}$ and $Q^{(g)}$ in a grid-connected inverter.

Fig. 4.8 depicts a block diagram of implementation. Two PI controllers are dedicated to track P^* and Q^* by manipulating δ and M of the inverter reference signal. Feed-forward loop for grid voltage phase (θ_{grid}) is used to make easier the synchronization process and to avoid undesired transients. In the same figure, red line represents the measured signals. Modulation technique based on SVPWM is used to generate the switching signals.

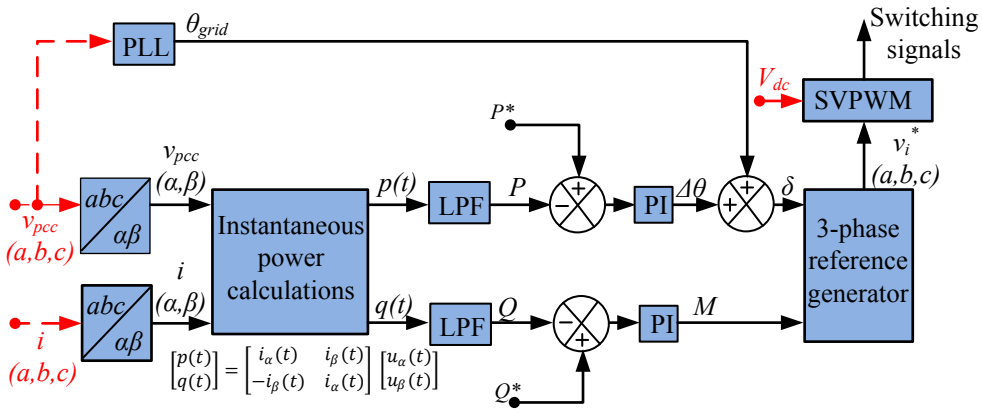


Fig. 4.8. Operation strategy based on δ and M as manipulated variables.

Another well-known approach for traditional inverters is based in a *d-q* synchronous reference frame. The inverter can be modelled as an ideal sinusoidal voltage source with the impedance of the output filter. From this equivalent circuit it is possible to obtain the state-space model. In order to control its injected P and Q, Park Transformation [142] as well as a synchronous reference frame with the same frequency than the grid frequency [143] are required. In addition, if the *d* axis is aligned with the grid voltage vector, *q* component is zero. Operating in this way variables in *abc* domain are transformed to *d-q* domain.

In this case, active and reactive powers are expressed as [144]

$$p = v_d i_d \text{ and} \tag{4.13}$$

$$q = -v_d i_q \ . \tag{4.14}$$

Therefore if the space grid voltage vector is known, active and reactive power can be achieved through current components at *d-q* frame.

Fig. 4.9 shows the control scheme in both axis *d* and *q*. The main advantages of this approach in comparison with the previous one are that in this case, it is possible to get decoupled power control loops, as well as it is possible to design the controllers in continuous time.

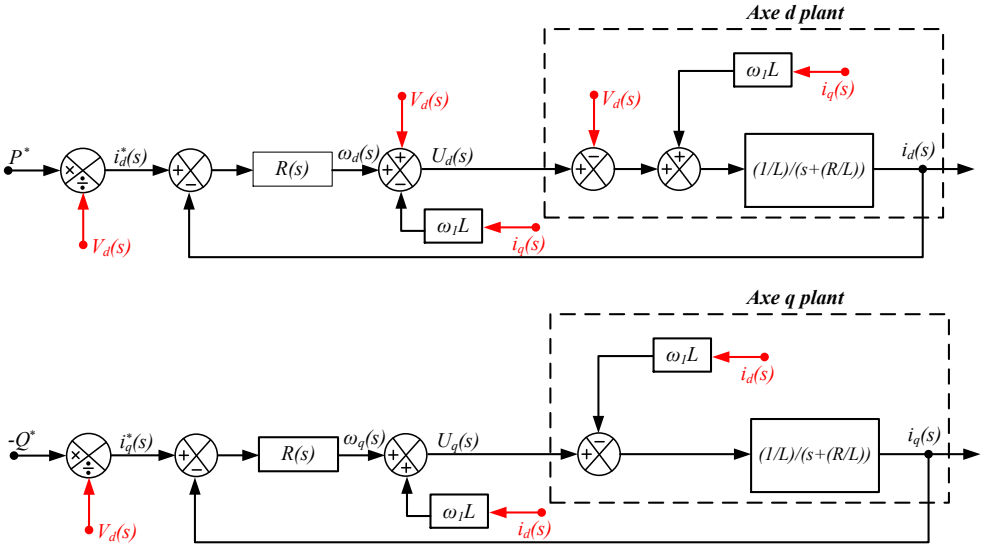


Fig. 4.9. *d-q* axes control sketch of the grid-connected inverter.

In paper [**h**] in the appendix a comparison between both aforementioned operation strategies is explained by simulation. As the strategy based on *d-q* reference frame presents advantages, it is validated experimentally as follows.

The experimental setup used to validate the strategy is shown schematically in Fig. 4.10. Fig. 4.11 represents the power stage composed by one Danfoss FC302 2.2 kW inverter, *LCL* output filter, bidirectional dc power supply and the grid connection by an autotransformer. The measurement stage is done by current and voltage LEM sensors (red line in the same figure). The inverter is equipped with a driver board. The control platform is based on dSPACE 1106 system hence the explained strategy is implemented in Matlab/Simulink. Table 4.3 summarizes the main parameters of the electrical setup and control system parameters. (These experimental tests were carried out at Aalborg University).

Fig. 4.12 shows the responses of the system when different steps are applied both in P^* (Fig. 4.12 a)) and in Q^* (Fig. 4.12 b)). In the left figure, P^* is 100 W, 500 W, 900 W and 1500 W in seconds 0, 10, 20 and 30 respectively while Q^* is maintained in 0 kVAr. In the right figure, Q^* changes from 100 kVAr, to 600 kVAr, to 1250 kVAr and to 600 kVAr in seconds 0, 10, 20 and 30 respectively while P^* is equal to zero. As it is possible to check, the system tracks the references with accuracy in both cases.

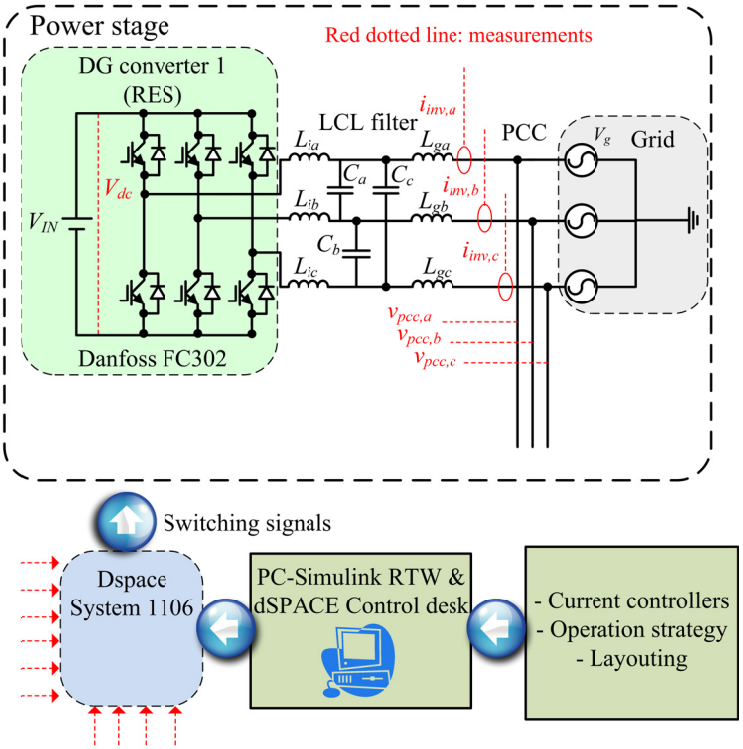


Fig. 4.10. Schematic of experimental power stage and setup configuration.

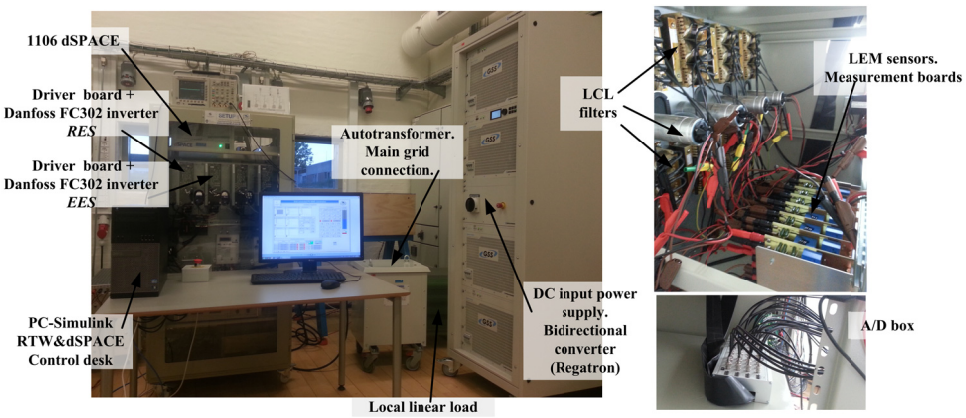


Fig. 4.11. Experimental configuration for testing the operation strategy in a traditional inverter.

Table 4.3. Electrical setup and control system parameters.

Parameter	**Description and unit**	**Value**
V_{dc} (V)	dc voltage (V)	650
f (Hz)	Frequency	50
V_{pcc} (V)	RMS voltage at the PCC	230
f_s (kHz)	Switching frequency	10
Inverter	Danfoss converter FC302	
$L_{i,a}$(mH)	Filter inductance	1.8
C_i (μF)	Filter capacitance (Δ connection)	9
$L_{g,a}$ (mH)	Filter inductance. Grid side	1.8
Grid	Trafo Type 3LT-23 Dyn 11	-
$K_{p,P}$	Active power proportional term	$6 * 10^{-4}$
$K_{i,P}$	Active power integral term	$4 * 10^{-4}$
$K_{p,Q}$	Reactive power proportional term	$3 * 10^{-4}$
$K_{i,Q}$	Reactive power integral term	$3 * 10^{-4}$

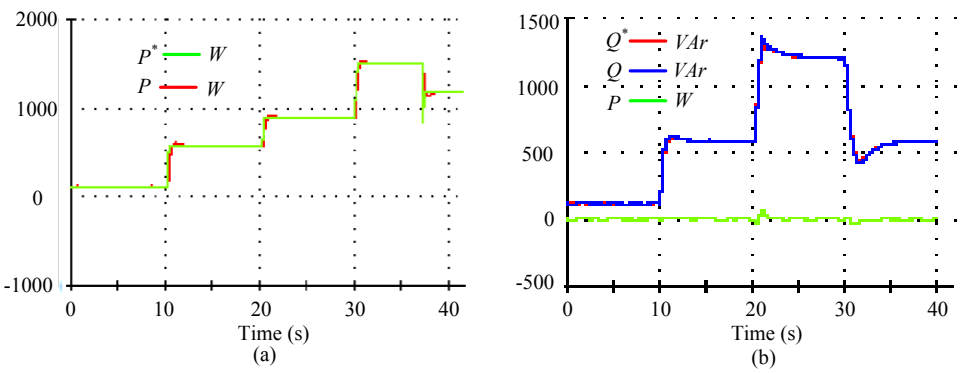


Fig. 4.12. Experimental results with control strategy based on *d-q* reference frame. a) Active power evolution. b) Reactive power evolution.

4.3.2 Proposed operation strategies for P and Q regulation in a three-level neutral-point-clamped qZS inverter

This section is dedicated to explain different control strategies proposed for both single-phase and three-phase versions of the inverter under study, to regulate P and Q in grid-connected mode. Different approaches to improve the dynamic behaviour have been taken into account. The section is divided into two subsections; strategies for single-phase in the first part and strategies for three-phase in the second part.

Single-phase version

The goal of the first proposed control strategy is to inject power into the grid with unitary power factor, that is, injecting a sinusoidal current in phase with the voltage at the PCC. It will be achieved by means of controlling the reference voltage signal inverter. For a simpler approach it is assumed an output L filter. Fig. 4.13 represents the case of study.

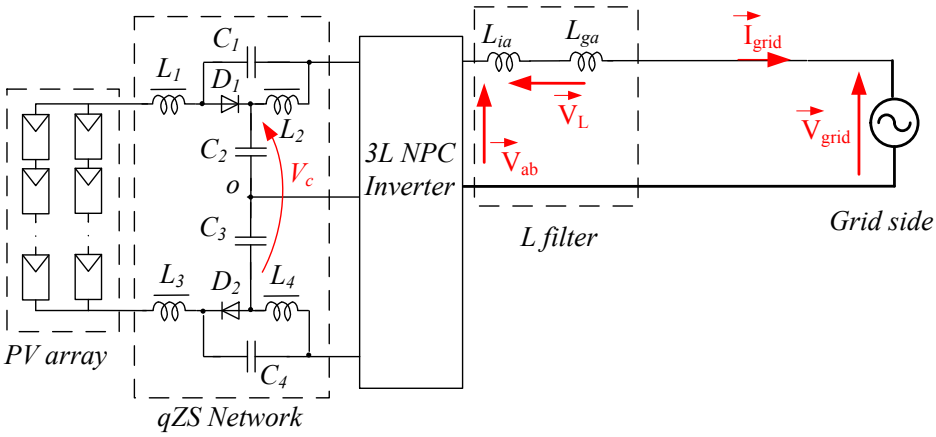


Fig. 4.13. Power stage of the grid-connected PV system based on a single-phase 3L-NPC qZSI.

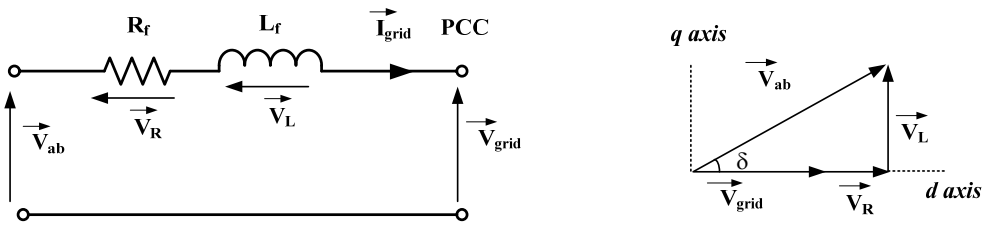
First of all, a power balance between dc and ac sides to obtain the injected RMS reference current (I^*_{grid}) into the grid is necessary to perform. This is carried out by means of

$$I_{pv}V^*_{pv} = I^*_{grid}V_{grid}\,, \tag{4.15}$$

Where V^*_{pv} is given from the MPPT algorithm. We also define the variables in Table 4.4, for a better understanding. To realize a more precise approach, we will take into account the resistance of the filter inductance (R_f). L_f includes the impedances of transformer and grid for simplification. Variables are represented in the equivalent scheme of the output filter (Fig. 4.14 a)) and its vector diagram in a d-q frame (Fig. 4.14 b)). The d component of this frame is synchronized with the voltage at the PCC.

Table 4.4. Variables involved in the first control strategy for single-phase topology.

Variable	Description and unit
$\vec{V}^*_{ab}$	Reference output voltage vector of the fundamental component in terminals of the 3L-NPC-qZSI. Voltage between branches.
$\vec{V}^*_L$	Reference voltage drop vector in the filter inductance.
$\vec{V}^*_R$	Reference voltage drop vector in the resistance of the filter inductance.
$\vec{I}^*_{grid}$	Reference injected current vector to the grid.
$\vec{V}_{grid}$	Voltage grid vector. Voltage at the PCC.



(a) (b)

Fig. 4.14. a) PCC equivalent scheme. b) Vector diagram.

According to the vector diagram of Fig. 4.14 b) one has

$$\vec{V}^*_{ab} = \vec{V}_{grid} + \vec{V}^*_R + \vec{V}^*_L \,, \tag{4.16}$$

that could be expressed in a *d-q* frame as

$$\vec{V}^*_{ab} = V_{grid}\vec{u}_d + V^*_R\vec{u}_d + V^*_L\vec{u}_q \tag{4.17}$$

where $\vec{u}_d$ and $\vec{u}_q$ are unitary vectors in the *d* and *q* directions.

The RMS value of $\vec{V}^*_{ab}$ can be calculated as

$$V^*_{ab} = \sqrt{(V_{grid} + V^*_R)^2 + (V^*_L)^2} \tag{4.18}$$

where V^*_R and V^*_L are RMS values of the reference vectors $\vec{V}^*_R$ and $\vec{V}^*_L$.

At the same time, V_{ab}^{*} is related to reference signal M and the dc-link voltage as

$$M = \frac{\sqrt{2}\,V_{ab}^{*}}{V_{dc}}, \tag{4.19}$$

which can be expressed as

$$M = \sqrt{2}\,\frac{\sqrt{(V_{grid} + I_{grid}^{*}R)^2 + (\omega L_f I_{grid}^{*})^2}}{V_{dc}}. \tag{4.20}$$

In this way, M has been calculated to obtain the desired amplitude of $\vec{V}_{ab}^{*}$ according to the vectors diagram of Fig. 4.14 b).

To calculate δ, a unitary vector ($\vec{u}_{ab}$) in the direction of $\vec{V}_{ab}^{*}$ is calculated as follows

$$\vec{u}_{ab} = \frac{(V_{grid} + I_{grid}^{*}R)\cdot\vec{u}_d + (\omega L_f I_{grid}^{*})\cdot\vec{u}_q}{\sqrt{(V_{grid} + I_{grid}^{*}R)^2 + (\omega L_f I_{grid}^{*})^2}}. \tag{4.21}$$

Thus, the reference output voltage vector ($\vec{V}_{ab}^{*}$) can be generated

$$\vec{V}_{ab}^{*} = \frac{V_{dc}}{\sqrt{2}} M\,\vec{u}_{ab}. \tag{4.22}$$

Fig. 4.15 represents some simulated waveforms related to the proposed strategy in the single-phase case. Fig. 4.15 a) shows the input voltage and current when the MPP is achieved and b) represents the dc-link voltage, where ST states are observed. Finally, in c) and d) the output voltage between branches before filtering and the grid voltage with the injected current are represented respectively. The main goal of this study was to check the capability of this converter when it is working in grid-connected mode. More details about this study are available in paper [**i**].

As aforementioned technique just allows the control of P, new control schemes for this application were developed and are explained as follows.

The original *d-q* transformation from *abc* coordinates (time varying signals) can only be used in three-phase systems [145] and it has been widely used in active power filter and reactive power compensator applications because the fundamental frequency components are mapped to dc values. The linear transformation from *abc* time varying signals to synchronous reference *d-q* components is given by [146]

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin\omega t & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ \cos\omega t & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \tag{4.23}$$

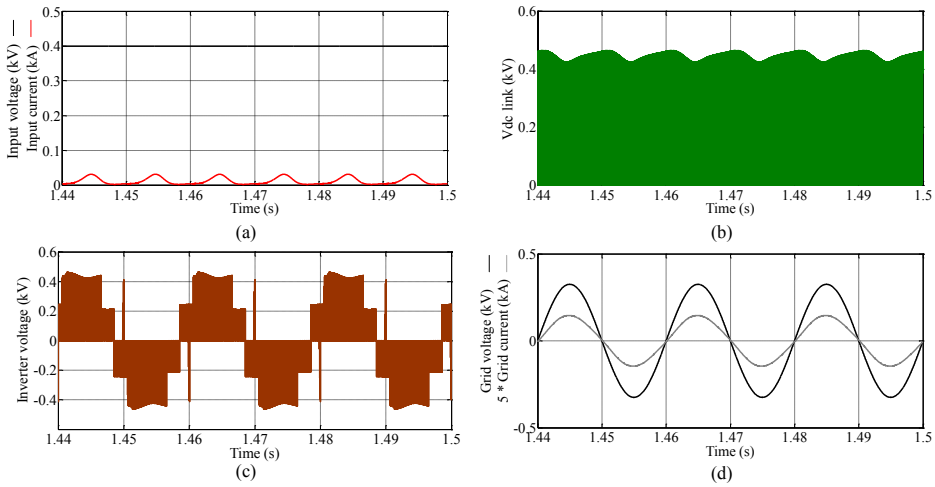


Fig. 4.15. Simulation of main waveforms. a) Input current and voltage. b) dc-link voltage. c) Output voltage before filtering. d) Output current and grid voltage.

The three-phase *abc* vector (currents or voltages) can also be transformed to a rotating *d-q* components if they are previously transformed by using an orthogonal *α-β* stationary frame [147] as

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{\sqrt{2}}{3}\begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \text{and} \tag{4.24}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{4.25}$$

Expression (4.24) comes from rotating the *α-β* stationary frame at the fundamental frequency, hence two orthogonal components are required to obtain the resulting *d* and *q* values. It is the main problem for using this theory in single phase circuits where just one phase signal (current or voltage) is available.

Different approaches have been developed to obtain the necessary orthogonal component and, in this way, *d-q* theory will be applied in single phase studies. [148] proposes the orthogonal imaginary circuit concept with the main idea of obtaining two variables, the real one (voltage or current) and an imaginary one, with equal characteristics but shifted 1/4 of period of the real one.

From the practical point of view, if we measure the real signal to be transformed to the *d-q* rotating frame, just using a time delay method (storing the value) we can obtain the

imaginary component and in this way, the measured signal is the α component and the delayed signal is the β component. This fact is illustrated in Fig. 4.16 a).

Mathematical foundations for the case where the real signal is a sine are as follows (example for voltage signal):

$$\begin{aligned} v_r &= v_\alpha = V\sin(\omega t+\varphi) \\ v_i &= v_\beta = V\sin(\omega t+\varphi-\pi/2) = -V\cos(\omega t+\varphi). \end{aligned} \tag{4.26}$$

To obtain the dc values in a *d-q* rotating frame from ac signals (Fig. 4.16 b)) it is necessary to use the linear transformations (4.24). If the real signal is considered as cosine, the linear transformation would be different [149] (replacing sin (ωt) with cos(ωt) and cos (ωt) with -sin(ωt)).

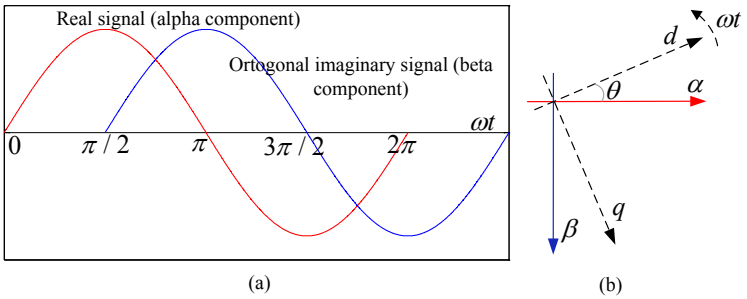


Fig. 4.16. a) Real and imaginary signals. b) α-β to rotating *d-q* reference frame transformation.

Equations (4.26) are transformed by means of linear transformation (4.25) and we have

$$\begin{aligned} v_d &= V\sin(\omega t+\varphi)\sin(\omega t) - V\sin(\omega t+\varphi-\pi/2)\cos(\omega t) = \\ &= V\cos(\varphi) \\ v_q &= V\sin(\omega t+\varphi)\cos(\omega t) + V\sin(\omega t+\varphi-\pi/2)\sin(\omega t) = \\ &= V\sin(\varphi). \end{aligned} \tag{4.27}$$

The above equations compose the dc components of the original ac signals at the fundamental frequency in the synchronous *d-q* frame. Finally, the inverse linear transformation from *d-q* signals to α-β is given as

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \sin\omega t & \cos\omega t \\ \cos\omega t & -\sin\omega t \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix}. \tag{4.28}$$

Once these previous mathematical bases are explained, to develop the control schemes in this rotating frame for the single phase case is possible as follows.

For the first approach (Fig. 4.17 a)), the control of active and reactive power is carried out by two integral regulators, which operate in a coupled way. Control action derived

from the q current component error (I^*_q -I_q) acts over the d and q component of the inverter reference voltage (V^*_d and V^*_q). It means that this integral controller adjusts the amplitude of the reference signal. Control action derived from the d current component error (I^*_d-I_d) acts just over the q component V^*_q, adjusting the phase of the inverter reference voltage. This reasoning is derived from the well-known electrical relationships (between P-δ and Q-V). In addition, feedforward loops from the grid voltage are included to smooth the connection of the inverter to the grid, which avoids undesirable transients. Finally, as the d-q frame has the same frequency as the grid frequency, and the d axis is aligned with the grid voltage vector, the q component of the grid voltage will be zero as in the previous strategy explained.

When V^*_d and V^*_q are determined, the minimum value of the required dc-link voltage can be calculated. This reference value (V^*_c) is compared with the measured dc-Link voltage (V_c) to activate or not to activate the reference value of D_s (D^*_s), depending on whether the boosting voltage is needed or not, respectively. D_s is adjusted by the third integral controller. Finally, the scaled reference signal ($v^*_{control}$) is the input for the SPWM block as

$$v^*_{control} = \frac{(1 - D^*_S)\, v^*_{ab}}{V_c}. \tag{4.29}$$

Fig. 4.17 b) shows a variant of the previous operation strategy by decoupling the active and reactive power control loops. In this proposal, control actions from (I^*_d-I_d) and from (I^*_q -I_q) are added to the $V_{d,grid}$ and $V_{q,grid}$ feedforward loops respectively, to generate the inverter reference signal.
This approach is based on the equations (4.13) and (4.14). The dc-link voltage control is exactly the same as in the previous case.

Fig. 4.17 c) depicts a modification of the control strategy for the dc-link voltage control. In this case, this control loop is independent of the power controllers, and the dc-link voltage reference is given by a predefined value.

To validate and compare the three different control strategies described, a comprehensive simulation study was performed based on the parameter of the single-phase prototype. The values for the integral controllers (see Table 4.5) were obtained using the Ziegler-Nichols method based on the response curve [150] and then improved by trial and error in the simulations.

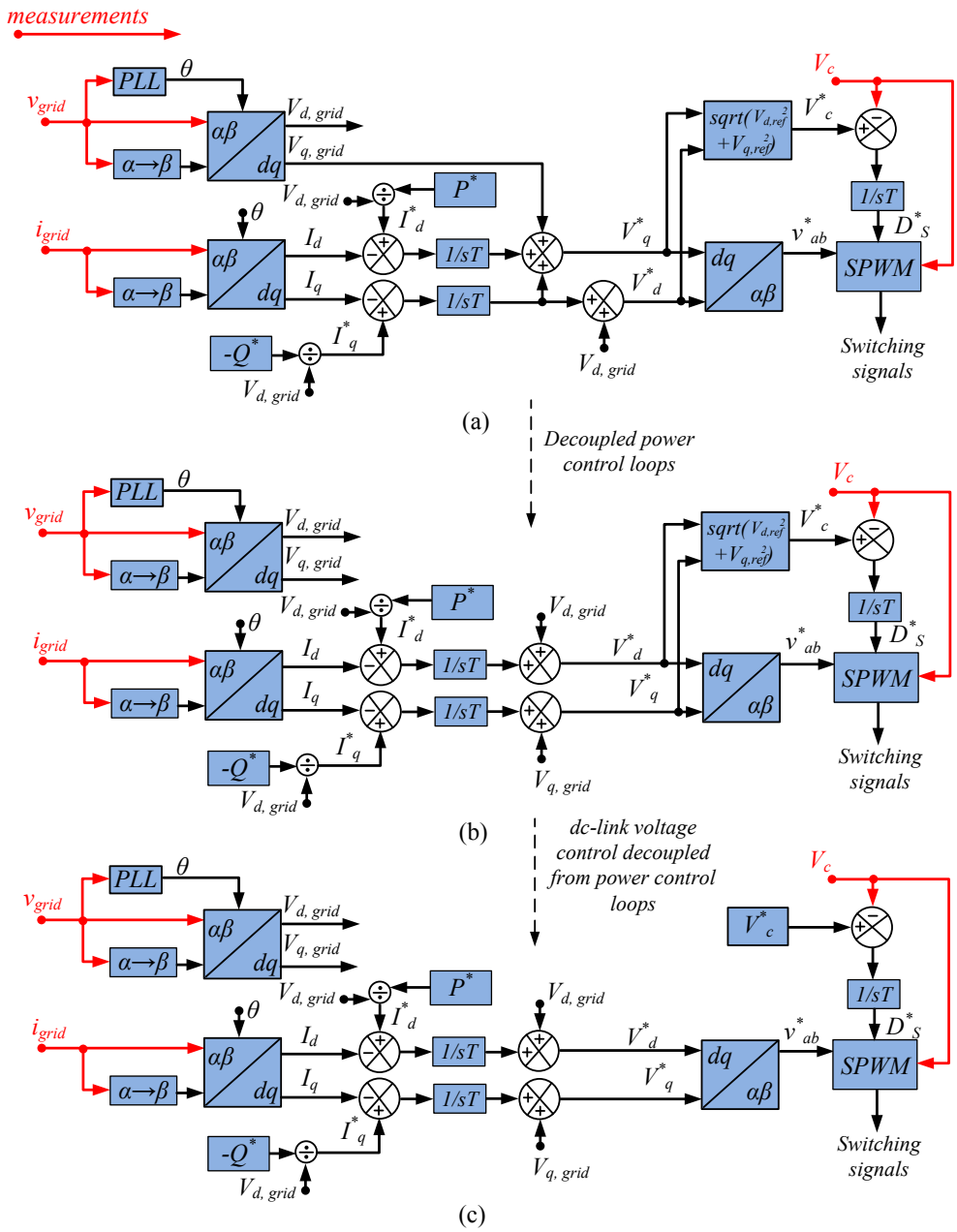


Fig. 4.17. Proposed control schemes. a) Coupled power control loops and coupled dc-link voltage control. b) Decoupled power control loops. c) Decoupled dc-link voltage control.

Table 4.5. Values for the simulation study.

Type	Parameter and unit	Description	Value
Electrical values	**V_{in} (V)**	Input voltage	365
	V_{grid} (V)	Grid RMS voltage	230
Power controllers (scheme a)	**$K_{i,P}$ (s)**	Time constant for I_d	0.05
	$K_{i,Q}$ (s)	Time constant for I_q	0.05
	$K_{i,c}$ (s)	Time constant for V_c	0.08
Power controllers (scheme b)	**$K_{i,P}$ (s)**	Time constant for I_d	0.05
	$K_{i,c}$ (s)	Time constant for I_q	0.05
	$K_{i,c}$ (s)	Time constant for V_c	0.08
Power controllers (scheme c)	**$K_{i,P}$ (s)**	Time constant for I_d	0.05
	$K_{i,Q}$ (s)	Time constant for I_q	0.05
	$K_{i,c}$ (s)	Time constant for V_c	0.065
Simulation parameters	**f_{sw} (kHz)**	Switching frequency	50
	T_s (µs)	Simulation step	0.25

As the main goal of this study is to analyze the system responses in dynamic conditions, different events are programmed. From the off-grid situation, the inverter is connected to the grid at second 0.2. Then, steps in I^*_d and I^*_q are implemented at seconds 0.5 and 1.2 respectively, in order to inject active and reactive power (2 A). Finally, the input voltage is suddenly reduced with a step as well, from 365 V to 295 V, because the boundary between the buck and the boost working mode is around 325 V (peak value of the grid voltage). With all these events it is possible to analyze all the control loops based on integral controllers.

Different responses under described conditions are depicted in Fig. 4.18 a), b) and c). From top to bottom, the evolution of the grid injected currents (I_d and I_q components) for each control strategy are revealed. The transients obtained after the step in V_{IN} are derived from the coupling between power control loops and dc-link control loop. Once the dc-link becomes stable (see Fig. 4.19), the injected power is stable as well.

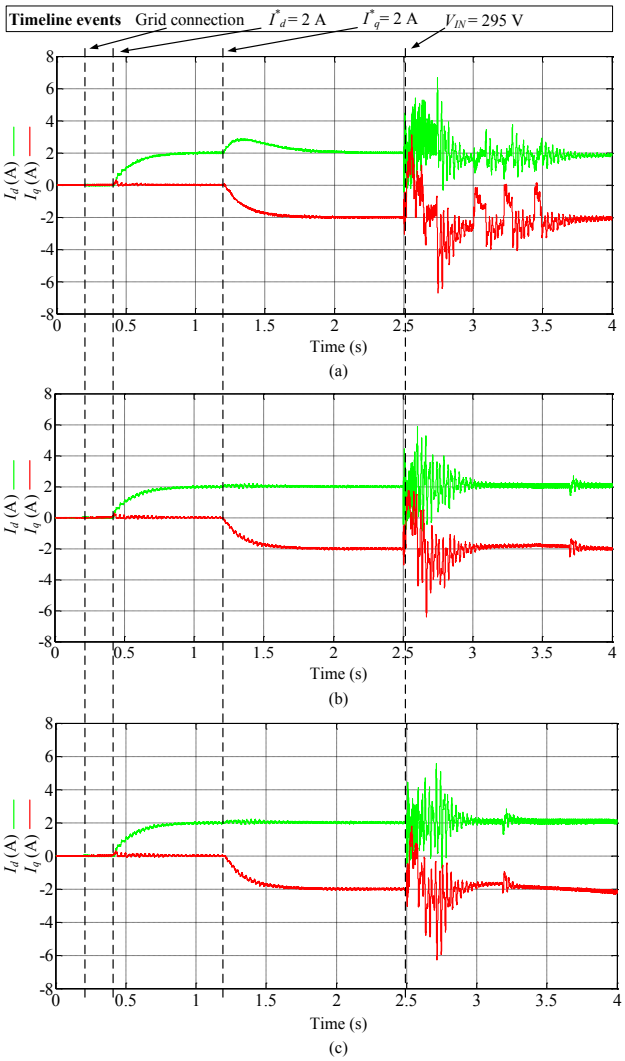


Fig. 4.18. Responses of the system under programmed conditions: a) First control scheme. b) Second control scheme. c) Third control scheme.

Fig. 4.19 shows the input voltage and the capacitor voltage in the case of the control strategy of Fig. 4.17 b) that is selected as the most appropriated strategy. When the input voltage step is applied, the converter changes from the buck to the boost mode and, in this last situation, the capacitor voltage acquires the minimum value required to assure the desired active and reactive power (Fig. 4.19 a)). Evolution of the D_s is presented in b). Figures c) and d) show the output voltage signals before filtering when D_s is zero and maximum, respectively.

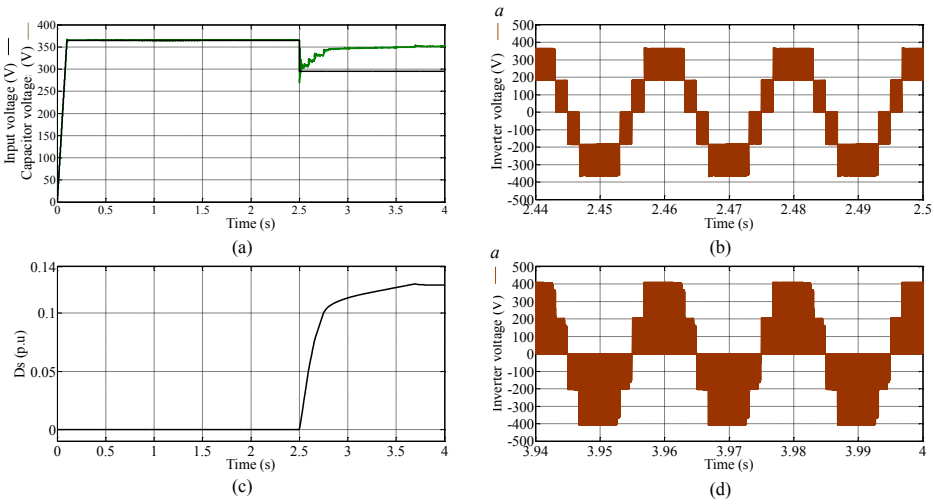


Fig. 4.19. Different magnitudes obtained with the second control scheme: a) input voltage and capacitor voltage. b) Output voltage without ST. c) D_s evolution. d) Output voltage before filtering with ST.

A detailed comparison and discussion according to different criteria such as rise time, overshoot, settling time and steady state error for each new proposed control strategy is available in papers [**j**] and [**k**], in order to justify why the second strategy is considered to be the most suitable one.

Three-phase version

The case of study regarding the three-phase 3L-NPC-qZSI in grid-connected application is represented in Fig. 4.20.

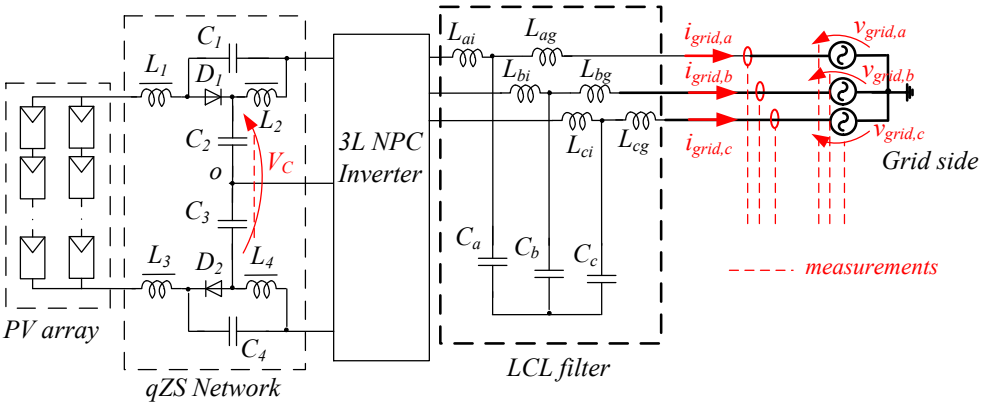


Fig. 4.20. Case of study. Schematic circuit of a grid-connected three-phase 3L-NPC-qZSI in PV application.

In the same way that the control scheme designed for single-phase case (Fig. 4.17 b)), P and Q can be controlled by using the d-q theory [125]-[129] to generate the reference signals of the manipulated variables. The main difference with the single-phase approach is that the imaginary circuit theory is not required since two components in α-β domain are available. The same requirements for the d-q frame alignment are considered as previously for the single-phase control scheme.

In grid-connected PV applications, P^* is usually given by a MPPT. On the other hand, Q^* is limited by the rated current of the semiconductors according to the highlighted equation in Fig. 4.2. In this case, two PI controllers are involved to track P^* and Q^* by acting over the manipulated variables (V^*_d and V^*_q, respectively) to produce the desired voltage signals (using back Clarke and Park transformations). Finally, a $V_{d,grid}$ feedforward loop is added again to make easier the synchronization process. Some studies report a PQ decoupling control [129] but this approach was neglected for the reasons that will be explained further.

Full operation strategy can be followed on the block diagram of Fig. 4.21.

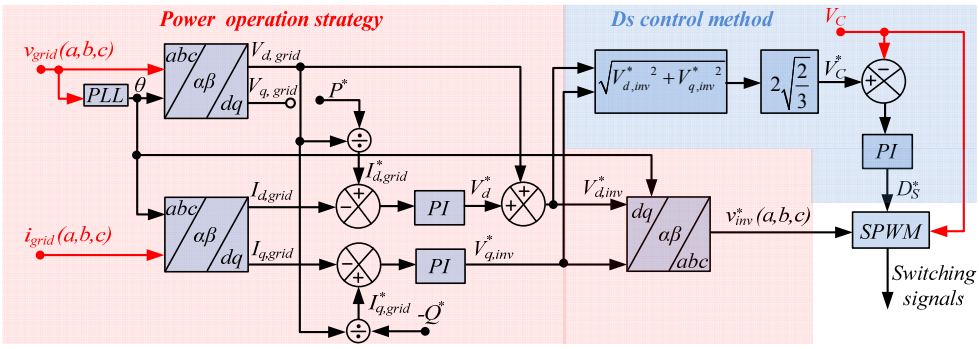


Fig. 4.21. Power operation strategy and the proposed ST control method for the three-phase case.

Once the desired voltage signals to control the power are obtained, it is easy to determine the minimum value of the dc-link voltage required as in the single-phase approach. From direct and quadrature inverter reference voltages derived from the power control loops, V^*_c can be composed with the procedure shown in Fig. 4.21. Finally, a third PI controller is intended for manipulating D^*_s, which assures the required dc-link voltage by boosting (if necessary) the input voltage.

To tune the three PI controllers, an empirical method by observing the stability of the system responses was used. Both power closed control loops were adjusted to obtain fast responses of the manipulated variables (V^*_d and V^*_q) without errors in the steady state in regard to the references powers.

The PI controller dedicated to the dc-link voltage control by acting on the D_s (manipulated variable as well) is tuned according to the next reasoning. If D_s varies, the peak

dc-link voltage also changes and would become uncontrollable [130]. In addition, this effect is transferred into the output ac side, which distorts the output voltage and increases the voltage stress across the semiconductors. Finally, changes in D_s also have influence on the output power. Hence, power controllers are also affected. If the response times of power controllers and the dc-link voltage controller are similar, the interaction between them is really significant and the system responses become unstable. Due to the aforementioned reasons, the tuning procedure of PI controllers is exhibited as a critical task.

To validate the three-phase control scheme presented, a simulation study based on the three-phase converter was performed with the main parameters in Table 4.6.

Table 4.6. Main parameters for the simulation study.

Type	Parameter and unit	Description	Value
Electrical values	$\mathbf{V_{in}}$ **(V)**	Input voltage	500-771
	$\mathbf{V_{grid}}$ **(V)**	Grid RMS voltage	230
$\mathbf{K_P}$	$\mathbf{I_d}$	constant for I_d	$1{\cdot}10^{-4}$
	$\mathbf{I_q}$	constant for I_q	$1{\cdot}10^{-4}$
	$\mathbf{D_s}$	constant for V_C	$1{\cdot}10^{-5}$
$\mathbf{t_I}$	$\mathbf{I_d}$	Time constant for I_d	$5{\cdot}10^{-4}$
	$\mathbf{I_q}$	Time constant for I_q	$5{\cdot}10^{-4}$
	$\mathbf{D_s}$	Time constant for V_C	0.5
Simulation parameters	$\mathbf{f_{sw}}$ **(kHz)**	Switching frequency	100
	$\mathbf{T_s}$ **(µs)**	Simulation step	0.2

In Fig. 4.22 it is possible to see the main waveforms when the input voltage is low and hence the shoot-through control loop is acting (inverter works in boost mode). Active power reference is changed to 1.5, to 3 and to 5 kW in seconds 0.4, 0.6 and 0.8 respectively and reactive power reference to 1 kVAr in second 1.

In Fig. 4.22 a) it can be observed that the references of P and Q are tracked properly and there is no influence between both control loops. Slight distortion in the voltage shape is observed in b). It is due to the shoot-through insertion. Fig. 4.22 c) depicts the waveforms of input side, where it is possible to observe that input current is in contin-

uous mode and V_c is boosted in comparison with V_{in}. Finally, in Fig. 4.22 d) the inverter voltages are showed with presence of shoot-through states.

Fig. 4.23 represents the evolution of D_s during all the simulation time.

One of the most significant advantages of inverter based on impedance-source networks is the wide input operation range. Fast changes in input voltages are really common in PV applications due to fast changes in the irradiance conditions and, in this sense, next test is presented. Here P and Q responses during a V_{in} step are analyzed. This voltage changes from 770 V to 500 V in second 1.2 and the power responses are depicted in Fig. 4.24. It is possible to verify that in less than 100 milliseconds (5 fundamental periods) the system tracks the references again thanks to the regulation of shoot-through states (inverter changes suddenly from buck to boost mode).

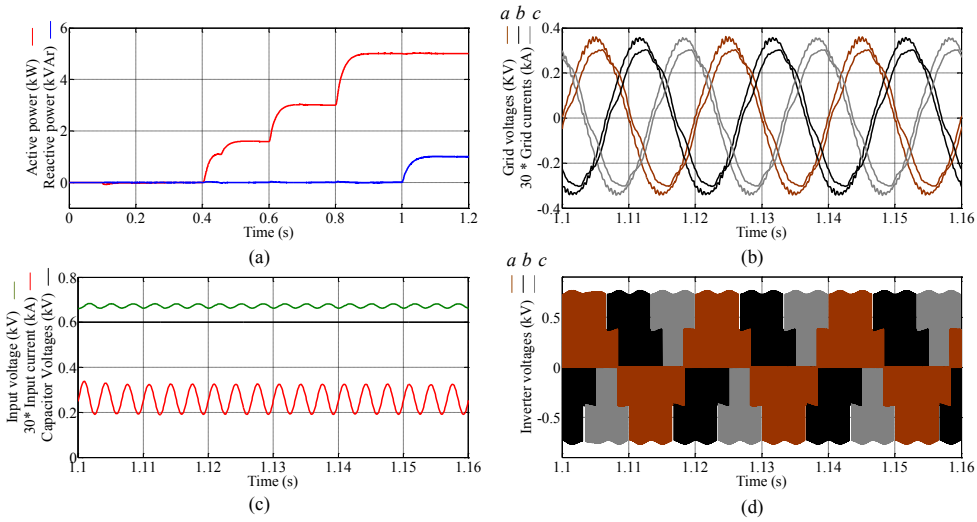


Fig. 4.22. Main waveforms with shoot-through operation. a) P and Q responses under different reference values. b) Steady waveforms of v_{grid} and i_{grid}. c) Steady waveforms of I_{in}, V_{in} and V_c (boost is seen). d) Steady waveforms of v_{inv} (with shoot-through switching states).

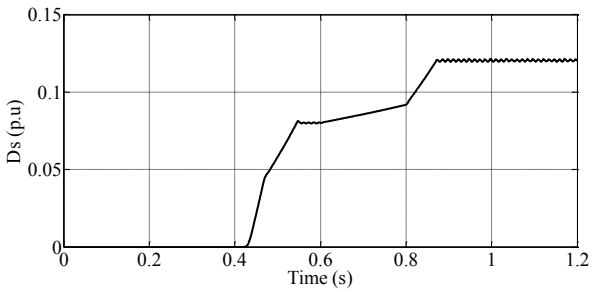


Fig. 4.23. D_s evolution.

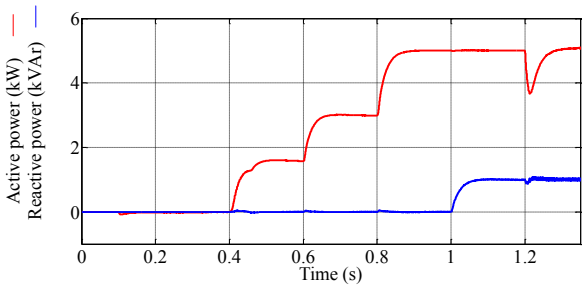


Fig. 4.24. System response during a step in input voltage.

A more extended version about the control strategy to regulate P and Q in the three-phase version is exposed in paper [**I**] of the appendix.

4.3.3 Integration with energy storage systems

This section derives from the unpredictable power generation capability of DG based on PV (Fig. 4.25 represents the power generated by a real PV plant during a sunny and cloudy days) which is defined as non-manageable power generation plant [6] due to its dependency on irradiance and temperature conditions.

The ESS deals with mitigation of inconstant PV power productions produced by changes in the irradiance. This kind of operation allows to have a better operability and production predictability of these plants when they are connected to the grid. Moreover, with the combination of a RES and ESS (battery-assisted PV system), it is possible to assure a reference active and reactive power (P^* and Q^*) to be injected into the PCC, which gives a quasi-manageable role to the 3L-NPC-qZSI.

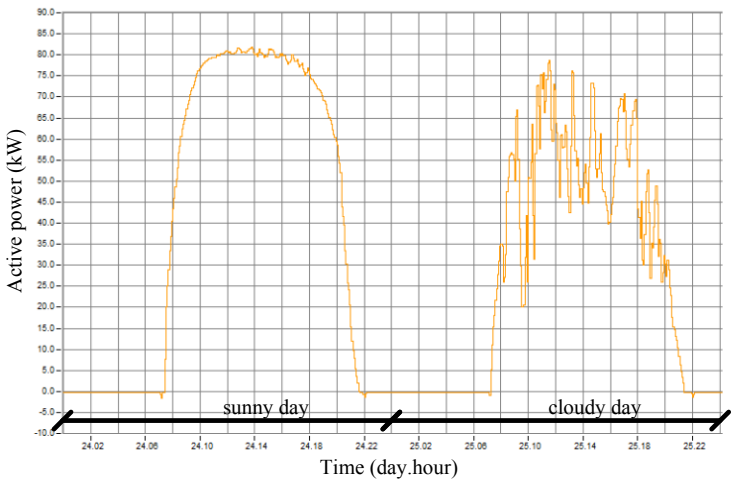


Fig. 4.25. Measured PV generation curve in a sunny and cloudy days.

Scheme presented in Fig. 4.26 can represent the aforementioned concept. The inconstant PV generation (left picture) can be compensated by the charge/discharge of any ESS (central picture) to finally assure a predictable curve to be integrated the RES with the main grid (right picture).

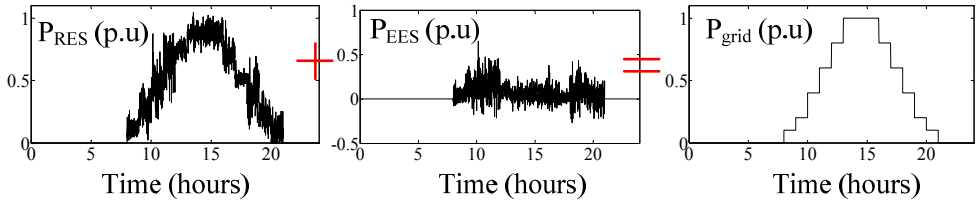


Fig. 4.26. Power balance between RES, ESS and grid.

Due to the integration of any ESS with the RES, a four quadrant operation (Fig. 4.27 a) become possible by charging or discharging the ESS, depending on the availability of P_{pv} and the grid reference power (Fig. 4.27 b).

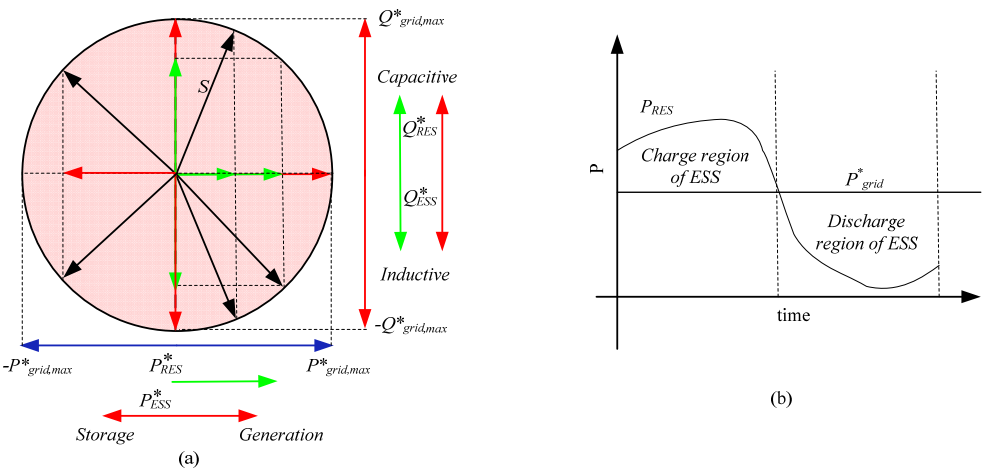


Fig. 4.27. a) Active and reactive power distribution between RES and ESS. b) Active power distribution between PV generation and battery charge/discharge.

The topology under consideration has the capability of integrating energy storage batteries. Fig. 4.28 illustrates a possible solution of battery integration for the three-phase topology. In this case battery cells are connected in parallel to the external capacitors. Another case of the integration of the energy storage battery cells is exposed in Fig. 4.29. In this case the cells are connected in the parallel to the inner capacitors. Both solutions have their advantages and disadvantages.

In general, the second solution is much simpler from the control point of view. In order to maintain the charging or discharging mode some certain voltage level must be pro-

vided on the battery cells. Taking into account the control strategy based on controlling P and Q by means of M and δ previously described, a simple charging/discharging control can be implemented.

On the other hand, second solution requires high voltage battery cells that must be approximately equal to the peak grid voltage. In the first version of integration, the nominal cell voltage can be much lower, but more sophisticated control algorithms are required.

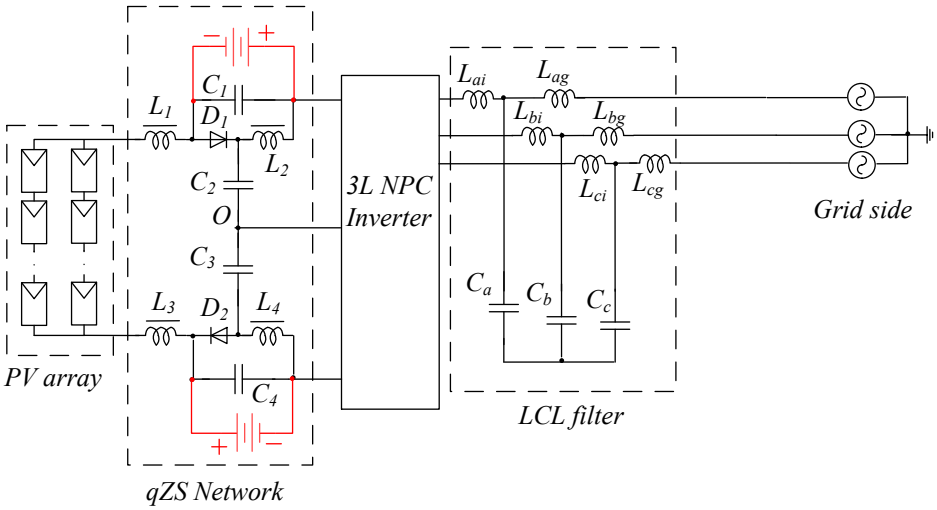


Fig. 4.28. First integration possibility of energy storage battery cells.

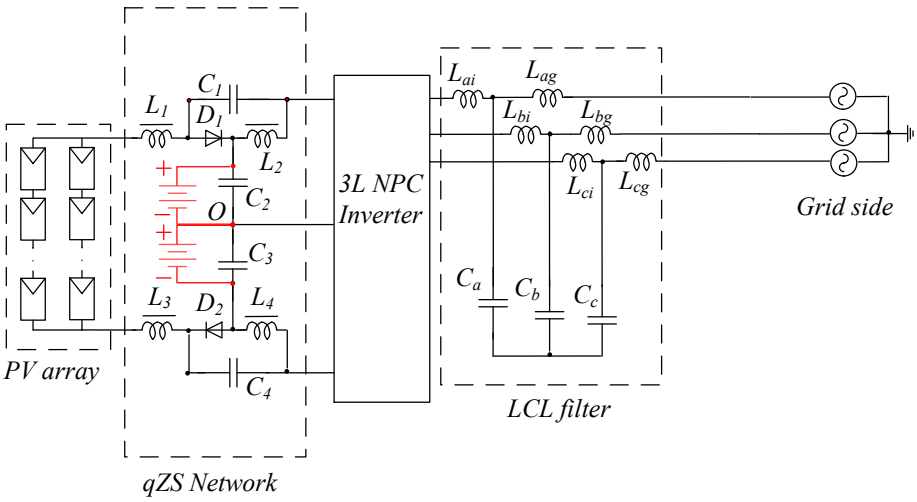


Fig. 4.29. Second integration possibility of the energy storage battery cells.

Typical discharge curve of voltage and current is depicted in Fig. 4.30, where the main parameters are full charge voltage (E_{full}), full discharge cut off voltage (E_{cut_off}), exponential point voltage or the voltage at the end of the exponential zone (E_{top}) and nominal voltage (E_{nom}). Q_{top} represents capacity at the end of the exponential zone, Q_{nom} and Q_{max} are the nominal and maximum capacity respectively.

Fig. 4.31 shows the sketch of the main functional blocks of the control strategy for integrating EES.

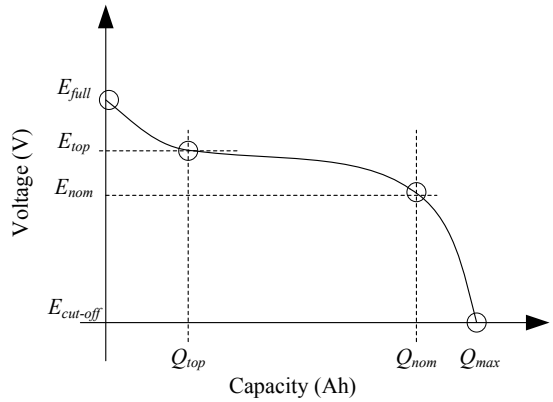


Fig. 4.30. Typical discharge curve.

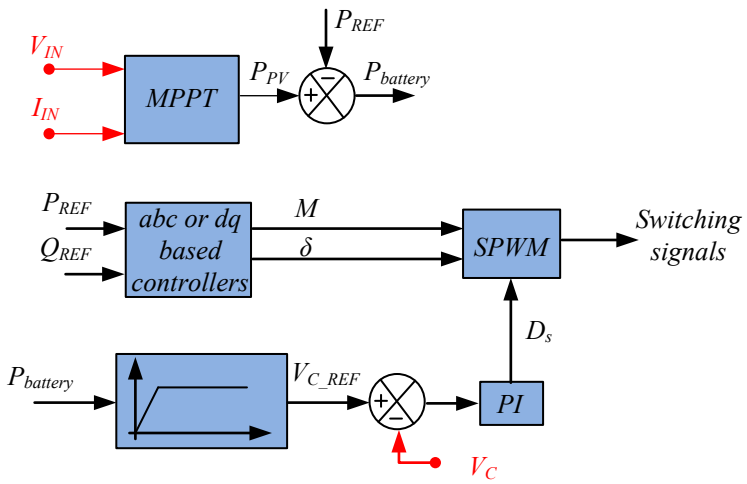


Fig. 4.31. Sketch of the simplified control strategy for charge/discharge control.

It should be mentioned that the proposed algorithm can be applied for both the above cases of the storage battery cell connection. V_c corresponds to the capacitor voltage. The main idea of the proposed scheme is to control this voltage when the output power

is constant while the power from PV varies in a wide range, which depends on the solar irradiation. Fig. 4.27 b) showed such power distribution.

If the output power from the PV array is higher than required on the output side, the $P_{battery}$ will be positive and the reference voltage level of the capacitor will be raised in order to provide battery charging. In the opposite case, the reference capacitor voltage value will be lower than the nominal value that provides the battery discharge.

A simulation study was performed to validate the previous ideas. Fig. 4.32 a) illustrates the simulation results that correspond to the charge mode of the battery. It can be seen that the capacitor voltage V_{C1} is slightly higher than the battery voltage that provides positive charging battery current $I_{battery}$.

It should be mentioned that the output power is about 1.5 kW. The input power derived from the PV panel was about 1.8 kW. It means that around 300 W are saved in the storage battery.

Fig. 4.32 b) illustrates an opposite case. It can be seen that the capacitor voltage V_{C1} is slightly lower than the battery voltage that provides the discharging battery current $I_{battery}$. In this case the input power was around 1.1 kW while the output power required the same value. It means that 400 W flow from the batteries to the output load.

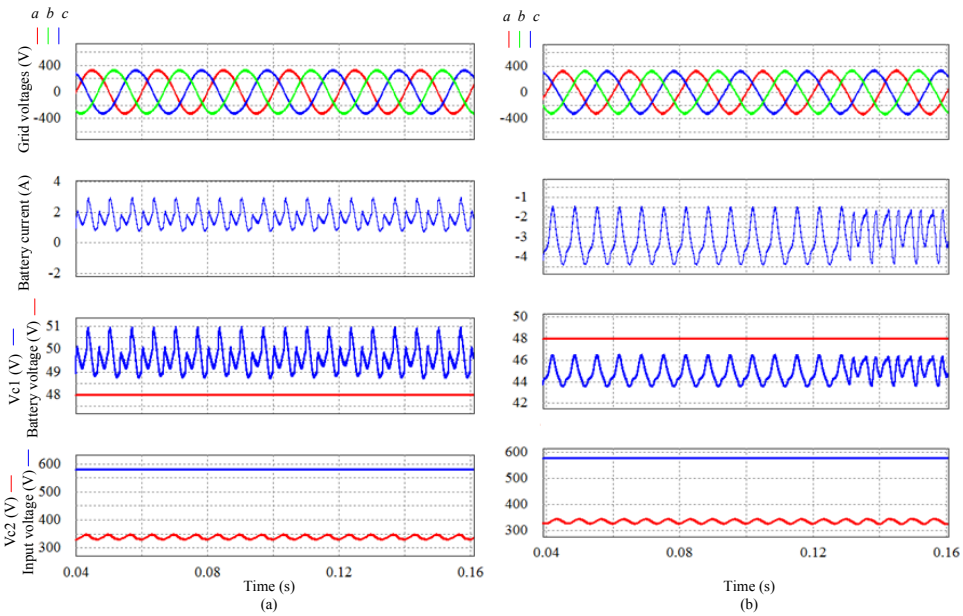


Fig. 4.32. a) Main waveforms in the charging mode. b) Discharging mode.

At the same time, it should be emphasized that the diagrams above illustrate only the operation capability of the charge/discharge control. The current shape of the batteries,

which is very important in the practical design, can be significantly improved by the implementation of an additional current control loop.

4.4 Active filtering functions

Power electronic devices are widely used in industrial, commercial and domestic applications. All of them demand non-sinusoidal current and reactive power from the source. This phenomena causes voltage distortion at the PCC, that affects to users connected to the same one (Fig. 4.33 represents this cause-effect).

Shunt active power filters (APF) [145] are one of the possible technical solutions to deal with such problem. By using proper closed loop control strategies to generate the reference currents, they can supply the reactive power and harmonic contents demanded by the load.

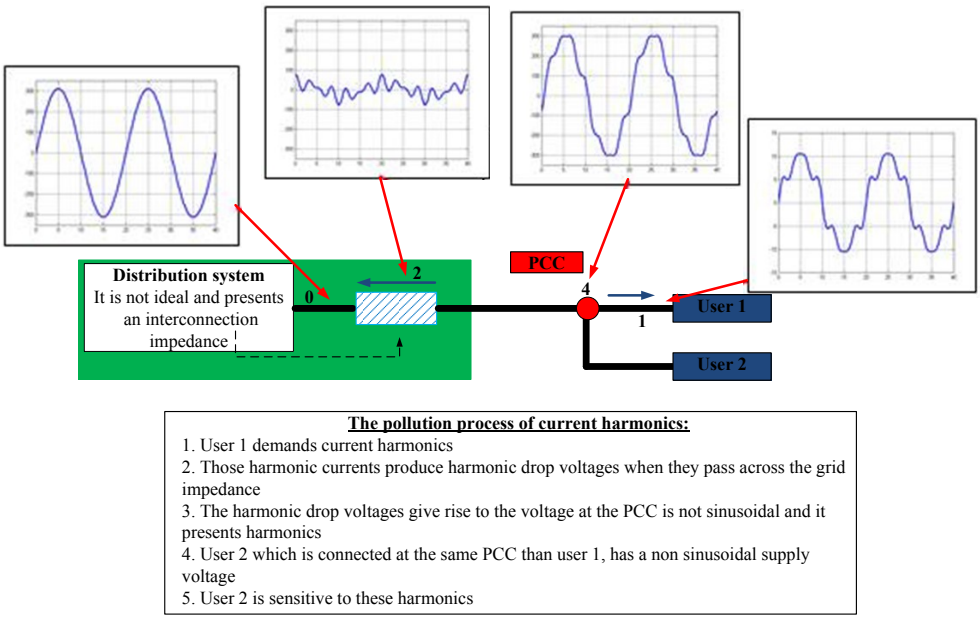


Fig. 4.33. Voltage distortion process caused by harmonic loads.

As it was explained, the current low voltage electrical systems include a lot of distributed PV inverters, which can take advantage of this distributed location to supply the non-linear loads connected to the PCC, improving in a certain way the grid voltage quality. In this sense, this section explores the abilities of the 3L-NPC-qZSI, when it is working as APF and a non-linear load is connected at the same PCC (schematic of studied case is depicted in Fig. 4.34).

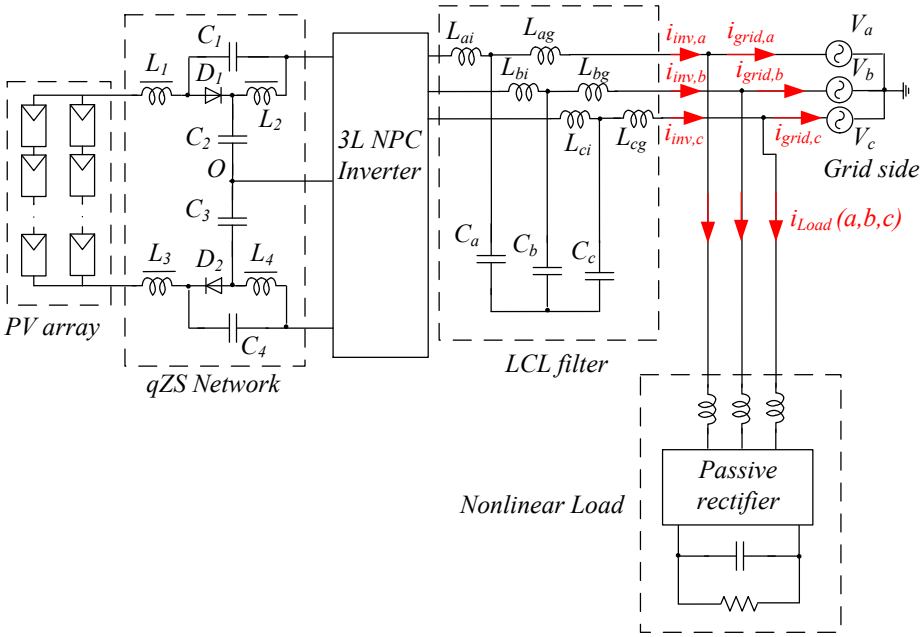


Fig. 4.34. Schematic of the studied case.

Traditional control strategies for shunt APF generate the reference current that must be provided to compensate reactive power and harmonic currents demanded by the load. This involves a set of currents in the phase domain, which will be tracked, generating the proper switching signals for the electronic converter, by means of the appropriate closed loop switching control technique such as hysteresis or dead-beat control. Four control strategies stand out among the literature. Those ones are called: *p-q* method [147], i_d-i_q method [151], unitary power factor and perfect harmonic cancellation [152].

The proposed strategy in this section is derived from the *p-q* theory approach, combined with a dc-link voltage control loop. The operation is explained below, according to scheme presented in Fig. 4.35.

Reference current of the 3L-NPC-qZSI, ($i_{inv,ref}$ (a,b,c)), is composed by the active power from the PV MPPT algorithm, reactive power ($q(t)$) and non-active power ($p(t)$- $\bar{p}(t)$) demanded by the load. Those last two terms are obtained as follows: once have been v_{grid} (a,b,c) and i_{Load} (a,b,c) sensed, they are transformed into α-β quantities (Clarke transformation) in order to calculate the instantaneous real power ($p(t)$) and the instantaneous reactive power ($q(t)$) as:

$$p(t) = v_{grid,\alpha} \cdot i_{Load,\alpha} + v_{grid,\beta} \cdot i_{Load,\beta} \tag{4.30}$$

$$q(t) = v_{grid,\alpha} \cdot i_{Load,\beta} - v_{grid,\beta} \cdot i_{Load,\alpha} \,. \tag{4.31}$$

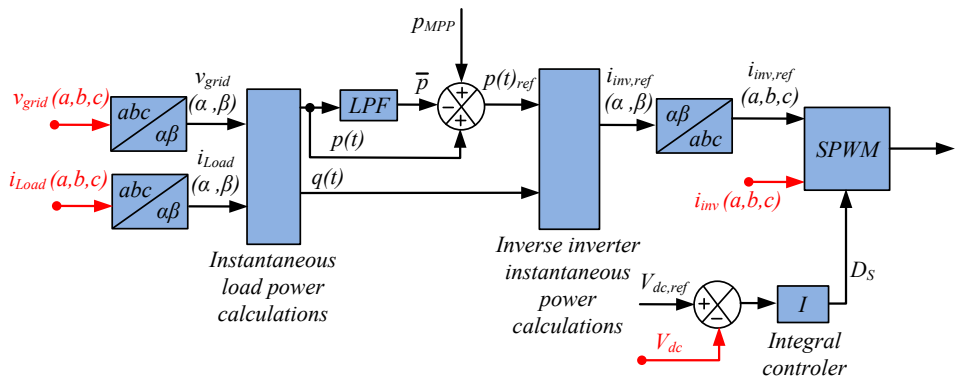


Fig. 4.35. Block diagram of the proposed control strategy.

After filtering *p(t)*, just ac component (non-active power) of *p(t)* is left. Subsequently, it is easy to obtain *α-β* quantities of $i_{inv,ref}$ *(a,b,c)* to finally turn them into phase domain currents with inverse Clarke transformation. Operating in this way, just sinusoidal current in phase with the grid voltage will be demanded from the distribution grid.

The dc-link voltage control loop is built with one integral controller, which adjusts the shoot-through duty cycle depending on the error between a predefined value for the dc-link voltage ($V_{dc,\ ref}$) and the sensed dc-link voltage (V_{dc}) (it is as indirect dc-link control method again). If error is positive, boost mode is presented in the converter.

In order to track $i_{inv,ref}$ *(a,b,c)*, a proportional controller is performed to limit the maximum current ripple. Error between reference and sensed currents is scaled with the assumed ripple. After this, it is needed to limit such value in order to take into account the possibility of including D_s due to the next constraint (implementation sketch is depicted in Fig. 4.36):

$$M \leq 1 - D_s \,. \tag{4.32}$$

The obtained values after this procedure are considered as duty cycles of the 3L-NPC-qZSI. To generate the switching signals (active states, zero states and shoot-through states), the PWM explained in section 3.5.2 is applied.

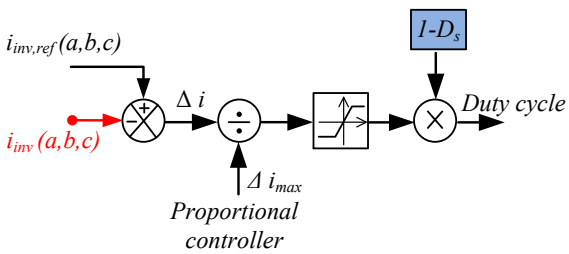


Fig. 4.36. Block diagram of duty cycle generation.

Different conditions are selected to analyze the system performance. They can be summarized in:

• No compensations.

• Reactive power and harmonic content (demanded by the load) compensation. It is assumed that the P_{MPP} is equal to zero.

• Reactive power, harmonic content compensation and the P_{MPP} is equal to fundamental active power demanded by the load.

• Reactive power, harmonic content compensation and the P_{MPP} is higher than the fundamental active power demanded from the load.

To illustrate the good performance of the full system, just the fourth case is showed below, as it is considered as the most general one. Fig. 4.37 a) represents the demanded current by the load. In this last situation, the power of the PV array at the *MPP* is higher than the fundamental active power, the power that the load is demanding. The excess of this active power is injected into the grid; hence, a sinusoidal current in phase with the voltage at the PCC is flowing into this. Waveforms of i_{inv} *(a,b,c)* and i_{grid} *(a,b,c)* are depicted in Fig. 4.37 b) and c), respectively.

Fig. 4.37 d), e) and f) show other relevant waveforms, input current into the qZ network, dc-link voltage and voltage between the middle point of branch a and the ground. Fig. 4.37 d) shows that the input current is in continuous mode. Fig. 4.37 e) and f) reveal that the converter is working in boost mode, because both voltages drop uniformly to zero during the whole fundamental period because of the insertion of ST states.

Description and waveforms of the other three considered scenarios can be found in paper [**m**] in the appendix.

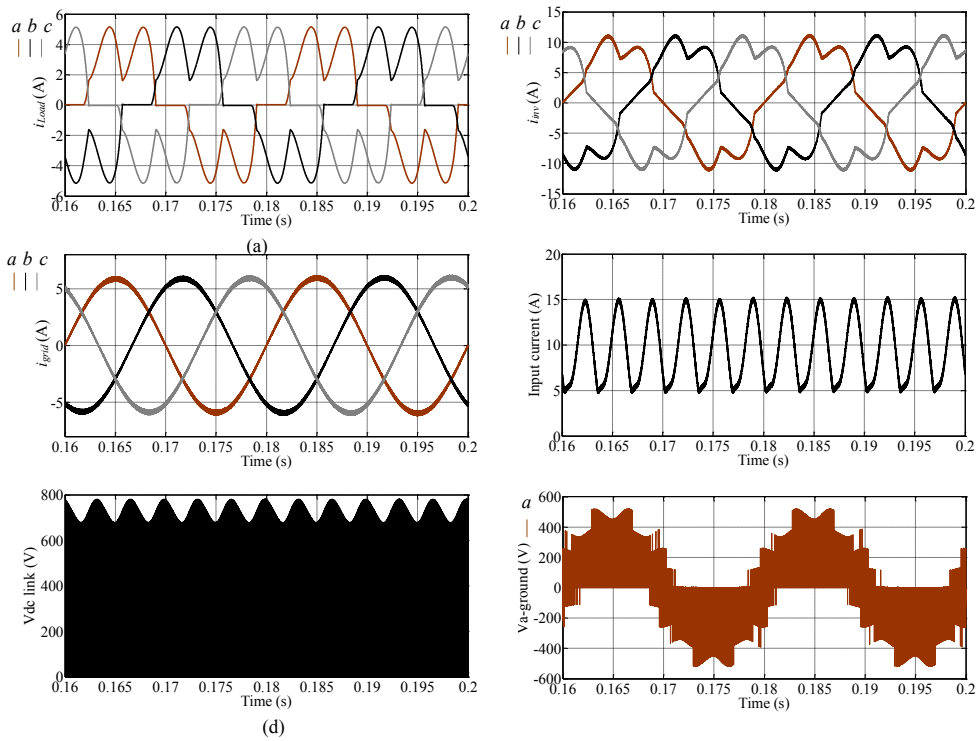


Fig. 4.37. a) Current demanded by the load. b) i_{inv} *(a,b,c)* with non-active, reactive power compensation and *MPP* power higher than power demanded by the load. c) i_{grid} *(a,b,c)* that flows to the grid. d) Input current. e) dc-link voltage. f) Voltage between the middle point of branch *a* and the ground.

Chapter 5
Conclusions and Future Works

5.1 Summary of key results

This Doctoral thesis presents a new topology from the family of single-stage buck-boost multilevel inverters – the three-level neutral-point-clamped quasi-Z-source inverter. The proposed three-level neutral-point-clamped quasi-Z-source inverter combines such advantages of the quasi-Z-source inverter and three-level neutral-point-clamped voltage source inverter topologies as low voltage stress of the switches, single-stage buck-boost power conversion, continuous input current, shoot-through withstandability, and low output voltage and current THD. Thanks to the blocking voltage of the main switches, that is reduced twice compared to the two-level topology, faster transistors can be implemented. It will result in higher switching frequencies and, therefore, a more compact impedance source network and low pass output filter. For the three phase version, MOSFET based on SiC semiconductors are used because of this new appearance in the market.

A special new carrier-based modulation technique for the three-level topology with the distributed shoot-through generation is developed. The control method proposed has the ability to balance the dc-link voltage. As a result, it obtains the capability of combining the required boost factor with the superior output voltage quality. The first and new proposed modulation method in single phase version was improved since it was observed that switching signals and duty cycles (directly connection with power losses) of switches were quite unbalanced inside of each branch. The main advantage of this second technique consists in equally distributed switching and conduction losses among two branches while the total converter efficiency remains approximately the same. The new approach was extended to the three-phase system based on the same basis. The efficiency of this inverter, in the rated power point is higher than 98 % and in the boost mode, by using shoot-through signals, efficiency is not lower than 95.5 %.

Related to the control schemes of this special inverter, it can be summarized that basically these schemes must provide coexistence of an operation strategy of the inverter, a maximum power point tracking algorithm, a dc-link voltage control method and a special modulation technique to embed the shoot-through states into the normal ones. Firstly it has been investigated how the traditional maximum power point tracking algorithms can be applied to this family of inverters. Then a new control strategy for single phase Z/qZ source inverter based on a *d-q* synchronous reference frame with an indirect dc-link control method is proposed. The control strategy generates the *d-q* reference voltage components of the inverter in order to control the active and reactive power flows. This first approach has been improved since a strong coupling between power control loops and the dc-link voltage control loop was observed. For this single phase application some difficulties were found since the original *d-q* and *p-q* theories were developed to three-phase three-wire or four-wire systems and they cannot be used directly for single-phase systems. For the three-phase system, a similar scheme was derived based in a *d-q* synchronous reference frame as well. Finally there was proposed some control schemes to explore the abilities of this new inverter to be integrated with energy storage systems and to deal with active filtering functions. With all of this functionalities the new inverter will become and active device of the electrical grid ensuring local support, quality warranties and security of supply.

5.2 Future work

Future research is related to the experimental validation of some of the new proposed control algorithms for grid-connected active functionalities of the three-level neutral-point-clamped quasi-Z-source inverter. Since the main objective was to demonstrate the abilities and high performance of this new converter, it was decided to use for the control system different embedded solutions based on FPGA. To deal with new challenges, a new prototype compatible with rapid prototyping control platform will be assembled to tune and to optimize in a faster way the control parameters.

Other future research will be the experimental comparison between different member of this family of buck/boost multilevel inverter in photovoltaic application according to certain parameters such as performance, reliability, cost and power density.

It is also interesting to remark that the influences and relationships between the impedance network and the output filter have not been reported yet in the literature. It is a possible topic for future research as well.

5.3 Resumen de resultados principales

Este trabajo de Tesis Doctoral presenta una nueva topología dentro de la familia de inversores multinivel reductores-elevadores en una sola etapa. El convertidor se denomina “inversor de tres niveles con el punto neutro fijado con fuente cuasi impedante”,

en versión monofásica y trifásica. La topología propuesta combina las ventajas inherentes a los convertidores con red impedante y las de los inversores multinivel tales como un menor stress de sus semiconductores, conversión de energía en una sola etapa con elevación, corriente de entrada en modo continuo, protección frente a cortocircuitos y menor tasa de distorsión de la tensión y de la corriente de salida. Dado que la tensión de bloqueo de los semiconductores que constituyen la nueva topología se reduce a la mitad respecto de los inversores convencionales de dos niveles, se han podido utilizar transistores más rápidos para su construcción, resultando en la operación del mismo con frecuencias de conmutación más elevadas, con elementos pasivos de la red impedante y del filtro de salidas de menor tamaño. Para la versión trifásica se emplean semiconductores MOSFET con SiC dada su novedad en el mercado.

También se ha desarrollado una nueva técnica de modulación para este convertidor que genera estados de conmutación "shoot-through" uniformemente distribuidos durante todo el periodo fundamental. Esto supone una mejora en cuanto a la calidad de la tensión de salida además de proporcionar el valor de elevación de tensión necesario. La primera propuesta que se hizo para la versión monofásica fue mejorada, pues se observó una distribución dispar del número de conmutaciones entre los semiconductores de cada rama. De esta forma la distribución de las pérdidas queda equilibrada, aumentando la fiabilidad del sistema. También se ha desarrollado la técnica de modulación para la versión trifásica de manera similar al caso monofásico, obteniéndose un rendimiento del 98 % en modo reductor y del 95.5 % en modo elevador.

En lo que respecta a los esquemas de control de este inversor se resume que en ellos debe coexistir la estrategia de operación, un algoritmo para el seguimiento del punto de máxima potencia, un método de control de la tensión del bus dc y una técnica de modulación que permita embeber los estados *shoot-through* junto con los estados normales. Primeramente se han investigado como estos algoritmos para el seguimiento del punto de máxima potencia pueden ser adaptados para este convertidor mediante el empleo de nuevas variables de control. A continuación se propone una nueva estrategia de control para la versión monofásica basada en un marco de referencia síncrono en ejes *d-q* junto con un método de control indirecto del bus de continua. Como la teoría *d-q* y *p-q* se desarrollaron originalmente para sistemas trifásicos a tres o cuatro hilos, se encontraron dificultades para su implementación en el sistema monofásico. Con el primer esquema propuesto se observó un acoplamiento importante entre los lazos de control de la potencia activa y reactiva y de tensión del bus de continua, el cual fue resuelto en una segunda versión del mismo. Finalmente se investigan otros esquemas de control para tener una idea de cómo este inversor puede realizar funcionalidades activas como el filtrado activo y una mejor gestión de la energía mediante almacenamiento. Con todas estas funcionalidades el inversor conseguirá ser un dispositivo activo conectado a la red, proporcionándole apoyo, garantizando una mayor calidad y seguridad de suministro.

From the strategy operation point of view, new trends in islanded microgrid and its particular control schemes (hierarchical control) would require the analysis of these methods and their adaptation to be used for this converter topology.

5.4 Trabajos futuros

Un trabajo futuro nacido como fruto de esta investigación es la validación experimental de algunos de los algoritmos de control propuestos para desarrollar funciones activas en conexión a red por parte de esta nueva topología novedosa. Dado que el objetivo principal fue la construcción y validación las capacidades de este convertidor con alta eficiencia, se emplearon soluciones para el sistema de control basadas en sistemas embebidos como FPGA. Para acometer estas actividades, se plantea la construcción de un prototipo compatible con plataformas de prototipado rápido, con el fin de optimizar de una manera más rápida los parámetros de control.

Otra investigación futura es la comparación experimental entre diferentes miembros de esta familia de convertidores, muy adecuados para aplicación fotovoltaica, en cuanto a parámetros como rendimiento, fiabilidad, coste y densidad de potencia.

También se destaca que la influencia y relaciones de dependencia entre los elementos pasivos de la red impedante y los del filtro de salida todavía no han sido estudiadas. Este tema de investigación se plantea también como posibilidad para el futuro.

En lo que respecta a las estrategias de control, las nuevas tendencias en microrrredes y sus esquemas de control particulares (control jerárquico) requerirían el análisis y adaptación para la aplicación en estos nuevos convertidores.

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Appendix

The author´s publications directly connected to the topic of dissertation are added in this appendix, since they are considered as an extension or continuation of the thesis document. All of them are cited in the text.

[Paper-a] Carlos Roncero-Clemente, O. Husev, V. Miñambres-Marcos, E. Romero-Cadaval, S.Stepenko and D. Vinnikov, *"Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications"*. Informacije MIDEM. Journal of Microelectronics, Electronics Components and Materials, vol. 43, pp. 212-221. 2013. (Journal listed in last third (217/248)).

[Paper -b] C. Roncero-Clemente, O. Husev, T. Jalakas, E. Romero-Cadaval, J. Zakis and V. Minambres-Marcos, *"PWM for Single Phase 3L Z/qZ-Source Inverter with Balanced Power Losses"*. ELEKTRONIKA IR ELEKTROTECHNIKA, (Electronics and Electrical Engineering), vol. 20, pp. 71-76. 2014. (Journal listed in last third (204/248)).

[Paper -c] Oleksandr Husev, Andrii Chub, Enrique Romero-Cadaval, Carlos Roncero-Clemente and D. Vinnikov, *"Voltage Distortion Approach for Output Filter Design for Off-Grid and Grid-Connected PWM Inverters"*. Journal of Power Electronics, vol. 15, pp. 278-287. 2014. (Journal listed in last third (173/248)).

[Paper -d] Oleksandr Husev, Carlos Roncero-Clemente, Enrique Romero-Cadaval, Dmitri Vinnikov and Serhii Stepenko, *"Single phase three-level neutral-point-clamped quasi-Z-source inverter"*. IET Power Electronics, vol. 8, pp. 1-10. 2015. (Journal listed in second third (113/248)).

[Paper -e] Oleksandr Husev, Carlos Roncero-Clemente, Enrique Romero-Cadaval, Dmitri Vinnikov and Tanel Jalakas, *"Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application"*. Electric Power Systems Research. Accepted for publication in 2015. (Journal listed in second third (126/248)).

[Paper -f] Oleksandr Husev, Carlos Roncero Clemente, Sergey Stepenko, Dmitri Vinnikov and Enrique Romero Cadaval, *"CCM Operation Analysis of the Single-Phase Three-Level Quasi-Z-Source Inverter"*. 15th IEEE

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[Paper -g] Oleksandr Husev, Sergey Stepenko, Carlos Roncero Clemente, Enrique Romero Cadaval and Dmitri Vinnikov, *"Single Phase Three-Level Quasi Z-Source Inverter With a New Boost Modulation Technique"*. IEEE 38th Annual Conference of the IEEE Industrial Electronics Society, IECON 2012. Montreal (Canada). 2012.

[Paper -h] Carlos Roncero Clemente, Enrique Romero Cadaval, Pedro Roncero Sánchez and Eva González Romera, *"Comparison of Two Power Flow Control Strategies for Photovoltaic Inverters"*. IEEE 38th Annual Conference of the IEEE Industrial Electronics Society, IECON 2012. Montreal (Canada). 2012.

[Paper -i] Carlos Roncero-Clemente, Enrique Romero-Cadaval, Oleksandr Husev, Dmitri Vinnikov and Serhii Stepenko, *"Grid-Connected PV System Based on a Single-Phase Three-Level qZS Inverter"*. IEEE 39th Annual Confer-ence of the IEEE Industrial Electronics Society, IECON 2013. Vienna (Austria). 2013.

[Paper -j] Carlos Roncero-Clemente, Oleksandr Husev, Enrique Romero-Cadaval and Dmitri Vinnikov, *"P and Q Control Strategy for Single Phase Z/qZ Source Inverter Based on d-q Frame"*. 23rd IEEE International Symposium on Industrial Electronics, ISIE 2014. Estambul (Turkey). 2014.

[Paper -k] Carlos Roncero-Clemente, Oleksandr Husev, Enrique Romero-Cadaval J. Zakis, Dmitri Vinnikov and M.I. Milanés-Montero, *"Simulation Study of the Grid-Connected Single-phase Impedance Source NPC Inverter with Different Control Methods"*. IEEE International Conference on Industrial Technology (ICIT) 2015. Sevilla (Spain). 2015.

[Paper -l] Carlos Roncero-Clemente, O. Husev, E. Romero-Cadaval, J. Zakis, D. Vinnikov and M.I. Milanés-Montero, *"Operation Strategy and Shoot-Through Indirect Control Method for Three-Phase Z-Source Inverters"*. IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG) 2015. Riga (Latvia). 2015.

[Paper -m] C. Roncero-Clemente, O. Husev, E. Romero-Cadaval, J. Martins, D. Vinnikov and M.I. Milanés-Montero, *"Three-Phase Three-Level Neutral-Point-Clamped qZ Source Inverter with Active Filtering Capabilities"*. 9th International Conference on Compatibility and Power Electronics (CPE2015). Lisboa (Portugal). 2015.

[Paper-a] Carlos Roncero-Clemente, O. Husev, V. Miñambres-Marcos, E. Romero-Cadaval, S.Stepenko and D. Vinnikov, *"Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications"*. Informacije MIDEM. Journal of Microelectronics, Electronics Components and Materials, vol. 43, pp. 212-221. 2013. (Journal listed in last third (217/248)).

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 43, No. 4 (2013), 212 – 221

Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications

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Abstract: This research work analyzes the most popular maximum power point tracking algorithms for an off-grid photovoltaic system based on three-level neutral-point-clamped quasi-z-source inverter topology to transfer the maximum power to the loads or storage systems. Classical methods, such as dP/dV feedback, perturb and observe method and incremental conductance, have been adapted for this novel topology and tested by simulation in SimPowerSystem from Matlab/Simulink. All of them use the shoot-through duty cycle as a control variable in dynamic conditions of irradiance to generate the reference shoot-through duty cycle in the modulation technique. In the studied case the power converter is feeding a pure resistive load in all the methods compared. Finally, the dP/dV method has been implemented in the control system of an experimental prototype and verified in a real photovoltaic system.

Keywords: Multi-level inverter, solar energy, pulse width modulation converters, neutral-point-clamped inverter, quasi-z-source inverter, shoot-through, maximum power point tracking, photovoltaic system

Sledenje točke največje moči s trinivojskim NPC quasi-Z-source neomrežnim razsmernikom v solarnih aplikacijah

Izvleček: Raziskava opisuje najbolj popularen algoritem sledenja točke največje moči za neomrežne fotonapetostne sisteme na osnovi trinivojskih NPC quasi-z-source topologij razsmernika za prenašanje največje moči v bremena ali shranjevalnike. Klasične metode, kot so dP/dV, motilno opazovalne metode in inkrementalna prevodnost, so bile prirejene za novo topologijo in preizkušene s simulacijskimi orodji SimPowerSystem in Matlab/Simulink. Za generiranje referenčnega kratkostičnega vklopnega razmerja v tehniki moduliranja vse metode za kontrolni parameter v dinamičnih razmerah sevanja uporabljajo kratkostično vklopno razmerje. V raziskavah je v vseh primerih razsmernik napajal čisto uporovno breme. Končno se je dP/dV metoda vgradila v kontrolni sistem prototipa in se preverila na realnem fotonapetostnem sistemu.

Ključne besede: večnivojski razsmernik, solarna energija, pretvornik s pulzno širinsko modulacijo, NPC, quasi-z-source razsmernik, slednje točke največje moči, fotonapetostni sistem

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1 Introduction

Today's power electrical system scenario differs essentially from the traditional configuration. Several factors such as increased electrical consumption, electricity market liberalization, the need to reduce pollution and CO_2 emissions and technological advancement are boosting the distributed generation (DG).

Photovoltaic solar energy is one of the most relevant distributed energy resources in this new scenario [1]. Due to increased use of this technology, several regu-

lations [2] have been established in order to manage the photovoltaic plant inverters. These regulations stipulate that the inverters are to provide support and stability during grid fault events and injected reactive power is necessary in order to restore the voltage at the point of common coupling (PCC), especially when voltage sag occurs.

This energy can output only DC voltage, therefore an inverter interface has to be used, which requires reduced cost and increased reliability inverter topologies. Among inverter topologies, the three-level neutral-point-clamped (3L-NPC) inverter has several advantages over the two-level voltage source inverter, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased dv/dt, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage. As a drawback, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per branch. The 3L-NPC can normally perform only the voltage buck operation. In order to ensure voltage boost operation, an additional DC/DC boost converter should be used in the input stage [3]-[5]. It is necessary because in solar energy application, a wide range regulation capability of the input voltage is required due to its dependence on irradiance (W) and temperature (T).

To obtain buck and boost performance in a single stage, the focus is turned to a quasi-Z-source inverter (qZSI). The qZSI was introduced in [6] and it can buck and boost the DC-link voltage in a single stage without additional switches.

The qZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. In addition, the qZSI has a continuous mode input current (input current never drops to zero), which makes it especially suitable for renewable energy sources (e.g. fuel cells, solar energy, wind energy).

A new qZSI topology was proposed and described in [7]. It is a combination of the qZSI and the 3L-NPC inverter. The three-level neutral-point-clamped quasi-z-source inverter (3L-NPC qZSI) has advantages of both of these topologies.

Since the mentioned topology is rather new, in all previous studies the 3L-NPC qZSI was considered as an off-grid system [7]-[10]. To be connected to the electrical grid, a wide range of conditions should be considered (synchronization with the grid voltage, MPPT, anti-islanding methods, reactive power control, etc).

This paper discusses three MPPT algorithms (dP/dV feedback, perturb and observe method and incremental conductance) by simulation that can be used in this topology, using the shoot-through duty cycle as a control variable. In our experimental investigation one of the algorithms was verified in a real photovoltaic system.

2 System description

Fig.1 shows the photovoltaic conversion system each stage of which will be explained in this section.

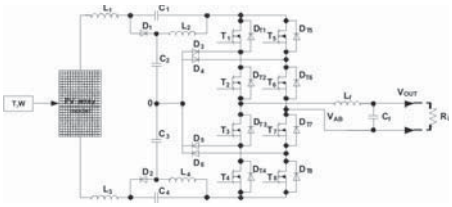


Figure1: Off-grid photovoltaic conversion system based on the 3L-NPC qZSI.

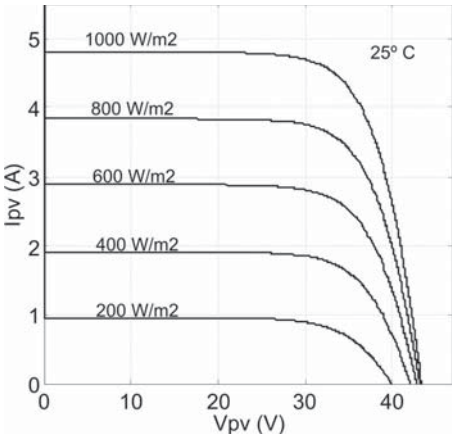
2.1 PV Array Model

Solar panels provide a limited voltage and current following an exponential I-V curve.

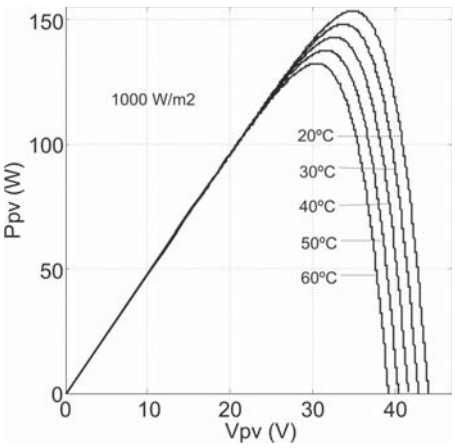
Several models have been proposed for solar panel simulation in the literature [11]-[15]. Most of them model the solar cell as an electrical equivalent circuit where such parameters as junction resistor between P-N unions, the contact resistor between cells and metal parts (R_s) and the resistor for shunt currents (R_{sh}) are needed. In [11-13], even the diode factor and the effective cell area are necessary. These parameters are not provided by the solar panel manufacturers in datasheets, which makes it difficult for engineers and users to apply these models.

Due to these reasons, a mathematical model based on I-V exponential curves and parameters provided by manufacturers in a datasheet was used to simulate the PV array. Mathematical foundation is detailed in [16]. By means of this model and the appropriate series-parallel association of modules, any PV array could be simulated. The family of I-V and P-V curves simulated in different conditions of temperature (T) and irradiance (W) for the case of solar panel Shell SP150-P [17] is shown

in Fig. 2 a) and b). The values of V_{oc}, I_{sc}, I_{MPP} and V_{MPP} were achieved with an error less than 1% in comparison with those provided by the manufacturer.



(a)



(b)

Figure 2: a) I-V family curves changing irradiance. B) P-V family curves changing temperature.

2.2 DC/AC Interface

DC/AC conversion is carried out by means of a single phase 3L-NPC qZSI [7]. This topology presents some particular features, such as continuous input current, higher switching frequency due to lower switching losses, balanced neutral-point voltage and high quality of the output voltage in comparison with traditional inverters providing benefits in PV conversion applications. One of the most important capabilities of the qZS family of inverters is the possibility of boosting the input voltage by means of shoot-through switching states. This boosting possibility avoids the use of a DC-DC boost converter between the PV array and the inverter to achieve the MPP operation and the control of the system. Passive elements of the qZ network have been calculated according to the method proposed in [9].

2.3 Output Filter and Load

An L-C filter has been chosen to minimize the THD of the output voltage. Filter values have been calculated according to the guidelines in [18]. It is based on current and voltage ripples among others criteria.

To analyze the transferred power from the PV array to the load, a pure resistive load is connected between the branches.

3 Modulation technique

A special sinusoidal pulse-width modulation (SPWM) technique was implemented in order to generate the switching signals of the power converter.

There are two kinds of switching signals to generate separately in ZS and qZS inverters. On the one hand, it is necessary to generate the normal switching signals (S_{Π}) in order to track the reference signal. On the other hand, the shoot-though states must to be added carefully.

Some requirements must be satisfied when shoot-through states are generated, for instance, the average output voltage should remain unaffected and the shoot-through states have to be uniformly distributed during the whole output voltage period with constant width. These features result in several advantages, such as minimum ripple of the input current, minimum value of the passive elements, reduction of the THD of the output voltage, and gaining of the desired boost factor.

In this work the modulation technique proposed in [10] was used to achieve the aforementioned features. Fig. 3 shows the generation of the normal and shoot-through switching states with this modulation technique and Fig.4. depicts its implementation sketch.

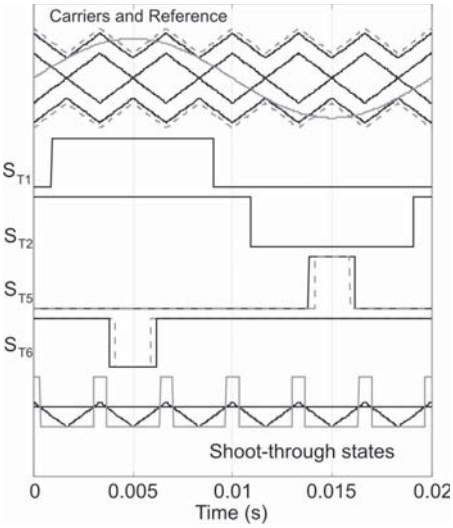


Figure 3: Simulation of the used shoot-through modulation technique.

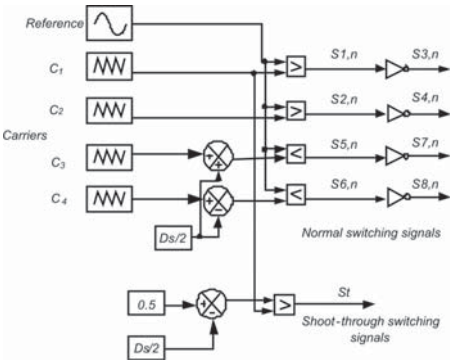


Figure 4: Sketch of the implementation of the modulation technique.

4 MPPT algorithms for 3l-npc qzsi

Tracking the maximum power point (MPP) of a PV array is necessary due to the high cost of solar panels and the dependence of power with W and T [19], being an essential task of PV inverters. In this way, many maximum power point tracker (MPPT) algorithms have been proposed in the literature [20]. Those methods vary in complexity of implementation, sensors required, convergence speed, cost, range of effectiveness and hardware implementation among others [20].

Three most traditional MPPT algorithms are highlighted due to their capabilities: perturb and observe (P&O), incremental conductance (InC) and the method based on DP/dV or dP/dI feedback.

Explained in this section, these MPPT methods have been adapted for the 3L-NPC qZSI topology. All of them work using the shoot-through duty cycle (D_s) as a control variable to track the MPP in dynamic irradiance conditions as well.

Fig. 5 shows the block diagram of the photovoltaic conversion system to be controlled in which the MPPT algorithms have been implemented.

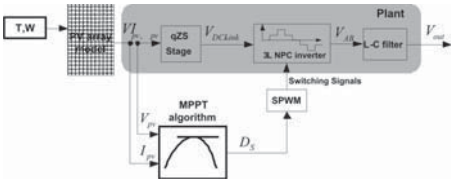


Figure 5: Block diagram of the studied photovoltaic conversion system.

4.1 Method Based on dP/dV Feedback

One way to achieve the MPP operation is to calculate the slope (dP/dV) [21]-[25] of the PV array power curve and feed it back to the converter with any control method to drive such slope to zero.

Depending on the topology and the mode of working of the converter, the slope can be computed in different ways. In our case, a PI controller that adjusts the D_S of the shoot-through modulation technique explained in section III is used to drive the slope to zero. The PI controller was tuned manually, looking for a slow response without error in steady state. This fact is considered to emulate the inertia and the response times of the electrical grid (synchronous machines and conventional power plants) to avoid instabilities and transient non-desired effects [26] when the converter is connected to the grid. Fig. 6 shows the implementation scheme of the MPPT algorithm based on dP/dV feedback for the 3L-NPC qZSI using the D_s as a control variable.

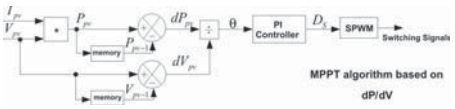


Figure 6: Implementation scheme of dP/dV feedback method.

4.2 Perturb and Observe Method (P&O)

This method [27]-[29] has been used by many researchers in different ways but the idea remains the same. A perturbation in the voltage of the PV array is perturbing the PV array current, resulting in the modification of the PV array power. By means of the increment of the PV voltage when the operation is on the left of the MPP, the PV power is increased and the PV power is decreased if the operation is on the right of the MPP. The same reasoning is possible when the PV voltage is decreased. If one perturbation in one direction produces the increment of the PV power, the next perturbation should be in the same direction and if it is not the case, the perturbation has to be reverse. Table I summarizes the process.

To produce the perturbation in the voltage of the PV array of our case where the DC/AC is converted by a 3L-NPC qZSI, perturbations in the D_s are inserted. The value of this perturbation is equal to 0.005. By means of this process the MPP is reached and the system oscillates around the MPP, as shown in Fig. 7 (points A and B). Fig. 8 depicts a sketch of the implementation of this method.

Table 1: Summary of MPPT Algorithm Based on P&O

Perturbation	Change in Power	Next Perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

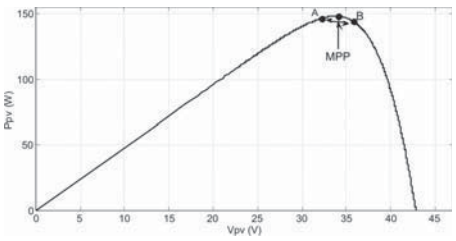


Figure 7: Power operation with the P&O MPPT method.

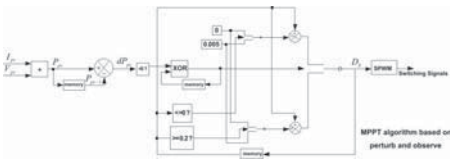


Figure 8: Implementation scheme of the P&O method.

4.3 Incremental Conductance (IncCond)

This method [30]-[31] analyzes the slope of the PV array power curve. This slope is zero at the MPP, positive on the left of the MPP and negative on the right. Thus:

$$\frac{dP}{dV} = \frac{d\,(IV)}{dV} = I + V\,\frac{dI}{dV} \cong I + V\,\frac{\Delta I}{\Delta V} \qquad (1)$$

and as a consequence, the incremental conductance ΔI/ΔV is equal, greater than or less than –I/V at the MPP, on the left of the MPP and on the right of the MPP, respectively. The MPP can be tracked by comparing the instantaneous conductance (I/V) with the incremental conductance (ΔI/ΔV) as the flowchart in Fig. 9 shows. In our case by changing D_s, the voltage V_{pv} where the PV array is forced to operate is changed, trying to find the MPP (ΔI/ΔV= –I/V).

The size of the incremental step (changes inserted in D_s) determines the convergence (velocity and accuracy) of this MPP tracking method. Using larger increments in the control variable, the system will be faster but it will not operate close to the MPP. The step size was designed taking into account the same criteria as the tuning of the PI controller in the method based on dP/DV feedback.

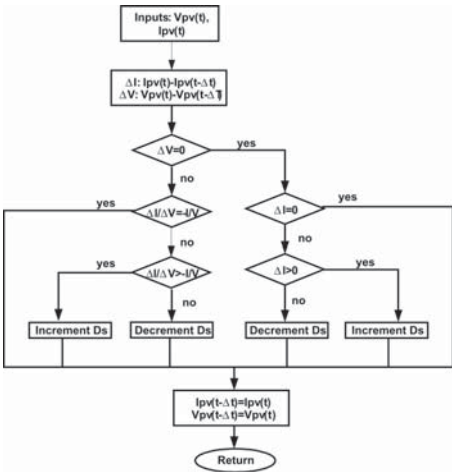


Figure 9: Incremental conductance flowchart.

5 Simulation results

In order to verify the explained MPPT algorithms, a comprehensive simulation study was performed in SimPowerSystems of Matlab/Simulink. Parameters of

the simulation are described in Table II. To analyze the transferred power to the load and the effectiveness of each MPPT method, a smooth step (Fig. 10. a) in the irradiance from 1000 W/m2 to 900 W/m2 (Fig. 10. b)) in second eight up to sixteen was made while the temperature was maintained constant (25 ºC). This action emulates the shadows phenomena. Fig. 11 shows the evolution of the transferred power from the PV array to the load and the evolution of the control variable (D_s) in dynamic conditions by using each MPPT algorithm.

Table 2: Simulation parameters.

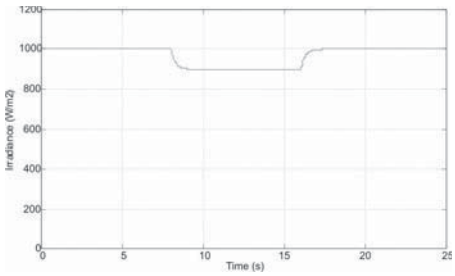
Group	Parameter	Description and unit	Value
PV Array	V_{oc}	Open circuit voltage (V)	43.4
	I_{sc}	Short circuit current (A)	4.8
	I_{MPP}	Maximum power point current (A)	4.4
	V_{MPP}	Maximum power point voltage (V)	34
	N_S	Series connected panel	7
	N_P	Parallel connected panel	1
Passive Elements	Inductors L_1,L_3	(mH)	2.55
	Inductors L_2,L_4	(mH)	0.255
	Capacitor C_1,C_4	(mF)	4
	Capacitor C_2,C_3	(mF)	1.3
	R_{load}	(Ω)	60
	C_{filter}	(μF)	0.47
	L_{filter}	(mH)	4.4
dP/dV	K_p	Proportional constant of PI controller	0.001
	K_i	Integral constant of PI controller	0.01
P&O		Perturbation size in D_s	0.005
Inc Cond		Perturbation size in D_s	0.005

5.1 Method Based on dP/dV Feedback

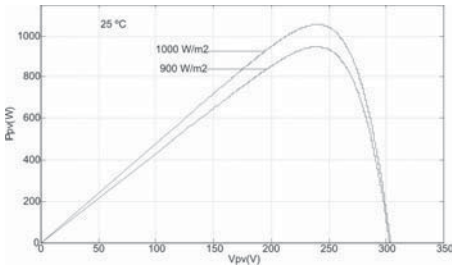
Figs. 11 (a) and 11 (b) show the evolution of the transferred power to the load and the evolution of the D_s when the MPPT algorithm based on *dP/dV* feedback is working. We can see how the system works in the MPP in each level of irradiance at high accuracy by means of the adjustment of the D_s. It is important to pay attention to some singularities (second sixteen) that could appear when any of the denominators (dV) are equal to zero during the iterative process. The algorithm must be protected against this cause of instability.

5.2 P&O

Figs. 11 (c) and 11 (d) show the evolution of the output power and the D_s in the case of the P&O method. The



(a)



(b)

Figure 10: a) Smooth step applied in the solar system. b) P-V array curves in each level of irradiance during the step.

system again tracks the MPP with accuracy. In this case the system is working around the MPP.

5.3 IncCond

In Figs. 11 (e) and 11 (f) the same variables are shown for the third presented MPPT algorithm. The MPP is also achieved in each level of irradiance using this method.

6 Analytical comparison

In order to compare the exposed MPPT algorithms for a 3L-NPC qZSI, each algorithm is analyzed in this section.

According to the number of required sensors, all of them need the measure of voltage and current of the PV system to track the MPP. There are other traditional algorithms, such as the MPPT algorithm based on the fractional control of V_{oc} and I_{sc} or the method based on the DC link capacitor drop control that only requires the measure of one variable.

In terms of the complexity of the implementation of the analyzed methods, perturbation and observation and incremental conductance are of low complexity level because they are based on simple mathematical

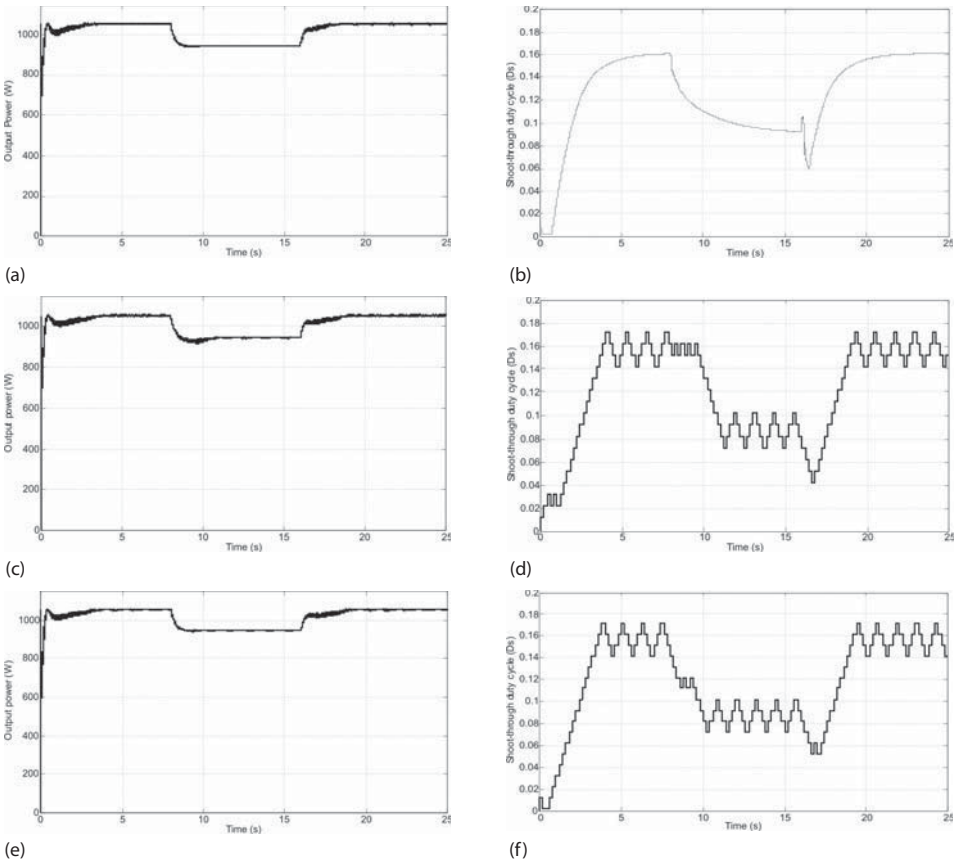


Figure 11: Evolution of transferred power and the evolution of Ds during a step in irradiance in each MPPT algorithm analyzed.

calculations. The MPP tracking algorithm based on dP/dV feedback is more complex due to the necessity to tune a PI controller and the calculation of a division of derivates in which it is necessary to prevent possible denominators equal to zero.

Another interesting feature is that the three algorithms can be implemented in digital or analogical technologies.

The speed of convergence of each method is quite different. On the one hand, methods based on perturbation and observation and incremental conductance present a variable speed that depends on the size of the step. A larger step produces faster convergence but at the same time, lower accuracy is achieved because the oscillation around the MPP will be larger. On the other hand, the MPPT algorithm based on dP/dV feedback, in general, has fast convergence. This speed depends on the parameters of the PI controller. In our case, every method has been implemented to find a slow response without error in steady state. This fact is considered to emulate the inertia and the response times of the electrical grid (synchronous machines and conventional power plants) to avoid instabilities and transient non-desired effects when the converter is connected to the grid and some changes in the irradiance or temperature occur. Also, the designed D_s gap of each method has been chosen between 0 and 0.2. Maximum power per used panel is 149.6 W when irradiance and temperature are 1000 W/m^2 and 25 ºC. After the step when irradiance decreases to 900 W/m^2, the maximum power is 135.17 W per panel. In the studied case where there are seven panels connected in series,

the array maximum power is 1054 W and 946.2 W in each situation. Using any of the studied methods, such values were achieved with accuracy.

7 Experimental results

In this section the experimental tests are explained. The chosen MPPT algorithm to be implemented in the experimental prototype is based on the adapted P&O using D_s as a control variable to introduce the perturbation in the system to reach the MPP. It is due to several reasons: it has a simple structure which allows an easy implementation: only two sensors are needed (to measure I_{pv} and V_{pv}), it can be used for digital or analog systems and it is not necessary to adjust any control system as a PI controller among others.

The converter built is described below. Table III shows the parameters of the experimental prototype of the 3L-NPC qZS inverter, with values of passive elements and also the type of semiconductors indicated. Passive elements were calculated according to [9] and [18], as in simulation studies. Fig. 12 shows the full system.

The control system is implemented in a low cost FPGA Cyclone IV family from Altera company [8]. Flexibility is the main advantage of this option, which allows realizing the shoot-through modulation technique with digital signal processing at high sample frequency. The measurement board is composed of the required current and voltage sensors.

Table 3: System parameters of the experimental prototype.

ELEMENT	VALUE OR MODEL
Control Unit (FPGA)	Cyclone IV EP4CE15E22C8
Driver Chip	ACPL-H312
Power switches	FCH47N60NF
qZS and clamp diodes	CREE C3D20060D
Input DC voltage U_N	220-450 V
Nominal Output AC voltage U_{OUT}	230 V
Capacitance value of the capacitors C_1, C_4	4000 µF
Capacitance value of the capacitors C_2, C_3	1000 µF
Inductance value of the inductors L_1 ... L_4	145 µH
Inductance of the inverter filter inductor L_i	560 µH
Inductance of the grid filter inductor L_{gi}	200 µH
Capacitance of the filter capacitor C_f	0.47 µF
Switching frequency	100 kHz

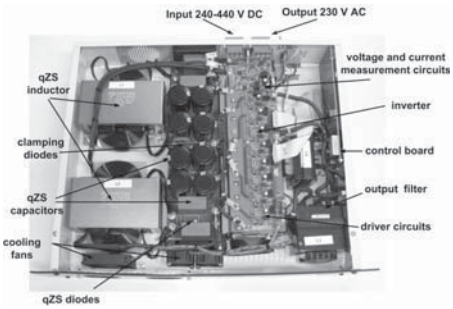


Figure 12: 3L-NPC qZS experimental prototype.

The experimental tests were carried out with a solar array composed of 14 modules LDK 185 D-24 (s), the principal parameters of which in standard conditions of W and T are shown in Table IV. Two strings of 7 serial panels were connected in parallel (2x7 configuration) to obtain a proper input voltage range. The output power is transferred to a pure resistive load.

Table 4: Parameters of module LDK 185 D-24 (s).

Parameters	Value at standard conditions (1000 W/m^2 and 25 ^{o}C
Nominal output power (Pmax)	185 W
Voltage at Pmax (Vmpp)	36.9 V
Current at Pmax (Impp)	5.02 A
Open circuit voltage (Voc)	45.1 V
Shot circuit current (Isc)	5.48 A

Fig. 13 shows the obtained results after reaching the maximum power point operation: the output current, output voltage, input PV voltage and input PV current.

Output magnitudes have a high level of quality. Measured total harmonic distortion (THD) with YOKOGAWA DL850 V equipment is 1.5 %. Input PV voltage presents a low frequency ripple at 100 Hz. It is typical of single phase systems. Input PV current presents this low frequency ripple and also ripple at high frequencies due to the switching frequency.

The transferred output power to the load is 1945 W, corresponding to the solar array maximum power at real conditions.

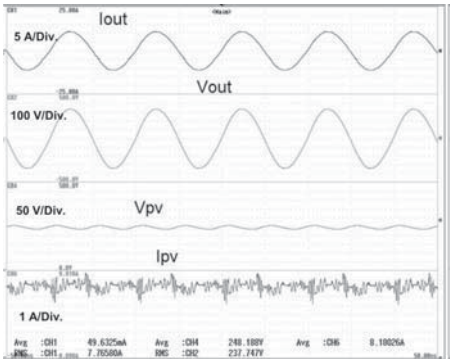


Figure 13: Experimental results at the maximum power point operation. From top to bottom: output current, output voltage, input PV voltage and input PV current.

8 Conclusions

Three traditional maximum power point tracking algorithms (methods based on dP/dV feedback, perturb and observe and incremental conductance) have been compared by means of simulation using SimPowerSystem of Matlab/Simulink. Each method has been adapted for a 3L-NPC qZSI using the shoot-through duty cycle as control variable to reach the MPP operation. Theoretical fundamentals and simulation results have been presented and discussed according to different criteria in order to choose the best solution for a real system. The P&O method, as the best solution, was chosen and implemented in the prototype and validated in a real solar plant.

9 Acknowledgment

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PWM for Single Phase 3L Z/qZ-Source Inverter with Balanced Power Losses

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***Abstract*—This paper presents a new modified carrier based single phase modulation technique with maximum constant boost control for three level Z or qZ-source inverter topology. The proposed technique is explained, analysed and compared with the previous one in simulation as well in experimental way. Obtained results are compared from the point of view of power losses in the electronic switches. Advantages and disadvantages of the converters performance based on the proposed modulation techniques implementation are discussed.**

***Index Terms*—Power conversion, pulse width modulation converters, solar energy, power semiconductor switches.**

I. INTRODUCTION

There are several modulation techniques or shoot-through control methods in the literature for single phase or three-phase two level Z source inverters [1]–[4]. Mainly, these controls are classified in: simple boost (SBC) [1], maximum boost (MBC) [2], maximum constant boost (MCBC) [3] and modified space vector modulation (MSVMBC) [4]. They have been used for controlling converters in several applications such as PV solar energy and fuel cells among others [5]–[6]. In addition, all those techniques can be used for qZ voltage source inverter [7].

In order to select the most appropriate one, it is necessary to take into account many key aspects as: shoot-through (Ds) states must be carefully and centrally added (uniform distribution), size of the passive elements (direct connection with the cost of the converter), THD of the output voltage, DC-link voltage ripple, switch voltage stress, inductor current ripples, efficiency, boost capabilities and the final application of the energy conversion. In [8], a deep experimental comparison between different modulation techniques for three-phase two levels Z-source inverter is discussed according to some aforementioned criteria. The main comparative results are represented in Table I. MCBC method is presented as a best option among the others.

Focusing now the attention on multilevel inverter topologies, modulation and control methods have had a high level of dedication by researchers in the last years [9]–[15].

A perfect comparison between different modulation methods was presented in [11]. They divide the modulation methods for multilevel converter in two main groups: space vector based methods and carrier based methods. Fig. 1 illustrates such classification just in case of high frequency applications.

TABLE I. MODULATION TECHNIQUES FOR Z OR QZ SOURCE INVERTER [8].

Modulation technique	SBC	MBC	MCBC	MSVMBC
Criteria				
Line voltage harmonic	-	+	0	+
Phase current harmonic	0	0	+	-
DC-Link voltage ripples	0	-	+	0
Switch voltage stress	0	+	0	-
Inductor current ripples	0	-	+	-
Efficiency	0	+	+	-
Obtainable AC voltage	0	0	+	-
Total	-	+++--	+++++	+----

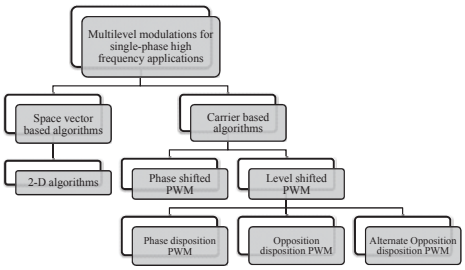

Fig. 1. Classification of multilevel high frequency modulation techniques.

Due to the aforementioned characteristics and recommendations, a new level shifted PWM (LS-PWM) in phase opposition disposition with MCBC was proposed in [16] for controlling a single-phase 3 level Neutral-Point-Clamped quasi-Z source Inverter (3L NPC qZSI) (Fig. 2). This modulation technique and its switching signal generation are depicted in Fig. 3. Also, it is explained in details in [16].

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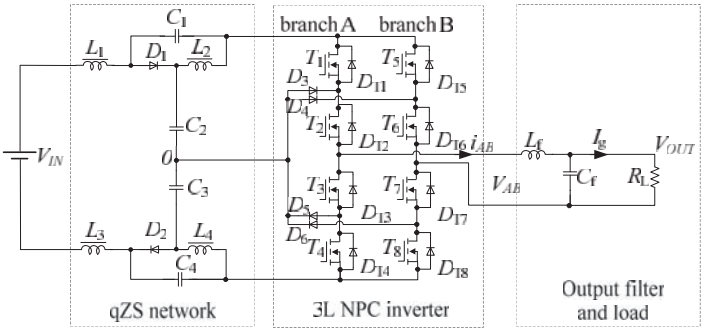

Fig. 2. Single-phase 3 level Neutral-Point-Clamped quasi-Z source inverter topology.

This modulation technique has been implemented and used in different works with success [7], [17]. But, at the same time, it is observed that switching signals and duty cycles (directly connection with power losses) of switches are quite unbalanced inside of each branch. This phenomenon can be observed in Fig. 3. In this technique, four carrier signals (C1, C2, C3 and C4) are required to generate the switching signals and C3 and C4 are shifted their level the amount of Ds/2 in order to compensate the average output voltage [16] when the Ds is applied.

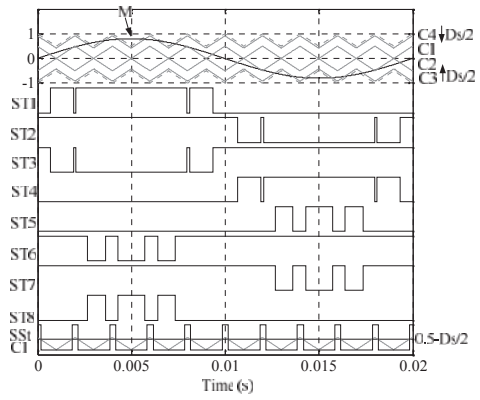

Fig. 3. Asymmetrical carrier-based PWM switching generation.

This paper proposes a new LS-PWM in phase disposition with MCBC which improves to the previous one from the point of view of balancing the power losses between branches. The new modulation technique can be used for Z-source or qZ-source 3 level topologies in single phase applications. Both modulation techniques have been compared and analysed as in simulation as experimentally. Such comparisons demonstrate that by using the new modulation technique, the proposed goal is achieved, presenting a better distribution of the power losses between branches and even between switches of each branch.

II. NEW BALANCED MODULATION TECHNIQUE

As it was exposed in previous chapter, the goal of developing a new modulation technique is to improve the previous one by means of balancing the power losses between branches. Those power losses are produced during switching states (switching losses) and also during on states (conduction states) in each electronic switch. Both losses must be taken into account in order to distribute them among branches of the converter. In this way different rates of the converter are improved such as: Mean Time to Failures (MTTF) and Mean Time between Failures (MTBF). As consequence, the reliability and the useful life of the converter will increase.

Figure 4 shows a simulated generation without and with shoot-through switching states based on new modulation technique. It has been used a modulation frequency index (m_f) equal to 10 (for a better representation), shoot-through duty cycle equal to 0.16 and the modulation index (m) is 0.84. Figure 5 illustrates the implementation sketch of the proposed modulation technique.

Two modulating sinusoidal waves (M1 and M2, one per branch) are compared with two level shifted triangular carriers (C1 and C2) in phase disposition. The result of this operation is obtaining the normal states of T1, T2, T5 and T6. T3, T4, T7 and T8 have the complementary states of the others, respectively. It is easy to detect in Fig. 4 that switching states of analogous switches are the same in both branches so power losses will be also the same.

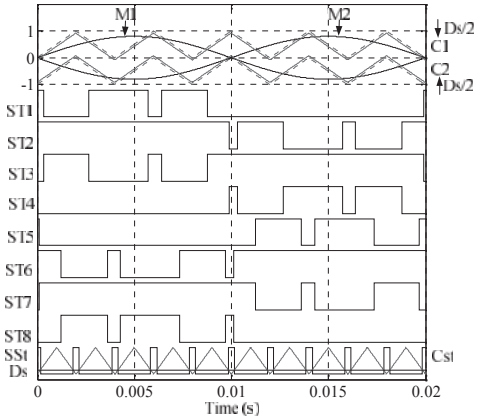

Fig. 4. Switching signals generation of the balanced modulation technique.

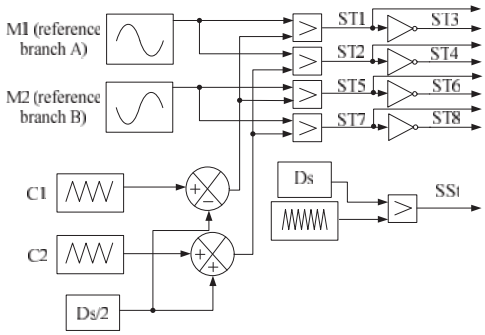

Fig. 5. Sketch of the implementation of the modulation technique.

The generation of the shoot-through states (SSt) is done by means of the comparison between Ds and one triangular carrier (Cst) at twice frequency than C1 and C2. Operating in this way, the symmetry of the output voltage is maintained and also MCBC is achieved. At the same time it is required to compensate the average output voltage (V_{ab}) when the shoot-through states are applied. It is done by shifting C1 and C2 quantities -Ds/2 and Ds/2 respectively.

III. ANALYTICAL COMPARISON BETWEEN PWM TECHNIQUES

In order to compare the previous and the proposed PWM in a quantitatively way, a comprehensive simulation study was performed in PSCAD.

First of all, the number of switching transitions (times) per switch during one fundamental period (defined at 50 Hz) were analysed in both PWM (Table II). These numbers or parameters are related to the switching losses and it are represented in Fig. 6(a) and Fig. 6(b) for each modulation technique as a function of m_f respectively (Ds is equal to 0.16).

TABLE II. ANALYSIS OF NUMBER OF SWITCHING SIGNALS PER SWITCH.

Previous modulation technique / Proposed modulation technique	Switching times at 100 kHz and Ds to 0.16	Switching average times per branch at 100 kHz ($\overline{T}_i$)	Standard deviation per branch (σ_{Ti})	Standard deviation of full converter
T1	3325	2658.5	769.6	1631
	3830			
T2	1992			
	1984			
T3	1992	2907	1065.8	
	1984			
T4	3325			
	3830			
T5	5308	3308	2309.4	987.1
	3830			
T6	1308			
	1984			
T7	1308	2907	1065.8	
	1984			
T8	5308			
	3830			

We can see as in Fig. 6 as well in Table II that in previous modulation technique, branch B presents higher internal unbalance between switching numbers (T5 and T8 switch 4 times more than T6 and T7). Branch B also presents more switching numbers unbalance in comparison with branch A than in proposed modulation technique (see σ_{Ti} in Table II). It is due to branch B just deals with compensating V_{ab} by changing the voltage V_{bo}. The compensation of the V_{ab} is done by both branches of the converter in the proposed PWM.

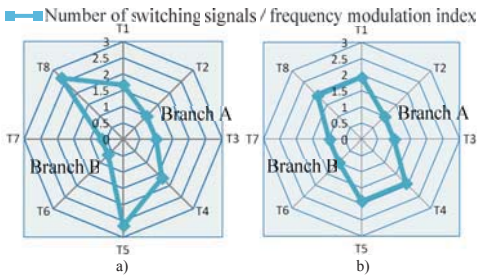

Fig. 6. Number of switching signals per switch/frequency modulation index in one fundamental period. Unbalanced modulation technique (a). Proposed modulation technique (b).

TABLE III. ANALYSIS OF T_{ON} PER SWITCH.

Previous modulation technique / Proposed modulation technique	T_{on} (ms)	Average Ton per branch ($\overline{T}_{ON,i}$)	Standard deviation per branch ($\sigma_{TON,i}$)	Standard deviation of full converter
T1	10.161	11.6	1.66	4.06
	8.291			
T2	13.039			
	14.9095			
T3	13.039	11.6	3.82	
	14.9095			
T4	10.161			
	8.291			
T5	6.4239	11.6	5.97	3.53
	8.291			
T6	16.7763			
	14.9095			
T7	16.7763	11.6	3.82	
	14.9095			
T8	6.4239			
	8.291			

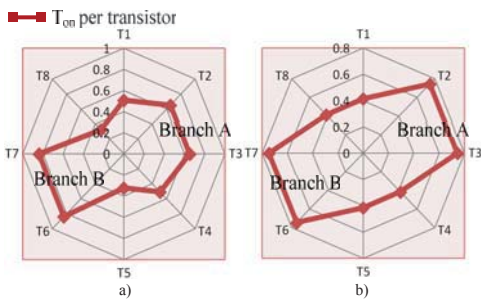

Fig. 7. T_{on} per switch during one fundamental period: Unbalanced modulation technique (a); Proposed modulation technique (b).

Secondly, the duty cycle of each switch (T_{on}) was calculated (Table III).

These values are related to the conduction losses and are represented in Fig. 7. The same conclusions are produced in the case of previous modulation technique. Branch B has a high level of conduction unbalance between its switches (T6 and T7 conduct 2.6 times more than T5 and T8) and also a different duty cycles with the analogous switch from branch A. New proposed PWM provides the same T_{on} of each analogous pairs of switches between branches and less unbalance within the branch.

We can conclude that by using the proposed modulation technique, both branches are symmetrically balanced from the point of view of switching and conduction losses. Also this balanced situation is inherited by the clamped diodes (D1, D2, D3 and D4) because their switches are the same than T1, T4, T5 and T8 respectively. Therefore, rates as MTTF, MTBF and reliability of the converter are improved.

IV. EXPERIMENTAL VERIFICATIONS

In order to prove all theoretical assumption the experimental investigation were carried out. The experimental prototype was deeply described in [17]. All tests were performed under 1.2 kW output power. Switching frequency was 100 kHz.

Figure 8 illustrates the gate-source switching signals of the first and second modulation techniques.

Figure 8(a) and Fig. 8(b) demonstrate the first modulation technique without and with shoot through correspondently. It is evident that all transistors are working in a different way. In all subfigures from up to down the switching signals of transistors correspond to T1, T2, T5 and T6. Figure 8(c) and Fig. 8(d) show the similar switching signals for second modulation techniques. In this case the switching signals of both branches are balanced.

Figure 9 shows the thermal pictures of the power board where driver circuits along with transistors terminals are located. Figure 8 demonstrates the gate resistors (R_G) of the transistors T1, T5 under first (a) and second (b) modulation strategies. Higher temperature of the gate resistors T5 confirms higher switching numbers of this transistor in the first modulation.

In case of second modulation technique branches are balanced from the point of view of switching signals and T_{on}.

Figure 10 illustrates the temperatures of the transistors chip that are located under the board on the radiators.

In the first case (Fig. 10(a)) difference between the temperatures of the difference branches is presented. This difference is mitigated under second modulation strategy (Fig. 10(b)).

It should be mentioned about total converter efficiency with different modulation strategies. This parameter was measured with YOKOGAWA DL850 V equipment. In the boost mode the efficiency was measured about 94,5 % for the first approach and 95 % for the second one. In case of buck operation the efficiency was around 97 % in both cases (Fig. 11) [17]. It is possible to conclude that the whole efficiency of the converter is practically the same (defined it as (P_{out}/P_{in}) by using both PWM techniques but, the stress of each branch is totally different, as thermic analysis and simulations have showed.

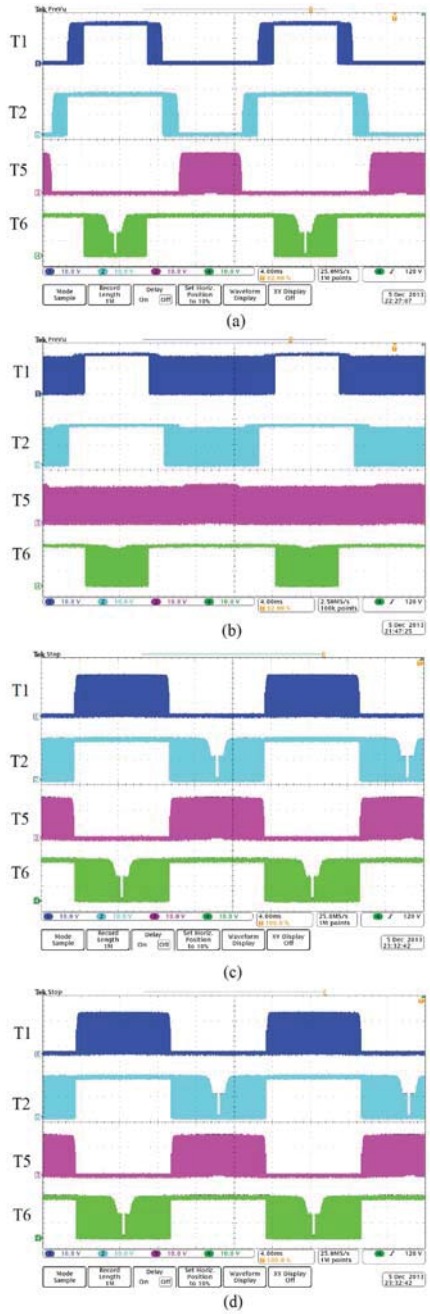

Fig. 8. Gate-source switching signals of the unbalanced (a, b) and balanced (c, d) modulation techniques without (a, c) and with (b, d) shoot-through generation.

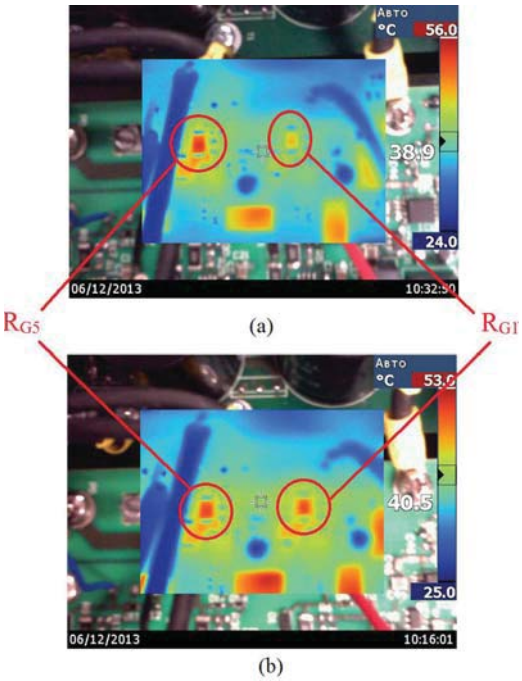

Fig. 9. Thermal picture of the gate resistors of the transistors T1, T5 under first (a) and second (b) modulation strategy.

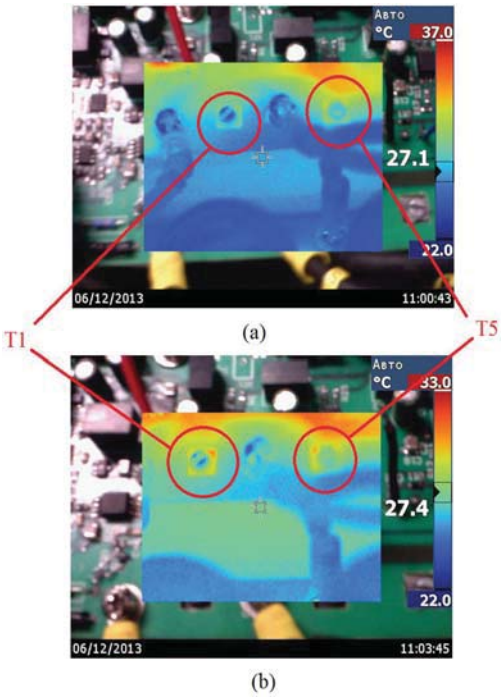

Fig. 10. Thermal picture of the chip transistors T1, T5 under first (a) and second (b) modulation strategy.

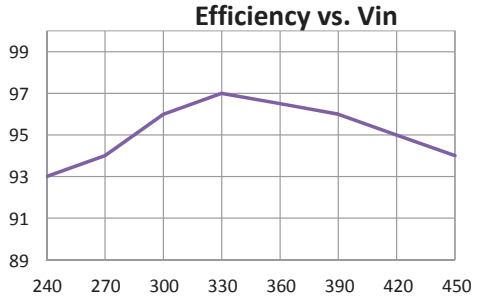

Fig. 11. Experimental measurements about efficiency versus input voltage.

V. CONCLUSIONS

This paper presents a new modified carrier based single phase modulation technique with maximum constant boost control for three level Z or qZ-source inverter topology.

The main advantage of the new proposed technique consists in equally distributed switching and conduction losses among two branches. Since the total converter efficiency remains approximately the same, the application of the two control strategies could be defined by thermal design of the converter.

Sometimes it is difficult to provide uniform heat sink for all transistors. It means that unbalanced thermal resistors for each transistor can be compensated by means of unbalanced modulation technique. And vice versa, balanced modulation technique is an appropriate control strategy for balanced thermal design.

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Voltage Distortion Approach for Output Filter Design for Off-Grid and Grid-Connected PWM Inverters

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Abstract

This paper proposes a novel voltage distortion approach for output filter design based on the voltage transfer function for both off-grid and grid-connected Pulse Width Modulation (PWM) Inverters. The method explained in detail is compared to conventional methods. A comparative analysis is performed on an example of L and LCL-filter design. Simulation and experimental results for the off-grid and the grid-connected single phase inverter prove our theoretical predictions. It was found that conventional methods define redundant values of the output filter elements. Assumptions and limitations of the proposed approach are also discussed.

Key words: Grid connection, Inverter, Output filter, Renewable sources control

I. INTRODUCTION

Recent years have seen heightened attention to the renewable energy. At the same time, the production cost of green energy is still high because of the high price of energy converters and other equipment. For instance, in the case of fuel cell or photovoltaic array, a DC-AC converter is required for the injection of renewable energy into the power distribution grid [Fig. 1(a)].

Traditionally, passive magnetic components required for boost capabilities and output filtering are very expensive and bulky.

Output filter is a substantial component of pulse width modulation (PWM) converters. Numerous papers cover the output filter design [1]-[26]. *L, LC, LCL* and *LLCL* output filters are commonly used in DC-AC converters.

L-filter is the simplest solution. Several design approaches with examples are described in [1]-[4]. The main drawbacks of the *L*-filter are its large size inductor and low output voltage quality in the open-loop control mode. Overall size can be reduced using an *LC* or *LCL*-output filter.

LC-filter is also a traditional solution [Fig. 1 (b)]. But it is mainly used in off-grid systems [5]-[9]. Moreover, any grid has its own internal inductance L_g [Fig. 1(a)], therefore an *LC*-filter cannot be considered for use in a grid-connected system as it is.

As compared to the first order *L*-filter, the *LCL*-filter [Fig. 1(c)] can satisfy the grid interconnection standards with a significantly smaller size and cost, but it might be more difficult to keep the system stable [10]-[24]. Another *LLCL* [Fig. 1(d)] solution was proposed in [25], [26]. In contrast to the *LCL*-filter, the *LLCL*-filter has nearly zero impedance at the switching frequency and can strongly attenuate the harmonic currents around the switching frequency. Here a precise value of the switching frequency is required.

To avoid stability problems in high order filters in the closed-loop control mode, damping methods are used. These methods are classified as passive or active. In the first case, generally, a resistor is added in series to the capacitor or in parallel to the grid inductor. The active damping method is based on the modification of the control system for resonance mitigation [18]-[21].

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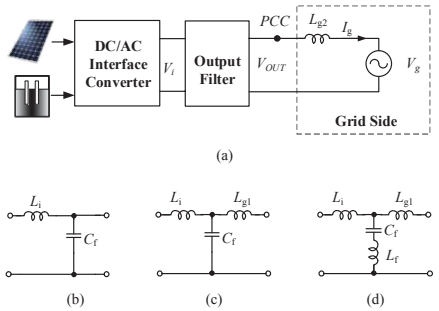


Fig. 1. Grid connected renewable energy system (a), *LC*-filter (b), *LCL*-filter (c), *LLCL*-filter (d).

The aim of this work is to find an optimal size of the output filter by means of a novel output voltage distortion approach and to compare it with other design approaches. In this paper, the output voltage distortion approach is proposed as a good solution for grid-connected as well as for off-grid systems.

II. Classical Approaches

This section presents existing output filter design approaches and those described in the literature. In general, most of them can be generalized as a current transfer function approach for grid- connected systems.

A. L-filter Design

There are several criteria for *L*-filter selection. For instance, the ripple criterion ensures that the error between the reference current and the grid injected current by the converter is within a margin.

Another criterion is based on the current ripple calculation on the switching harmonic. Fig. 2 shows a typical harmonic spectrum of the DC-AC inverter. It is possible to define the converter voltage harmonic at the switching frequency. Assuming that the current ripple is contributed only by the switching frequency, we can write:

$$THD_I \approx \sqrt{\frac{I_{SW}^2}{I_1^2}} = \frac{I_{SW}}{I_1}, \tag{1}$$

where I_{SW} is the grid RMS harmonic current at the switching frequency, I_1 is the RMS value of the current fundamental harmonic of the grid.

The current ripple passing from the converter side to the grid side can be computed upon consideration that at high frequencies, the converter is a harmonic generator, while the grid can be considered as a short circuit [2], [10], [12]. It is depicted in Fig. 3(a) and can be expressed as:

$$G_L(h_{SW}) = \frac{I_g(h_{SW})}{V_i(h_{SW})} = \left| \frac{-j}{w_1 \cdot h_{SW} \cdot (L_i + L_{g2})} \right|, \tag{2}$$

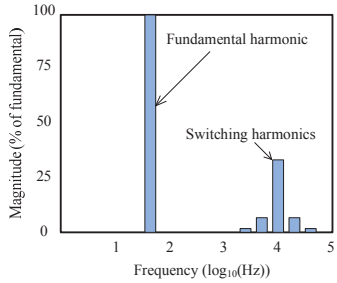


Fig. 2. Typical harmonic spectrum of the grid current.

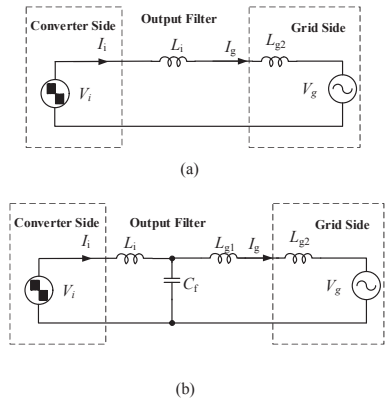


Fig. 3. Equivalent grid-connected converter with (a) L and (b) LCL output filter.

where h_{SW} – the number of switching harmonic, w_1 – fundamental harmonic, and total filter inductance $L_f = L_i + L_{g2}$.

From (2), the current ripple is defined:

$$I_{SW} = I_g(h_{SW}) = V_i(h_{SW}) \cdot \frac{1}{w_1 \cdot h_{SW} \cdot L_f}. \tag{3}$$

To estimate the inductance value it is necessary to define the harmonic component of the converter output voltage at the switching frequency $V_i(h_{SW})$. Resulting from Eqs. (2) and (3) and taking into account that the power factor is equal to 1:

$$L_f \geq \frac{V_i(h_{SW}) \cdot V_g}{w_1 \cdot h_{SW} \cdot P \cdot THD_I}, \tag{4}$$

where P is the rated output power.

In case the voltage harmonic component at the switching frequency is unknown, the current ripple can be estimated directly from the calculation using the inverter voltage waveform. Typically, such approach gives the same result, since there is a proportional dependence between the two magnitudes: ripple and content of harmonics [2], [3].

B. LCL-Filter Design

In this case the ripple attenuation passing from the converter side to the grid side can be computed on the basis of the previous assumption that at high frequencies, the converter is a harmonic generator, while the grid can be considered as a short circuit [Fig. 3(b)]:

$$G_{LCL}(h_{SW}) = \frac{I_g(h_{SW})}{V_i(h_{SW})} = \\ = \left| \frac{-j}{w_1 \cdot h_{SW} \cdot L_i - L_i \cdot L_g \cdot w_1^3 \cdot h_{SW}^3 \cdot C_f + w_1 \cdot h_{SW} \cdot L_g} \right|, \quad (5)$$

where we assume that $L_g = L_{g1} + L_{g2}$. From (5) the current ripple is defined:

$$I_{SW} = I_g(h_{SW}) = \\ = \left| \frac{V_i(h_{SW})}{w_1 \cdot h_{SW} \cdot L_i - L_i \cdot L_g \cdot w_1^3 \cdot h_{SW}^3 \cdot C_f + w_1 \cdot h_{SW} \cdot L_g} \right|. \quad (6)$$

To estimate the inductance value from this equation, it is necessary to define the harmonic component of the converter voltage at the switching frequency $V_i(h_{SW})$. As a result, based on Eqs. (1) and (6) we obtain:

$$THD_I = \frac{V_i(h_{SW}) \cdot V_g \cdot G_{LCL}(h_{SW})}{P}. \quad (7)$$

The resonance frequency f_{RES} in this case is defined as:

$$f_{RES} = \frac{1}{2\pi} \sqrt{\frac{L_g + L_i}{L_g \cdot L_i \cdot C_f}}. \quad (8)$$

Resonance frequency f_{RES} should be in a range between ten times the line frequency f_0 and one half of the switching frequency f_{SW} in order not to create resonance problems. Based on the aforementioned [10]-[12]:

$$10 \cdot f_0 \le f_{RES} \le \frac{f_{SW}}{2}. \quad (9)$$

We can determine L_g as a function of L_i, using the index r for the relation between the two inductances [11], [13].

$$L_g = r \cdot L_i. \quad (10)$$

Assuming that f_{RES} is determined, from Eq. (8) we can define the inductor from the inverter side:

$$L_i = \frac{1+r}{r} \cdot \frac{1}{4\pi^2 \cdot C_f f_{RES}^2} = \frac{1+r}{r} \cdot L, \quad (11)$$

where L is the weighted inductance value:

$$L = \frac{1}{4\pi^2 \cdot C_f f_{RES}^2}. \quad (12)$$

The capacitor value C_f is limited to decrease the capacitive reactive power at a rated load to less than the predetermined relative value Δ [26].

$$C_f \le \frac{\Delta \cdot P}{V_g^2 \cdot w_1}, \quad (13)$$

where P is the rated output power and V_g is the grid fundamental RMS voltage. The relatively small value of the reactive power is explained by additional losses in the system that it evokes. On the one hand, the larger value we choose the better filtering capability we obtain and on the other hand, the larger is the current stress on the semiconductors and passive elements.

Finally, from Eqs (7), (10) and (11) we obtain a relative index r of a quadratic equation.

$$r^2(L^2 w_1^2 h_{SW}^2 C_f - L) - (L^2 w_1^2 h_{SW}^2 C_f + L) + \\ + r(2L^2 w_1^2 h_{SW}^2 C_f - 2L - \frac{V_i(h_{SW}) \cdot V_g}{P \cdot THD_U w_1 h_{SW}}) = 0. \quad (14)$$

According to that approach, we can define the value of the capacitor, the weighted inductor and the index r, which provides a complete definition of the output filter.

It should be noted that the current ripple based approach is changed when the grid side current ripple is predefined. Once both the inverter side and the grid side current ripple are predefined, we can calculate the ripple difference and estimate the capacitor value. This approach is quite similar to the current transfer function approach and often used [10]-[12].

Paper [11] shows an example of an *LCL*-filter design for an active rectifier. The calculation of the converter side inductor is followed by the grid side inductor calculation based on the converter and grid current ripples respectively. The main difference is in the calculation of the resonance frequency, which cannot be predefined, but can be estimated after the capacitor calculation.

III. NOVEL VOLTAGE DISTORTION APPROACH

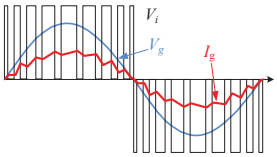
The main idea of the approach above is in the grid injected current in the nominal power point. At any moment of time the shape of the injected current is defined by the voltage difference between the inverter side and the grid side [Fig. 4(a)]. In the case of an ideal grid with negligibly low impedance, the voltage shape in point common coupling (PCC) has ideal sinusoidal voltage.

In the case of the off-grid mode with a passive load, the shape of the output voltage has fundamental harmonic and high frequency ripple similar to the output current shape [Fig. 4(b)].

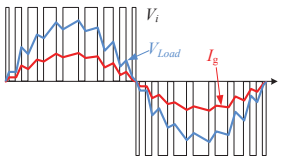
The result of the comparison of the approaches shows that the difference in the voltage applied to inductors is in the high frequency ripple. Assuming that high frequency ripple is relatively small and the output voltage on the resistor has pure sinusoidal shape, the current will be the same as in the case of the grid-connected inverter and we can use the voltage approach for the grid-connected system as well.

Resulting from the above considerations, we can represent the grid side like equivalent inductance in series with a passive resistor that corresponds to the nominal power [Fig. 4(c)].

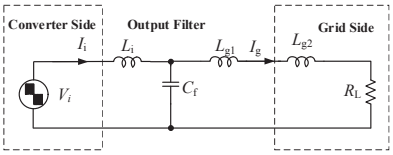
Since the output filter can be represented as the voltage transfer function in the case of predefined output voltage quality, we can define the parameters of the output filter.



(a)



(b)



(c)

Fig. 4. Voltage and current waveforms of the grid-connected system. (a) Islanding mode system. (b) Equivalent grid-connected converter. (c) Output filters at rated power.

Based on the above, the THD_U of the output voltage will be equal or higher than the THD_I of the grid injected current:

$$THD_U \geq THD_I \,. \tag{15}$$

In conclusion, in order to satisfy power quality demands in the full working range it is necessary to maintain THD_U in the preliminary specified range. The proposed approach differs from that described above by the voltage transfer function. A similar approach for the *LC*-filter calculation in the islanding mode was used in [7] with other optimality criteria.

A. L-filter Design

Taking into account the total inductance $L_f = L_i + L_{g2}$, the transfer function of the *L*-filter can be presented as:

$$K_L(s) = \frac{V_g(s)}{V_i(s)} = \frac{R_L}{R_L + s \cdot L_f} \,. \tag{16}$$

Regarding that the voltage distortion is defined only by the switching frequency, we can write that

$$THD_U \approx \sqrt{\frac{V_{SW}^2}{V_1^2}} = \frac{V_{SW}}{V_1} \,, \tag{17}$$

where V_{SW} is the voltage harmonic component of the converter at the switching frequency of the output voltage, V_1 is the fundamental harmonic. It can be defined from the transfer function at the switching frequency:

$$V_{SW} = K_L(h_{SW}) \cdot V_i(h_{SW}) \,, \tag{18}$$

where V_{SW} is the voltage harmonic component of the converter at the switching frequency of the output voltage, V_1 is the fundamental harmonic.

It can be defined from the transfer function at the switching frequency:

$$K_L(h_{SW}) = \frac{1}{\sqrt{1 + w_1^2 \cdot h_{SW}^2 \cdot \frac{L_f^2}{R_L^2}}} \,. \tag{19}$$

Resulting from Eqs. (17) and (18), we can write:

$$THD_U \geq \frac{K_L(h_{SW}) \cdot V_i(h_{SW})}{V_1} \,, \tag{20}$$

It should also be mentioned that the transfer function at the switching frequency depends on the equivalent load of the grid R_L. The maximum value K_{LC} corresponds to the maximum value of R_L.

Assuming $V_1 = V_g$, we can define the inductance value from Eqs. (19) and (20):

$$L_f \geq \frac{R_L \sqrt{V_i^2(h_{SW}) - V_g^2 \cdot THD_U^2}}{V_g \cdot THD_U \cdot w_1 \cdot h_{SW}} \,, \tag{21}$$

where R_L is the resistance that corresponds to the rated power.

B. LCL-filter Design

Neglecting the internal grid inductance L_{g2} and assuming $L_g = L_{g1}$ in Fig. 4 *b*, the transfer function of the *LCL*-filter can be obtained:

$$K_{LCL}(h_{SW}) = \frac{1}{\sqrt{(1 - w_1^2 h_{SW}^2 L_i C_f)^2 + (w_1 h_{SW} \frac{L_g}{R_L} - w_1^3 h_{SW}^3 C_f \frac{L_i L_g}{R_L})^2}} \,. \tag{22}$$

Similarly to the current transfer function design approach, we can determine L_g and L_i as a function of the weighted inductance L_i, using the index *r* for the relation between the two inductances. Finally, the relative index *r* of the fourth-order equation can be derived taking into account Eqs. (17) and (18).

$$K_{LCL}(h_{SW}) = = \frac{1}{(1 - w_1^2 h_{SW}^2 \frac{1+r}{r} \cdot L \cdot C_f) \sqrt{1 + w_1^2 h_{SW}^2 \frac{(1+r)^2 L^2}{R_L^2}}} \,. \tag{23}$$

As in the previous case, the only way to restrict the capacitor value is the injected reactive power defined by Eq. (13). Then, solving Eq. (23) using any appropriate tool, we can find index *r*. Next, from Eqs. (12), (10) and (11), we can determine L_g and L_i.

Finally, we can see the main difference of the voltage distortion approach in the last equation that defines the links

between the predefined input parameters, the capacitor, the resonance frequency and the index r.

It should also be noted that both approaches require the same set of the input parameters for output filter design. The only feature of the voltage distortion approach consists in the equivalent resistance R_L that corresponds to the rated power. It is obvious that if power is increasing, the quality of the output current is improving and the size of the output filter can be reduced. If power is not constant in the system, the output filter must be designed for the worst case. This is applicable to any renewable energy converter where the input power can vary in a very wide range.

Generally, in any grid-connected system, active or reactive power component injected to the grid does not influence the filter design approach. If the reactive power component is present, the full power must be considered and the equivalent resistance R_L will correspond to the full rated power. In the grid-connected inverter, the reactive power is controlled by means of phase shifting between the fundamental inverter voltage and the grid voltage, the voltage harmonic at the switching frequency will be the same.

In the case of the off-grid systems, only pure resistive load was considered. In the case of the capacitive load or any other impedance load, the reactive components must be considered as part of the filter. As a result, the current and the voltage transfer functions will be modified but the general idea of both approaches will be the same.

IV. Optimal Ratio Between Grid and Converter Inductances of *LCL*-Filter

The relative index r in Eq. (23) has several solutions. Relative solutions define the ratio between the grid side and the converter side inductances.

Let us assume that the total inductance $L_{Tot}=L_i+L_g$ is constant. From (10) and (11), we can express:

$$L_g = \frac{r}{1+r} \cdot L_{Tot}, \quad L_i = \frac{1}{1+r} \cdot L_{Tot}. \tag{24}$$

As a result, voltage and current transfer functions for high frequency ripples can be expressed as the function of r that has extreme points. In general, dependences for both approaches are represented in Fig. 5.

It can be seen that the function has minimum and maximum values. Minimum value r_{MIN} corresponds to the maximum attenuating factor of the high switching ripples. Mathematically we can obtain two maximum values that correspond to one resonance frequency. In order to find a certain quantity value of index r, which corresponds to the optimal solution, extreme points must be found:

$$\frac{d}{dr} G_{LCL}(r) = 0, \quad \frac{d}{dr} K_{LCL}(r) = 0. \tag{25}$$

Typically, this equation has several solutions, but it can be accepted only in a range $0<r\leq 1$. It means that the converter side has to be larger or equal to the grid side inductance. In the opposite case, huge current spikes in the semiconductors will be present.

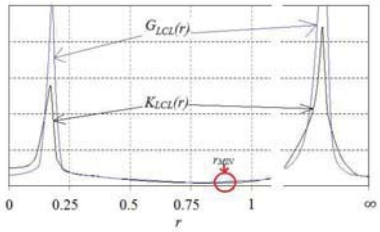


Fig. 5. Voltage and current transfer functions versus inductance ratio.

V. Comparative Evaluation of The Proposed Approaches

To compare different approaches, the calculation of the output filter for a case study system with different switching frequencies was carried out. A grid-connected system with a *1 kW* three-level (3L) inverter was chosen for simulation and experimental verification. The converter voltage harmonic component assumed at the switching frequency $V_i(h_{SW})$ in the 3L topology was about $0.45V_g$ (Fig. 2). It depends on the modulation index and pertains to the worst case. The RMS value of the grid voltage V_g is 230 V.

The current transfer function approach versus the voltage transfer approach is a subject of discussion in this section.

A. Classical Approach

According to the classical approach, the inductances for the L-filter can be calculated using expression (4). For instance, for the above mentioned parameters, $THD_I = 3\%$ and switching frequency of *25 kHz*:

$$L_f \geq \frac{0.45 \cdot 230^2}{2\pi \cdot 50 \cdot 500 \cdot 1000 \cdot 0.03} = 5.05\, mH. \tag{26}$$

For the *LCL*-filter design, the capacitor value C_f is limited by the capacitive reactive power at a rated load. Assuming that the capacitive reactive power is less than 2%, we can calculate from Eq. (13):

$$C_f \leq \frac{1\% \cdot P}{V_g^2 \cdot w_1} \leq \frac{1\% \cdot 1000}{230^2 \cdot 2\pi \cdot 50} \leq 0.6\,\mu F. \tag{27}$$

Once the capacitor is chosen, we can predefine the resonance frequency of the *LCL* output filter. According to Eq. (9), the resonance frequency must be in a range between ten times the line frequency f_0 and one half of the switching frequency f_{SW}. At the same time, the resonance frequency must be tuned in order to satisfy the $0<r\leq 1$ condition.

For instance, assuming $C_f = 0.47\,\mu F$, substituting Eq. (12), which defines the weighted inductance value L in Eq. (14) and solving Eq. (14) relative to the index r, we can obtain a certain

index r for any resonance frequency f_{RES}. If $r>1$ or there are no real solutions at all, then the resonance frequency must be changed in order to satisfy the $0<r\leq 1$ condition. After several iterations we obtain $r=0.97$ for $f_{RES}=10.2\ kHz$. It corresponds to the maximum resonance frequency within the condition $0<r\leq 1$.

Finally, taking into account the weighted inductance value L and Eqs. (11) and (10), we can define the values L_g and L_i:

$$L=\frac{1}{4\pi^2\cdot 0.47\cdot 10^{-6}\cdot 10200^2}=0.51\,mH\ , \quad (28)$$

$$L_i=\frac{1+0.97}{0.97}\cdot 0.51=1.1\,mH\ , \quad (29)$$

$$L_g=(1+0.97)\cdot 0.51=1.02\,mH\ . \quad (30)$$

Table I summarizes the results of the calculation. Similar calculations were performed for other switching and resonance frequencies.

B. Voltage Distortion Approach

An example of the L and LCL-filter calculation according to the proposed approach is discussed below.

Taking into account the switching frequency $25\ kHz$, and $R_L=53\ Ohms$ that corresponds to the nominal load ($1\ kW$), from Eq. (21) we obtain L_f:

$$L_f\geq\frac{53\sqrt{0.45^2\cdot 230^2-230^2\cdot 0.03^2}}{230\cdot 0.03\cdot 2\pi\cdot 50\cdot 500}=4.57\,mH\ . \quad (31)$$

It is evident that according to this approach, the inductance obtained was slightly smaller.

Let's consider the LCL-filter design according to the proposed approach.

First step is to estimate the capacitor value C_f is limited by the capacitive reactive power at a rated load and will be the same. Similarly to the classical approach, the next step is substituting Eq. (12), which defines the weighted inductance value L in Eq. (23) and solving Eq. (23) relative to the index r. We can obtain a certain index r for any resonance frequency f_{RES}. If $r>1$ or there are no real solutions at all, then the resonance frequency must be changed in order to satisfy the $0<r\leq 1$ condition.

By means of the iteration process solving Eq. (23) to estimate the maximum resonance frequency along with minimum values of the inductors in order to satisfy the $0<r\leq 1$ condition.

For instance, for the same parameters: $P=1\ kW$, $THD_U=3\%$ and the switching frequency $25\ kHz$, assuming $C_f=0.47\ \mu F$, we obtain $r=0.76$ for $f_{RES}=12.5\ kHz$.

Finally, we can calculate the weighted inductance L from Eq. (12) along with L_g and L_i. from Eqs. (10) and (11):

$$L=\frac{1}{4\pi^2\cdot 0.47\cdot 10^{-6}\cdot 12500^2}=0.34\,mH\ , \quad (32)$$

$$L_i=\frac{1+0.76}{0.76}\cdot 0.34=0.8\,mH\ , \quad (33)$$

$$L_g=0.76\cdot 0.8=0.61\,mH\ . \quad (34)$$

TABLE I
CALCULATED PARAMETERS OF THE OUTPUT FILTERS FOR 1 KW GRID-CONNECTED INVERTER

Approach	Switching Frequency, kHz	L	LCL			
		L_f, mH	L_i, mH	L_g, mH	C_f, μF	f_{RES}, kHz
Classical	25	5.05	1.1	1.02	0.47	10.2
			0.69	0.68	1	8.6
	50	2.52	0.36	0.35	0.47	17.4
			0.25	0.24	1	14.5
	100	1.26	0.13	0.12	0.47	29.5
			0.09	0.08	1	24.5
Voltage distortion	25	4.57	0.80	0.61	0.47	12.5
			0.58	0.23	1	12.5
	50	2.35	0.30	0.12	0.47	25
			0.16	0.05	1	25
	100	1.18	0.08	0.03	0.47	50
			0.04	0.01	1	50

We obtain $L_g=0.61\ mH$ and $L_i=0.8\ mH$. It is evident that the values obtained are smaller. First of all it is explained that the second approach can satisfy the $0<r\leq 1$ condition with a higher resonance frequency.

Increase of THD_U value leads decrease of the filter size. It should be noted that according to the proposed approach the output voltage distortion is counted. But assuming the difference in the applied inductor voltage negligibly small, we can use the obtained output filter parameters for the grid-connected inverter. As a result of the comparison, we can conclude that the presented values of the total inductance for the discussed types of the filter calculated by the voltage distortion approach are smaller. It is especially evident in the case of the LCL-filter.

VI. SIMULATION AND EXPERIMENTAL VERIFICATION

To compare the behavior of the inverter with the output filter parameters obtained, a PSIM simulation model of 1 kW 3L grid-connected inverter was tested.

The THD_I of the inverter output current is the main object of the investigation.

Table I represents the component values of L and LCL-filters calculated by different approaches with different switching frequencies. All the approaches must provide the predefined

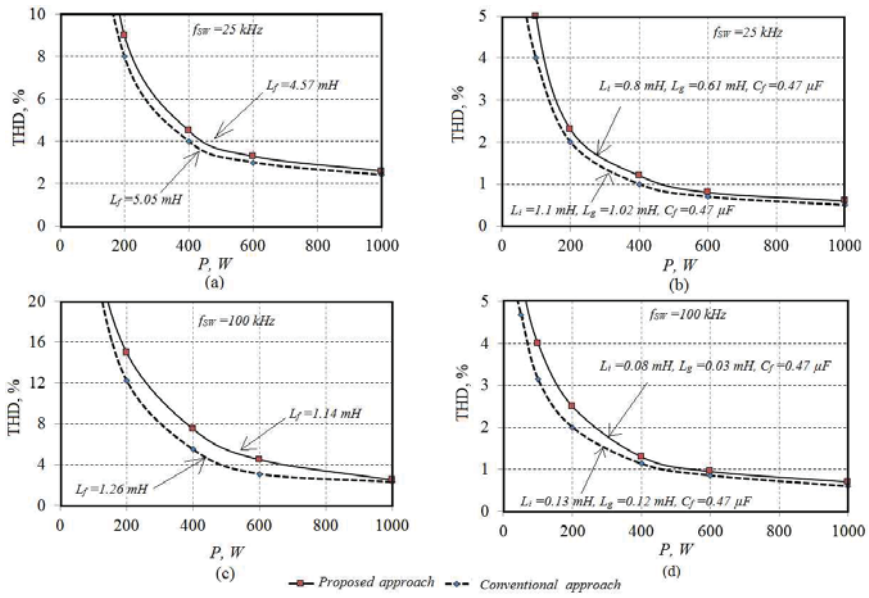


Fig. 6. THD_I versus output power. (a) *L*-filter with *25 kHz*. (b) *LCL*-filter with *25 kHz*. (c) *L*-filter with *100 kHz*. (d) *LCL*-filter with *100 kHz*.

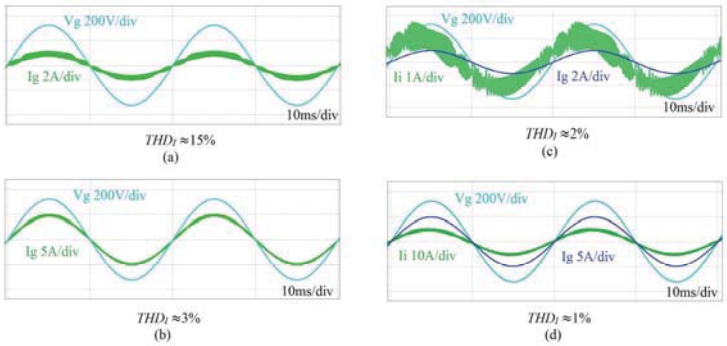


Fig. 7. Simulation results: (a) *L*-filter, 25 kHz, 160 W, *L*-filter, (b) 25 kHz, 800 W, *LCL*-filter, (c) 100 kHz, 160 W, (d) *LCL*-filter, 100 kHz, 800 W.

quality of the output current for nominal power. In order to verify this statement, several simulation and experimental tests were carried out. Fig. 6 shows the diagrams of dependences THD_I of the inverter output current versus the output power.

Fig. 6(a), 6(c) illustrate THD_I behavior of the grid-connected inverter with an *L*-filter. The upper figure corresponds to the *25 kHz*, the lower to the *100 kHz* switching frequency. The filter parameters are shown in the figure and in Table I.

It is evident that a slightly lower value of inductance leads to a slightly worse output current quality but still in the predefined range.

Fig. 6(b), 6(d) illustrates THD_I behavior of the *LCL*-filter. The upper figure corresponds to *25 kHz*, the lower to *100 kHz* of the switching frequency. The most interesting conclusion is that in despite of the significant difference in the inductance values, the difference in the output current quality is not so evident. Some difference can be seen at the low power points that are close to the idle mode. To distinguish current waveform differences, several simulation and experimental tests were performed. The simulation results are depicted in

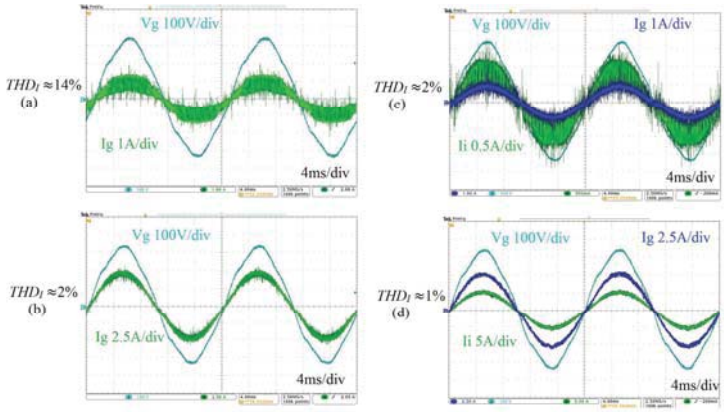


Fig. 8. Experimental results. (a) *L*-filter, 25 kHz, 160 W. (b) *L*-filter, 25 kHz, 800 W. (c) *LCL*-filter, 100 kHz, 160 W. (d) *LCL*-filter, 100 kHz, 800 W.

Fig. 7. The solid line corresponds to the voltage distortion approach while the dotted line to the conventional approach. Figs. 7(a), 7(b) illustrate the grid voltage and the output current of the inverterwith $L \approx 4.5\ mH$ and *25 kHz* switching frequency. Fig. 7(a) pertains to *160 W* output power, Fig. 7(b) to *800 W*. It can be concluded that the quality of the output current is close to that theoretically expected. The deterioration of the THD_I with the output power decreasing is in good agreement with the simulation results.

Similar diagrams are shown in Fig. 7(c) and 7(d) for the *LCL*-filter: $L_i = 0.54\ mH$, $L_g = 0.2\ mH$, $C_f = 0.47\mu F$ and the switching frequency *100 kHz*.

Quality analysis confirms our theoretical expectations. Despite the high current ripple in the converter side inductor due to the presence of the capacitor, the output current has low ripple. Fig. 7(c) as in the previous case pertains to *160 W* output power, Fig. 7(d) to *800 W*. This filter was preliminarily calculated by the voltage distortion approach for the *100 W* nominal power and can provide satisfactory output current quality in a wide range.

Fig. 8 shows that the experimental results are similar to the simulation results presented in Fig. 7 but in the off-grid mode with an active load. Ignoring noise in the measured signals, we can regard the waveforms in good agreement with the simulation results. THD_I calculated by an oscilloscope is slightly less than that obtained in the simulation, because according to the standard only 40 harmonics are counted.

VII. Conclusions

This paper presents a detailed output filter design of any off-grid or grid-connected inverter by means of comparative analyses of different design approaches. Several traditional approaches were discussed. Current ripple along with the current transfer function approaches are used for the *L* and *LCL*-filter design.

Among classical approaches, the voltage distortion approach based on the voltage transfer function was proposed for off-grid as well as for grid-connected inverters. Finally, the bulky analytical expressions derived allow the lowest output filter size for the *L* and *LCL*-filter to be obtained. The simulation and experimental results confirmed that conventional methods define the redundant value of the output filter elements. Such difference is connected with our assumptions done during the analysis. In the case of the current transfer function approach, the grid is considered like a short circuit and as a result, full inverter side high switching voltage is applied to the output filter. In fact, this is not the case here. At the same time, by the voltage distortion approach we can reach worse but closer to the predefined output current quality. Bulky equations for the voltage distortion approach could be easily implemented as custom software for practical engineers.

It should be mentioned that the smallest size of the output *LCL*-filter has an opposite side like higher resonance frequency that reduces the possible switching frequency range. Both the stability issue during the tuning process of the closed-loop control system and the type of the control system that strongly depends on the operating mode of the converter should be taken into account. Also, the internal grid inductance must be negligibly low. In the opposite side, the grid voltage waveform cannot be considered as ideal sinusoidal voltage that was assumed in the proposed approach.

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Single phase three-level neutral-point-clamped quasi-Z-source inverter

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Abstract: This study presents a novel three-level neutral-point-clamped quasi-Z-source inverter in the single-stage buck-boost multilevel inverter family. The topology was derived by combining the properties of the quasi-Z-source network with those of a three-level neutral point clamped inverter. It features such advantages as low voltage stress of the switches, single-stage buck-boost power conversion, continuous input current, short-circuit withstandability and low total harmonic distortion of the output voltage and current. The authors present a steady state analysis of the topology along with a special modulation technique to distribute shoot-through states during the whole fundamental period. Component design guidelines for a single-phase case study system are described. All the findings have been confirmed by simulations and experiments. The topology could be recommended for applications requiring continuous input current, high input voltage gain and enhanced quality of the output voltage.

1 Introduction

Three-level inverters have attracted increasing attention in industrial applications, such as motor drives [1, 2], active filters [3, 4] and renewable energy systems [5]. The major advantage of multilevel inverters over the traditional two-level voltage source inverters (VSIs) is the stepwise output voltage [1–7]. The result is higher power quality, better electromagnetic compatibility, lower switching losses and absence of need for a transformer at the distribution voltage level [7, 8].

The three-level neutral-point-clamped (3L NPC) inverter has many advantages over the two-level VSI : twice lower semi-conductor voltage stress, higher switching frequency because of lower switching losses, decreased dv/dt and better harmonic performance. However, the 3L NPC can perform only the voltage buck function. It means that the AC peak output voltage cannot exceed the DC-link voltage and the DC-link voltage has to be higher than the AC peak output voltage. The shoot-through problem, which could be caused by misgating because of electromagnetic interference, is an issue related to the reliability of a converter. Thus, the dead time to block the cross conduction of the upper and lower switches has to be provided in the VSI, which causes the waveform distortion.

Voltage boost operation requires an additional DC/DC boost converter in the input stage, which makes the overall system more costly and harder to control. At the same time, the Z-source inverter (ZSI) proposed in [9] overcomes the limitations and problems of the traditional VSIs. Such a topology provides the boost function with the inherent short-circuit immunity [10, 11]. The quasi-Z-source inverters (qZSIs) proposed in [12–17] enable further improvements of the traditional ZSIs. Besides the advantages inherited from the ZSIs [18], the qZSIs have such merits as reduced passive component ratings, continuous input current and a common DC rail between the source and the inverter. qZSIs suit very well for renewable energy systems [19–23] because of excellent performance and availability of all the requirements, in particular for the photovoltaic (PV) systems. These inverters are capable of performing maximum power point tracking (MPPT) and inversion with no need for an extra DC/DC converter. Furthermore, continuous input current makes them especially suitable for fuel cell applications [16].

The single-stage buck-boost multilevel inverter was proposed in 2006 as the logical extension of the two-level ZSI [24]. In contrast to the traditional NPC inverter, the inverter in Fig. 1*a* uses two isolated DC sources and two separate Z-source networks for boosting its input voltage to a higher DC-link voltage level. To decrease the number of passive components, the Z-source NPC inverter with a single impedance network was proposed in [2]. However, this topology must also be fed from two DC sources. By the introduction of the high-frequency transformer and two additional capacitors (Fig. 1*c*), the Z-source NPC inverter with a single impedance network could be supplied from a single DC source [25]. Moreover, by a transformer with the

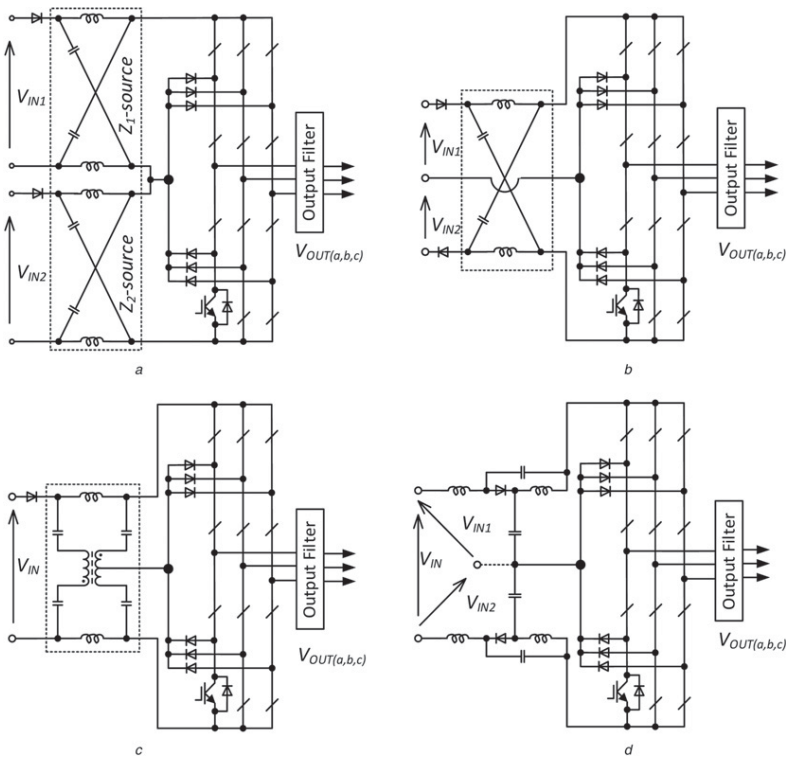

Fig. 1 *3L NPC single-stage buck-boost inverters*

a Z-source NPC inverter with two impedance networks and two DC sources
b Z-source NPC inverter with a single impedance network and two DC sources
c Z-source NPC inverter with a single impedance network and a single DC source
d New proposed quasi-Z-source NPC inverter

turns ratio different from 1:1, an input voltage gain higher than with the traditional Z-source network could be achieved. From the practical point of view, the topologies shown in Figs. 1*a*–*c* have one common drawback – the discontinuous input current during the boost conversion mode could have negative influence on the input voltage source, especially in renewable energy applications.

This paper presents a novel three-level neutral-point-clamped quasi-Z-source inverter (3L NPC qZSI). The solution depicted in Fig. 1*d* is intended for applications that require continuous input current. The main idea is to combine two symmetrical qZS networks. As a result, along with continuous input current, it combines a wide input voltage operation range and shoot-through immunity. The twice lower voltage stress on the semi-conductors allows fast MOSFETs to be used, which leads to high switching frequency and better power density. Moreover, the power source can be single or separated by means of a neutral point. A generalised comparison of the

Table 1 Generalised properties of the single-stage buck-boost multilevel inverter family

	Z-source NPC inverter with two impedance networks (Fig. 1*a*)	Z-source NPC inverter with a single impedance network (Fig. 1*b*)	Z-source NPC inverter with a single impedance network (Fig. 1*c*)	Quasi-Z-source NPC inverter (Fig. 1*d*)
continuous input current in CCM	NO	NO	NO	YES
operation possibility with a single DC source	NO	NO	YES	YES
operation possibility with multiple DC sources	YES	YES	NO	YES

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properties of the single-stage buck-boost multilevel inverter family members is presented in Table 1.

Section 2 describes in detail the operation principle with a steady state analysis. Section 3 introduces a special single phase modulation technique developed to distribute shoot-through states during the whole fundamental period; Section 4 presents guidelines for component design for a single phase case study under continuous conduction mode (CCM). Sections 5 and 6 describe the simulation and experimental studies to validate theoretical predictions. The main advantages of the new topology are emphasised and a possible field of application is proposed in the Conclusions.

2 Operation principle of 3L NPC qZSI

This section explains the operation principle of the system of a single-phase 3 L NPC qZSI (Fig. 2) consisting of two complementary transistor pairs for every leg and four clamping diodes. Two identical qZS-networks have a common node between the capacitors C_2 and C_3, forming the neutral point of the topology. Typically, two kinds of modulation strategies could be used for operating a 3L NPC qZSI: using a switching frequency equal to the output frequency or using a PWM strategy with a sinusoidal modulation signal and four different high frequency carrier signals.

The output voltage of the inverter has five different levels: $0, \pm B\cdot(V_{\rm IN}/2)$ and $\pm B\cdot V_{\rm IN}$ in the negative and positive directions, where B is the boost factor of the inverter defined as $B = V_{\rm DC}/V_{\rm IN}$. The fundamental period of the proposed 3L NPC qZSI in the CCM can be divided into eight time intervals. Table 2 shows the switching states of the transistors for each time interval. All the switching states are separated into three modes: active state, zero state and shoot-through state that can be applied within the zero state. Active states are divided into six submodes. States 3 and 5 correspond to the level $-B\cdot(V_{\rm IN}/2)$, states 6 and 8 to $+B\cdot(V_{\rm IN}/2)$.

To estimate the component values, we performed the steady state analysis by means of voltage balance across the inductors and current balance across the capacitors. It means that the average voltage across the inductors and the average current across the capacitors are equal to zero:

$$\frac{1}{T}\int v_{L1}(t)\mathrm{d}t = 0, \quad \frac{1}{T}\int i_{C1}(t)\mathrm{d}t = 0$$

Table 2 Switching states of transistors in 3L NPC qZSI

	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
1	0	1	1	0	0	1	1	0
2	1	1	1	1	1	1	1	1
3	1	1	0	0	0	0	1	0
4	1	1	0	0	0	0	1	1
5	0	1	0	0	0	0	1	1
6	0	0	1	0	1	1	0	0
7	0	0	1	1	1	1	0	0
8	0	0	1	1	0	1	0	0

The converter switching period in the CCM is expressed as

$$\frac{t_{\rm A}}{T} + \frac{t_{\rm Z}}{T} + \frac{t_{\rm S}}{T} = D_{\rm A} + D_{\rm Z} + D_{\rm S} = 1 \tag{1}$$

where $D_{\rm A}$ is the duty cycle of the active state, $D_{\rm Z}$ is the duty cycle of the zero state and $D_{\rm S}$ is the duty cycle of the shoot-through state.

The sum of the capacitor voltages defines the peak value of the DC-link voltage:

$$\mathrm{V}_{\rm DC} = \mathrm{V}_{C1} + \mathrm{V}_{C2} + \mathrm{V}_{C3} + \mathrm{V}_{C4} \tag{2}$$

where V_{C1}, V_{C2}, V_{C3}, V_{C4} are the average voltages across the capacitors over one fundamental period.

Taking into account that the qZS network is symmetrical, we obtain

$$L_1 = L_3, \quad L_2 = L_4 \tag{3}$$

$$C_1 = C_4, \quad C_2 = C_3 \tag{4}$$

Correspondingly, the voltages are

$$v_{L1} = v_{L3}, \quad v_{L2} = v_{L4} \tag{5}$$

$$V_{C1} = V_{C4}, \quad V_{C2} = V_{C3} \tag{6}$$

The capacitor voltages can be found from the voltage balance

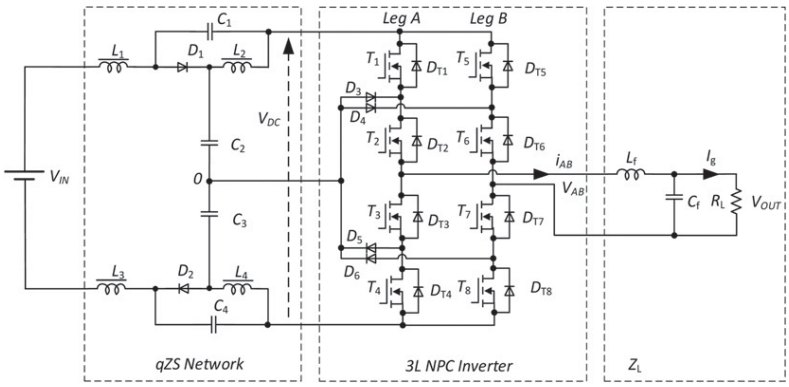

Fig. 2 *New proposed quasi-Z-source NPC inverter: single phase case study system*

across the inductors:

$$V_{L1} = \frac{1}{T}\int v_{L1}(t)\mathrm{d}t = \frac{1}{T}\left(\left(V_{C2} - \frac{V_{\mathrm{IN}}}{2}\right)t_A - \left(V_{C1} + \frac{V_{\mathrm{IN}}}{2}\right)t_{\mathrm{S}}\right) = \left(V_{C2} - \frac{V_{\mathrm{IN}}}{2}\right)D_{\mathrm{A}} - \left(V_{C1} + \frac{V_{\mathrm{IN}}}{2}\right)D_{\mathrm{S}} = 0 \quad (7)$$

$$V_{L2} = \frac{1}{T}\int v_{L2}(t)\mathrm{d}t = \frac{1}{T}(V_{C1}\cdot t_{\mathrm{A}} - V_{C2}\cdot t_{\mathrm{S}}) = V_{C1}\cdot D_{\mathrm{A}} - V_{C2}\cdot D_{\mathrm{S}} = 0 \quad (8)$$

Taking into account the conditions presented above, we obtain the voltages across the capacitors:

$$V_{C1} = V_{C4} = \frac{D_{\mathrm{S}}\cdot V_{\mathrm{IN}}}{2 - 4\cdot D_{\mathrm{S}}} \quad (9)$$

$$V_{C2} = V_{C3} = \frac{V_{\mathrm{IN}}\cdot(1 - D_{\mathrm{S}})}{2 - 4\cdot D_{\mathrm{S}}} \quad (10)$$

The final equation for the boost factor can be expressed as follows:

$$B = \frac{V_{\mathrm{DC}}}{V_{\mathrm{IN}}} = \frac{V_{C1} + V_{C2} + V_{C3} + V_{C4}}{V_{\mathrm{IN}}} = \frac{1}{1 - 2\cdot D_{\mathrm{S}}} \quad (11)$$

3 Special single phase modulation technique

Several modulation techniques could be applied in the 3L NPC qZSI topology [2, 10, 24–29]. In the previous section, the fundamental frequency modulation was considered to explain the operation principle of the proposed topology. In this section, we present a special pulse width modulation (PWM) technique to distribute the shoot-through states during the whole fundamental period.

Typically, the PWM technique uses a sinusoidal modulation signal and four high frequency carrier waveforms (Fig. 3*a*). As in all the modulation techniques, the shoot-through states must be located within the zero state ($V_{AB} = 0$) that maintains constant and normalised average voltage during the switching period.

In the classical PWM technique (Fig. 3*b*) applied in the 3L NPC qZSI, zero states are located in a fraction of the fundamental period. Shoot-through states are placed during the intervals t_0–t_1, t_2–t_3 and t_4–t_5. This technique produces a concentration of the shoot-through states that could result in such problems as higher ripple of the input current and possible capacitor voltage disbalance.

To eliminate or mitigate the effects produced by the concentration of shoot-through states, a variation of the typical PWM technique was proposed in [30] (Fig. 3*c*). Its main objective is to distribute the shoot-through states over the whole fundamental period of the inverter.

Two cases were considered to illustrate the operation of the proposed modulation technique. With no shoot-through generation ($D_{\mathrm{S}} = 0$), the operation is equal to the typical PWM VSI operation where four triangular carriers and one modulating wave are compared with obtain the states of the transistors. T_1, T_2 and T_5, T_6 as well as T_3, T_4 and T_7, T_8 have the complementary states, respectively.

In the next case (Fig. 3*c*), the carrier signal level is modified to include the shoot-through states. *Carrier*$_1$ includes a constant value with the desired D_{S} and generates the shoot-through states with the constant pulse width. As a result, uniformly distributed generation of the shoot-through states is achieved.

Equally distributed shoot-through generation partially replaces the half DC-link voltage in the output inverter voltage V_{AB}. To compensate this replacement of the average voltage V_{AB}, the second leg B (T_5, T_6, T_7 and T_8) changes the voltage V_{B0}. Fig. 3*c* illustrates this compensation (solid lines). During the positive half-cycle, leg B produces $V_{B0} = -V_{DC}/2$ more times, restoring the average voltage V_{AB}. This is achieved by means of the *carrier*$_4$ displacement, which generates the switching of T_6. During the negative half-cycle, a similar approach was applied. Leg B produces $V_{B0} = +V_{DC}/2$ more times, restoring the average voltage V_{AB}. This was achieved by means of the *carrier*$_3$ displacement, which controls the switching of T_5.

Figs. 3*a*–*c* show schematically the resulting switching signals of transistors T_1, T_2, T_5 and T_6 and shoot-through states. The lower part of Fig. 3 illustrates the waveform of the inverter output voltage without and with the shoot-through using the conventional and the modified modulation techniques and the frequency modulation index equal to 10.

3.1 Boost regulation capability

The modulation technique proposed reaches the desired input voltage boost by means of equally distributed shoot-through states with a constant width. The qZS-network works at the maximum switching frequency. It is illustrated in Fig. 3*c*.

Further, we have to take into account here that the modulation index M has its upper limit:

$$M \le 1 - D_{\mathrm{S}} \quad (12)$$

At the same time, the results of the steady state analysis are applicable in this modulation technique. Finally, we can obtain the expression for the RMS value of the sinusoidal output voltage V_{OUT}:

$$V_{\mathrm{OUT}} = \frac{1}{\sqrt{2}}M\cdot B\cdot V_{\mathrm{IN}} = \frac{1 - D_{\mathrm{S}}}{\sqrt{2}\cdot(1 - 2\cdot D_{\mathrm{S}})}\cdot V_{\mathrm{IN}} \quad (13)$$

To distinguish the DC-link boost factor and the output voltage, we introduce the notation of the gain factor G:

$$G = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{1}{\sqrt{2}}\cdot M\cdot B\cdot V_{\mathrm{IN}} = \frac{1 - D_{\mathrm{S}}}{\sqrt{2}\cdot(1 - 2\cdot D_{\mathrm{S}})} \quad (14)$$

Theoretically, a converter has endless input voltage regulation capabilities. In practice, the maximum blocking voltage of the semi-conductors limits the upper limit of the input voltage and losses limit the lower voltages.

4 General design guidelines

4.1 Dimensioning of passive components

In a desired case, the currents through the inductors along with the DC-link voltage must be constant. The voltages

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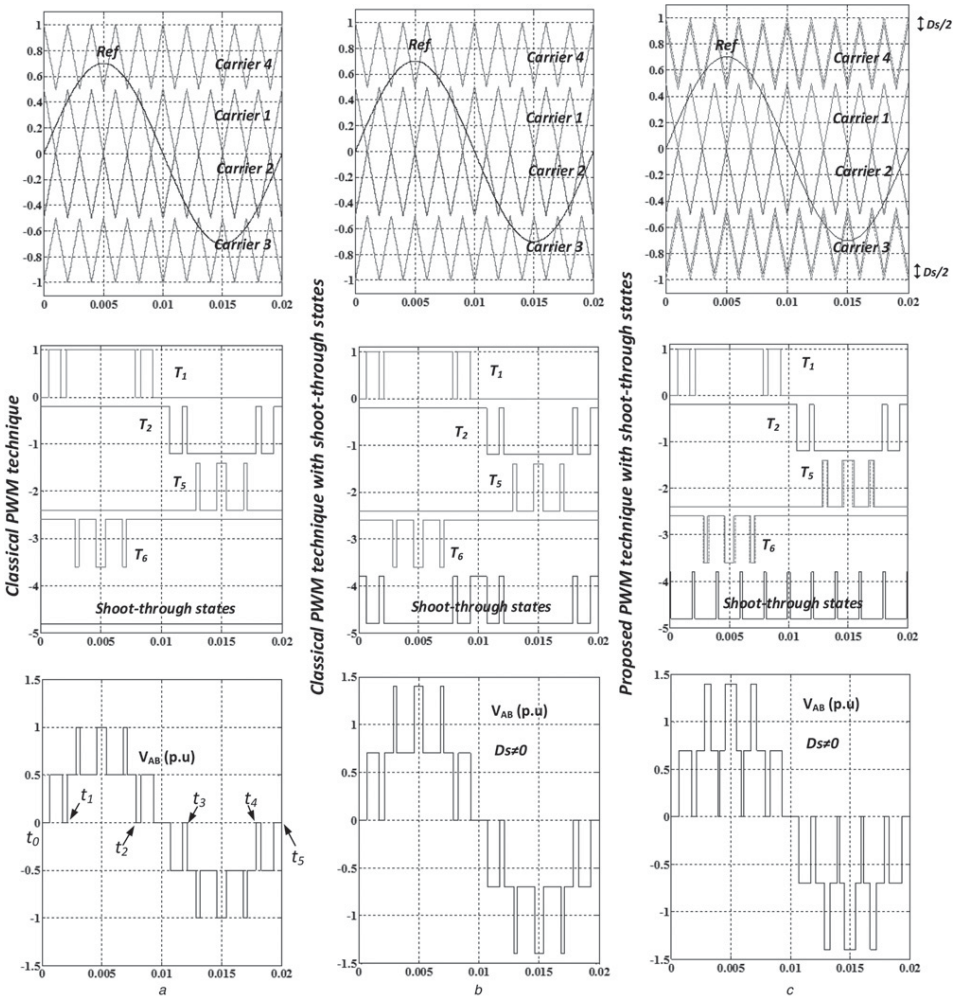

Fig. 3 *Sketch of the special modulation technique*

a Classical modulation technique
b Classical modulation technique with the shoot-through states
c Proposed modulation technique with the shoot-through states

across the capacitors must be calculated according to (9) and (10). The average inductor current is equal to the input current. The main problem lies in the low and high switching frequency ripples. The DC-link voltage and the input current have low frequency fluctuations (100 Hz) evoked by the instantaneous value of the output power (Fig. 4*a*). The high frequency ripples are mostly caused by the high frequency generation of the shoot-through states (Fig. 4*b*).

These fluctuations result in higher losses. Thus, special attention should be paid to the dimensioning of passive components. The abovementioned passive components will lead to the transition from the CCM to the discontinuous conduction mode (DCM). The aim here is to define the boundary between the CCM and the DCM operation in a single phase system.

Several approaches can be used. From the theoretical point of view, it is most appropriate to solve the difference equations for the full cycle. This method can give direct analytical expressions for the element calculation. At the same time, from the practical standpoint, the method seems useless because of the complexity of the final expressions.

In a simplified approach, high switching frequency is neglected to estimate low frequency ripples. In this case, the output current is represented as an ideal AC current source equal to the fundamental harmonic of the DC-link

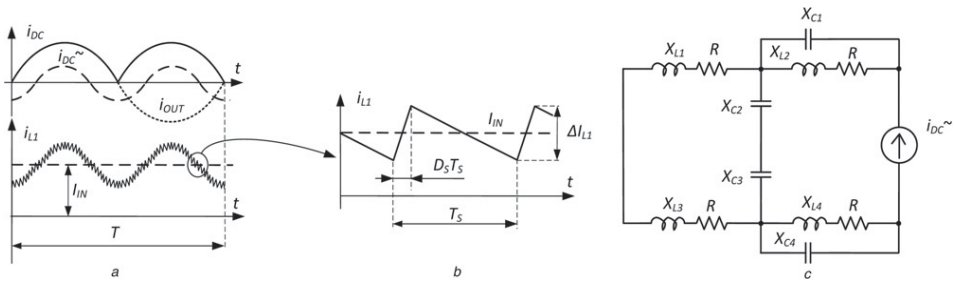

Fig. 4 *Generalised operating waveforms*
(a, b) Along with an equivalent scheme
(c) Proposed converter in the CCM

current (Fig. 4*a*).

$$i_{DC\sim} = I_{DC\_Max} \cdot \sin\left(4\pi \cdot \frac{1}{T} \cdot t - \frac{\pi}{2}\right) = \frac{\sqrt{2} \cdot 4}{3 \cdot \pi} \cdot \frac{P_{OUT}}{V_{OUT}} \cdot \sin\left(4\pi \cdot \frac{1}{T} \cdot t - \frac{\pi}{2}\right) \quad (15)$$

where P_{OUT} is the output power of the inverter.

Assuming that the CCM is achieved and the qZS-network is symmetrical, we can represent the converter behaviour by a simple equivalent circuit (Fig. 4*c*) for an AC component. A similar approach was used in [31] except that low frequency fluctuations in the inductors were not considered. It is relevant if $|X_C| \ll |X_L|$, where X_C is the capacitor reactance and X_L is the inductive reactance. In a more general case, in the conditions above, we can define the AC component of the input current

$$i_{L1\sim} = I_{DC\_Max} \cdot \sin\left(4\pi \cdot \frac{1}{T} \cdot t - \frac{\pi}{2}\right) \cdot \left|\frac{X_{C2}}{X_{C2} + X_{L1} + R}\right| = \frac{\sqrt{2} \cdot 4 \cdot P_{OUT} \cdot T^2 \cdot \sin(4\pi \cdot (1/T) \cdot t - (\pi/2))}{3 \cdot \pi \cdot V_{OUT} \sqrt{16\pi^2 \cdot C_2^2 \cdot R^2 + (16\pi^2 \cdot C_2 \cdot L_1 - T^2)^2}} \quad (16)$$

where R is the parasitic resistor of the inductor.

The average input current is obtained by means of power balance where we assume that the output power P_{OUT} is approximately equal to the input power P_{IN}:

$$P_{IN} = V_{IN} \cdot I_{IN} \simeq P_{OUT} \quad (17)$$

Taking into account power balance and (16), low frequency input current ripple factor K_{LL1} can be calculated as

$$K_{LL1} = \frac{\hat{i}_{L1\sim}}{I_{IN}} \simeq \frac{\hat{i}_{L1\sim} \cdot V_{IN}}{P_{OUT}} \simeq \frac{8(1 - 2 \cdot D_S) \cdot T^2}{3\pi(1 - D_S)\sqrt{16\pi^2 \cdot C_2^2 \cdot R^2 + (16\pi^2 \cdot C_2 \cdot L_1 - T^2)^2}} \quad (18)$$

The AC voltage component of the capacitors can be expressed similarly

$$v_{C1} \sim = i_{DC\sim} \cdot \left|\frac{(X_{L2} + R) \cdot X_{C1}}{X_{C1} + X_{L2} + R}\right| = i_{DC\sim} \cdot \frac{(4\pi \cdot T \cdot L_2 + R \cdot T^2)}{\sqrt{16\pi^2 \cdot C_1^2 \cdot R^2 + (16\pi^2 \cdot C_1 \cdot L_2 - T^2)^2}} \quad (19)$$

Low frequency voltage ripple factor K_{CL1} for capacitors C_1 and C_4 can be obtained from (9) and (19):

$$K_{CL1} = \frac{\hat{v}_{C1\sim}}{V_{C1}} = \frac{8P_{OUT} \cdot (1 - D_S) \cdot (4\pi \cdot T \cdot L_2 + R \cdot T^2)}{3\pi \cdot V_{OUT}^2 D_S \sqrt{16\pi^2 \cdot C_1^2 \cdot R^2 + (16\pi^2 \cdot C_1 \cdot L_2 - T^2)^2}} \quad (20)$$

Voltage ripple factor for capacitors C_2 and C_3 as well as the current ripple factor for inductors L_2 and L_4 can be derived in a similar way. The final expressions are as follows:

$$K_{LL2} = \frac{i_{L2\sim}}{I_{IN}} \simeq \frac{8(1 - 2 \cdot D_S) \cdot T^2}{3\pi(1 - D_S)\sqrt{16\pi^2 \cdot C_1^2 \cdot R^2 + (16\pi^2 \cdot C_1 \cdot L_2 - T^2)^2}} \quad (21)$$

$$K_{CL2} = \frac{v_{C2\sim}}{V_{C2}} = \frac{8 \cdot P_{OUT} \cdot (4\pi \cdot T \cdot L_1 + R \cdot T^2)}{3\pi \cdot V_{OUT}^2 \cdot \sqrt{16\pi^2 \cdot C_2^2 \cdot R^2 + (16\pi^2 \cdot C_2 \cdot L_1 - T^2)^2}} \quad (22)$$

It is evident that we can calculate the values of the passive components from (18), (20)–(22) taking into account the predefined low frequency ripples of the voltage and the current. Finally, we can conclude that the current and voltage ripples strongly depend on the shoot-through duty

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Table 3 Voltage and current stress on the semi-conductors

Semi-conductor	Voltage stress (maximum value), p.u.	Current stress (average value), p.u.
D_1, D_2	$\frac{1}{\sqrt{2}\cdot(1-D_S)}$	$\frac{(1-D_S)}{\sqrt{2}\cdot(1-2\cdot D_S)}$
$D_3 \ldots D_6$	$\frac{1}{\sqrt{2}\cdot(1-D_S)}$	0.25
$T_1 \ldots T_8$	$\frac{1}{\sqrt{2}\cdot(1-D_S)}$	1.4

cycle and on the ohmic losses in the inductors of the qZS-networks.

High frequency generation of the shoot-through states causes high frequency ripples, as illustrated in Fig. 4*b*. In the case of negligibly low current bias caused by low frequency ripples (accepted for one switching cycle), we can claim that high frequency ripples of the input current can be estimated from the shoot-through duration:

$$\Delta I_{L1} = \int_0^{T_S\cdot D_S} \frac{\mathrm{d}i_{L1}}{\mathrm{d}t}\cdot \mathrm{d}t = \int_0^{T_S\cdot D_S}\left(\frac{V_{\mathrm{IN}}+V_{C1}+V_{C4}}{2\cdot L_1}\right)\cdot \mathrm{d}t = \left(\frac{V_{\mathrm{IN}}+V_{C1}+V_{C4}}{2\cdot L_1}\right)\cdot T_{\mathrm{S}}\cdot D_{\mathrm{S}} \tag{23}$$

where T_S is the switching period.

We can express the high switching frequency current ripple factor K_{LH1} as

$$K_{LH1} = \frac{\Delta I_{L1}}{2\cdot I_{\mathrm{IN}}} \simeq \frac{V_{\mathrm{OUT}}^2\cdot(1-2\cdot D_{\mathrm{S}})}{2\cdot(1-D_{\mathrm{S}})\cdot L_1\cdot P_{\mathrm{OUT}}} T_{\mathrm{S}}\cdot D_{\mathrm{S}} \tag{24}$$

and finally, we obtain

$$L_1 \geq \frac{V_{\mathrm{OUT}}^2\cdot(1-2\cdot D_{\mathrm{S}})}{2\cdot(1-D_{\mathrm{S}})\cdot K_{LH1}\cdot P_{\mathrm{OUT}}} T_{\mathrm{S}}\cdot D_{\mathrm{S}} \tag{25}$$

From the last equations we can estimate the minimum inductance value to maintain high switching frequency ripples in the input current that is a condition of the CCM operation. The sum of low and high frequency input current ripples should be smaller than the average input current I_{IN}.

4.2 Dimensioning of semi-conductors

Traditionally, the voltage and current stresses are the key parameters for the dimensioning of semi-conductors. Table 3 shows the voltage and current stresses of semi-conductors in terms of relative units. It was assumed that 1 p.u. current rating corresponds to the RMS value of the output current and one p.u. voltage rating corresponds to the RMS value of the output voltage.

It should be noted that all the values are represented assuming an ideal dynamic performance of semi-conductors, which is to be considered in component selection. It is evident that the voltage stress on all the semi-conductors in the 3L NPC qZSI topology is twice lower than in the traditional VSI. Reduced voltage stress on the semi-conductors allows using high switching frequency MOSFETs.

5 Simulation results

To verify the abovementioned analytical predictions, simulations by help of PSIM were performed. Fig. 5 illustrates several tests validating (18)–(25). These equations define dependences between high and low frequency ripple factors against passive component values and the shoot-through duty cycle. Fig. 5*a* illustrates the high and low switching frequency ripple factor of the input current as a function of the shoot-through duty cycle. All the other parameters, including switching frequency 100 kHz, were constant. We can see an exact match at the high frequency ripple factor K_{LH1}. It is obvious that the theoretical value of the low frequency ripple factor K_{LL1} is lower than in the resulting simulation.

Fig. 5*b* shows the same input current ripple factor against inductances in the system. It should be noted that $L = L_1 = L_2 = L_3 = L_4$ and $C = C_1 = C_2 = C_3 = C_4$. As in the previous case, the theoretical high switching frequency ripple factor K_{LH1} matches accurately our simulation results. The situation is more interesting with the low frequency input current ripple factor K_{LL1}. According to the theoretical hypothesis, a resonance phenomenon was expected to occur. Because of the parasitic resistor R, this effect is not so well defined. From the point of view of the losses, the value of the parasitic resistor R is negligibly low, but it is

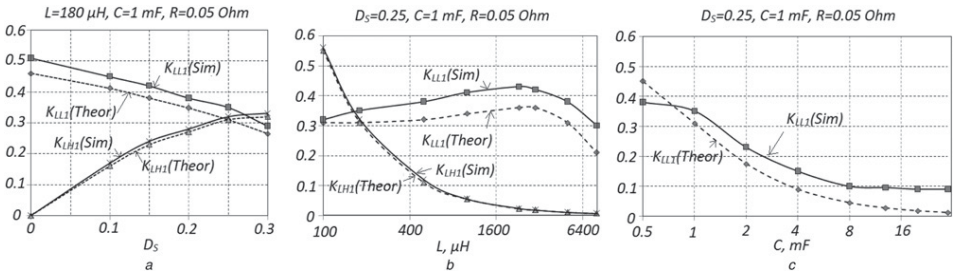

Fig. 5 *Simulation investigation of low and high switching frequency input current ripple*

a High and low input current ripple against the shoot-through duty cycle
b High and low input current ripple against inductance
c Low input current ripple against capacitance

Table 4 System parameters used for simulation and experiments

Control unit (FPGA)	Cyclone II EP2C5T144C8
transistors driver chip	ACPL-H312
transistors $T_1 \dots T_8$	SPW24N60C3
qZS and NPC diodes $D_1 \dots D_6$	8ETH06PBF
input DC voltage V_{IN}	220–325 V
output AC RMS voltage V_{OUT}	230 V
output power	1 kW
capacitance value of the capacitors C_1 and C_4	1.2 mF
capacitance value of the capacitors C_2 and C_3	0.94 mF
inductance value of the inductors $L_1 \dots L_4$	180 μH
inductance of the filter inductor L_0	2.2 mH
capacitance of the filter capacitor C_0	0.47 μF
switching frequency	100 kHz

very important for the attenuation coefficient of the oscillation. The ripple factor of the simulated current is higher. This difference is explained by the simplification of the analysis. In case the capacitors are changing (Fig. 5*c*), the resonance phenomenon is not evident.

It is well known that the attenuation coefficient of the oscillation circuit is directly proportional to the resistance and the capacitor, inversely proportional to the inductance. It means that a relatively low value of inductance and a high value of capacitance negate oscillations.

Similar results can be derived for the voltage ripple factor. It can be concluded that this approach can be preliminarily used for passive element calculation. It can help to select optimal values of inductors and capacitors to be clarified after the simulation with the parameters of real losses.

6 Experimental verification

To verify the proposed topology experimentally, a 1 kW laboratory prototype was assembled. The types and values of the components used in the experimental prototype are presented in Table 4. Taking into account the results above, the final passive elements for the experimental verification were chosen to provide the full CCM in the whole operating range.

The control system is based on the FPGA board with EP2C5T144C8 from Altera. FPGA makes it easier to implement the shoot-through mode that is important for the given topology. The ACPL-H312 chosen is a cheap high frequency unidirectional driver. High switching frequency MOSFETs with fast body diodes and hyper fast qZS diodes allow the switching frequency to be raised up to 100 kHz, which in turn reduces the size of the passive components. The passive resistor was used as a load. The regulated DC power supply was used as an input voltage source. All the measurements were made by a digital oscilloscope Tektronix DPO7254, current probes Tektronix TCP0030 and voltage probes Tektronix TPA-BNC.

Figs. 6*a* and *b* present the experimental results without and with the shoot-through states at the output power of 800 W. It can be seen that the input current is continuous at the boundary between the CCM and the DCM. The voltage of the capacitor C_1 is near zero. The capacitors C_3, C_4 have identical voltage waveforms. It reveals that the capacitors provide a stable DC-link voltage. In the first test point, the input voltage was set to 325 V that corresponds to the VSI mode where the shoot-through states are not required. It can be seen that the output *LC*-filter is sufficient in order to provide acceptable output voltage quality (lower than 5%).

Fig. 6*b* presents similar results with $D_S = 0.16$. The main idea is to maintain the constant output AC voltage during variable DC input voltage. In the second test point, the input voltage is decreased from 325 to 265 V. As can be seen, the inverter operates in the CCM. The shoot-through switching states equalise the asymmetrical switching of the transistors. It provides a more stable behaviour of the converter. The diagrams below show that the oscillating processes in the qZS-network do not lead to unstable DC-link voltage behaviour.

At the same time, Fig. 7 demonstrates the study of the operation conditions of the semi-conductors. Figs. 7*a* and *b* show the voltage and current waveforms of the transistor T1 and T5 corresponding to the states without shoot-through. It shows that the branches of the inverter

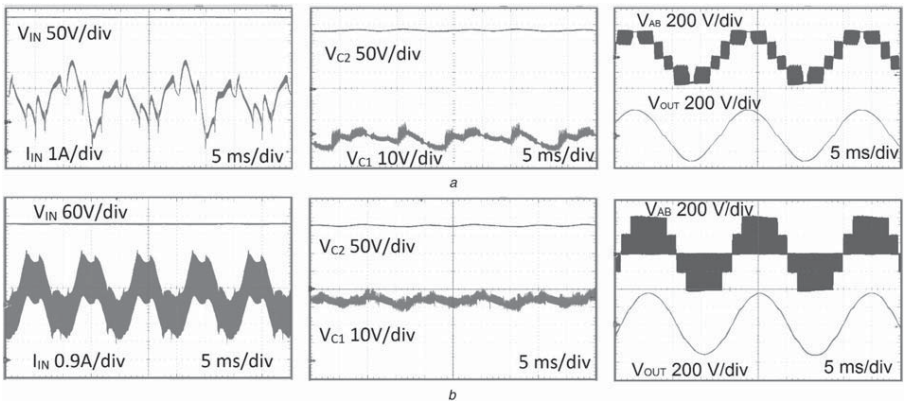

Fig. 6 *Experimental results of the 3L NPC qZSI*

a With shoot-through duty cycle
b Without shoot-through duty cycle

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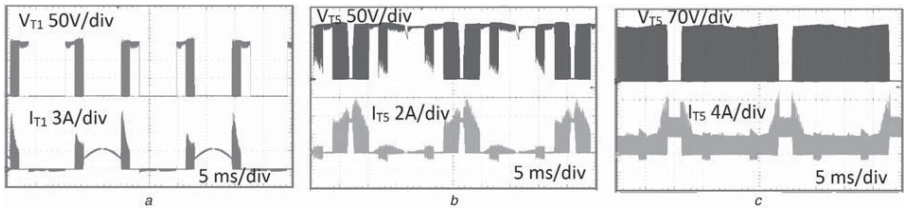

Fig. 7 *Voltage and current stress on the semiconductors*

a Voltage and current stress on the qZS diodes
b T1 and T2 transistor voltage waveforms during the fundamental cycle
c T1 and T2 transistor voltage waveforms during the switching cycle

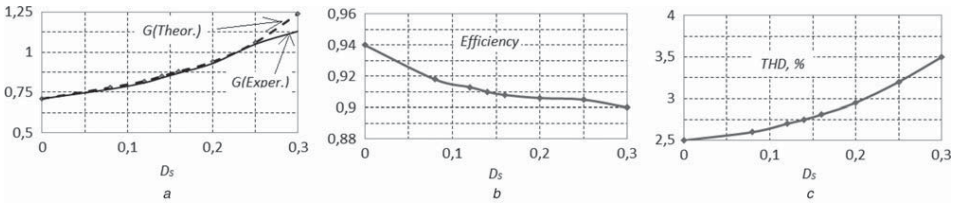

Fig. 8 *Summarised experimental study of the gain factor, the THD of the output voltage and the efficiency*

a Comparison of the gain factors obtained analytically (dashed line) and experimentally (solid line) against the shoot-through duty cycle
b Efficiency against the shoot-through duty cycle
c THD of the output voltage against the shoot-through duty cycle

work are under unequal conditions and that should be taken into account during the thermal design. Fig. 7*c* illustrates the operation difference with the shoot-through states for the transistor T5. The shoot-through states equalise the switching losses of the transistors. The presented figure enables us to estimate the current stress relative to the nominal current. At the same time, it is evident that the DC-link voltage is equally distributed among the transistors, which is very important in any multilevel topology. Further, good dynamic characteristics of the transistors lead to the absence of significant voltage spikes.

Fig. 8 summarises our experimental study of the gain factor, the total harmonic distortion (THD) of the output voltage and the efficiency. The experimental gain factor of the inverter (Fig. 8*a*) is close to that mathematically predicted which proves the quality of the obtained mathematical expressions.

The measured efficiency of the experimental prototype was in the range 90…94%. The maximum efficiency corresponds to the VSI mode without the shoot-through states and the modulation index equal to 1. Introduction of the shoot-through states decreases the efficiency, as shown in Fig. 8*b*. Fig. 8*c* shows the dependences of the THD of the output voltage against the shoot-through duty cycle. It can be seen from Fig. 8*c* that the presence of the shoot-through states slightly deteriorates the quality of the output voltage. However, because of high switching frequency, this influence is negligibly low.

It should be emphasised that the features of the semi-conductors make this solution feasible. All the semi-conductors in this topology operate in a hard switching mode. Sufficiently high efficiency can be achieved by advanced components, such as SiC Schottky diodes and power switches with low gate charge and barrier capacitance reverse diode.

7 Conclusions

This paper has presented a new topology from the family of single-stage buck-boost multilevel inverters – the three-level neutral-point-clamped quasi-Z-source inverter (3L NPC qZSI). The proposed 3L NPC qZSI combines such advantages of the qZSI and 3L NPC VSI topologies as low voltage stress of the switches, single-stage buck-boost power conversion, continuous input current, shoot-through withstandability and low output voltage and current THD. Thanks to the blocking voltage of the main switches reduced twice as compared with the two-level topology, faster transistors could be implemented. It will result in higher switching frequencies and, therefore a more compact impedance source network and low pass output filter. All these benefits could finally help to develop a compact, lightweight and reliable improved performance inverter.

A special new carrier-based modulation technique for the three-level topology with the distributed shoot-through generation was used. The control method proposed has an ability to balance the DC-link voltage. As a result, it obtains the capability of combining the required boost factor with the superior output voltage quality.

By a detailed steady-state analysis, new analytical expressions for CCM and DCM conditions for the single phase case study system were derived. The expressions derived help to understand qualitative and quantitative processes occurring in the qZS-networks of the three-level inverter. The simulation and experimental results are close to those mathematically predicted, which proves the quality of the obtained mathematical expressions.

Finally, the design recommendations and component selection guidelines were described. The properties of the proposed 3L NPC qZSI make it a reasonably competitive

topology for renewable energy applications. For example, in the PV applications, the input voltage boost capability compensates the influence of a partly shadowing effect, irradiance and temperature changes. It provides realisation of the MPPT algorithm without additional MPPT converters.

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Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application

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ABSTRACT

This paper presents a three-phase three-level neutral-point-clamped quasi-Z-source inverter as a novel solution for photovoltaic applications. The topology was derived by combining properties of the quasi-Z-source networks with those of three-level neutral-point-clamped inverters. A case study system, a steady state analysis and a novel special modulation technique for shoot-through states distribution during the whole operation period are described. Component design guidelines for a three-phase system are presented. All theoretical findings have been confirmed by simulation and experimental results. A "full SiC" experimental prototype was developed. A comprehensive study of the converter's efficiency is provided.

1. Introduction

Shortage of energy resources is a current concern. At the same time, renewable energy sources have become extremely popular. Photovoltaics (PV), wind turbines and fuel cells are most popular among renewable sources. By the end of 2013, the installed capacity of wind and solar PV power generation reached 318 GW and 139 GW, correspondingly [1].

Each source has its pros and cons. A common feature lies in their unstable operation that depends on many parameters. The main target of the power electronics converters is to provide stable output voltage despite unstable input parameters at the highest efficiency, cost and size optimization. As a result, many new types of interface converters have been developed. In PV applications, the main drawback in the present solutions lies in the narrow range of the input voltage regulation, cost and size optimization. Different solutions have been proposed [2–6].

Intermediate voltage boost dc–dc converters are used to overcome the narrow range of the input voltage regulation. At the same time, topologically, this solution is more complex and harder to control because of the two-stage power conversion. Another solution is based on the intermediate impedance-source network, classified as a single-stage energy conversion solution. Several review papers have been published [7–9].

This paper proposes a novel solution based on the three-phase three-level neutral-point-clamped quasi-Z-source inverter (3P 3L NPC qZSI) illustrated in Fig. 1. The general concept of the single-phase 3L NPC qZSI is described in [10] and experimentally verified in [11]. The three-phase 3L NPC qZSI is intended for applications that require a wide operation range of the input voltage along with the continuous conduction mode (CCM) of the input current. It is important to note that even though the system presented in Fig. 1 includes the PV panels ground capacitance [12] and the LCL filter is directly connected to the dc bus central point since it attenuates the high frequency components of the voltage across the PV parasitic capacitance [13], problematics related to leakage current paths, common-mode voltage and radiated electromagnetic emissions are considered out of the scope of this paper. Once this topology and modulation method would be validated, further works will

Abbreviations: 3P 3L NPC Qzsi, three-phase three-level neutral-point-clamped quasi-Z-source inverter; CCM, continuous conduction mode; LS-PWM, level shifted PWM; MCBC, maximum constant boost control; MBC, maximum boost control; MPP, maximum power point; MSVMBC, modified space vector modulation maximum boost control; PV, photovoltaic; PWM, pulse width modulation; qZSI, quasi-Z-source inverter; SBC, simple boost control; SVM, space vector modulation; THD, total harmonic distortion; VSI, voltage source inverter; ZSI, Z-source inverter.

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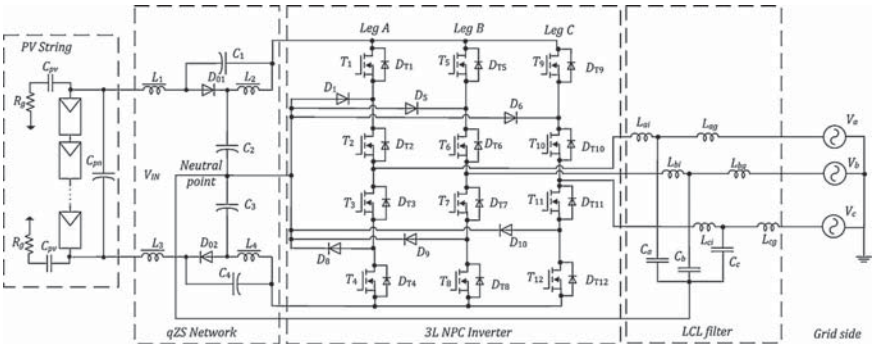

Fig. 1. Proposed novel 3P 3L NPC qZSI.

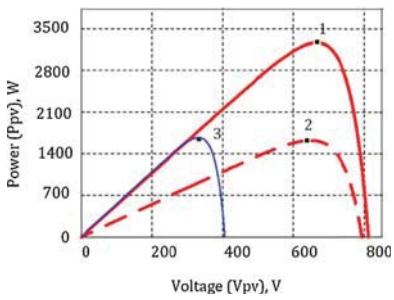

Fig. 2. PV curve of the case study.

deal with this problematic and its possible solutions [14,15] in PV inverter transformer-less applications.

1.1. Case study system description

A PV installation of 18 serial panels is a voltage source for the converter topology. Fig. 2 shows the resulting input PV curve. It is well known that solar panels provide limited voltage and current that follows an exponential *I–V* curve.

Several models have been reported for solar panel simulations [16–20]. A mathematical model based on the *I–V* exponential curves and parameters provided in the manufacturer's datasheet is used to simulate the PV array. Its mathematical foundation is detailed in [21]. Table 1 presents main specifications of a commercial solar module (LDK 185D-24(s)) [22].

Several working points are marked in Fig. 2. Even low but equally distributed solar irradiation does not require extremely high boost (point 2). High boost capabilities are demanded in a partly shadowed mode where only some of the panels in the array have lower irradiation (point 3). It can be seen that the maximum power point (MPP) with maximum irradiation corresponds to the voltage source inverter (VSI) mode that requires no voltage boost feature (point 1).

Section 2 describes the proposed solution in detail. Section 3 explains the new modulation technique developed for such applications. Section 4 presents the results of simulation and experiment verification.

Table 1
Main parameters from the panel datasheet [18].

Parameters	Unit	Value
Nominal output power (P_{max})	W	185
Voltage at P_{max}	V	36.9
Current at P_{max}	A	5.02
Open circuit voltage (V_{oc})	V	45.1
Short circuit current (I_{sc})	A	5.48

2. Description of the proposed solar inverter

The quasi-Z-source inverters (qZSIs) proposed in [23,24] were intended to further improve the traditional Z-source inverters (ZSI).

Besides the advantages inherited from the ZSIs [23], the qZSIs have reduced passive component ratings and continuous input current. In contrast to the two-level VSI, the 3L NPC inverter has many advantages, such as lower voltage stress across semiconductors, lower required blocking voltage capability, decreased dv/dt, higher switching frequency due to the lower switching losses, and better harmonic performance [24,25]. In addition, several papers [26–28] have reported that 3L topology has better elimination capability of the common mode leakage current, and as a result, no additional common mode filters are required.

2.1. Operation principle and steady state analysis of the proposed topology

Each branch of the inverter has three output voltage levels: $0 \pm V_{DC}/2$, where V_{DC} is the peak of the dc-link voltage. The operating period of the 3P 3L-NPC qZSI in the CCM may be divided into several time intervals. Table 2 shows all possible switching states of the transistors in the topology. Taking into account that the inverter has three branches, each of which may have three states, altogether 27 states are possible. At the same time, in a traditional three-phase system, states where all branches have positive or negative output voltage values are excluded.

Finally, due to the qZS network, another shoot-through state is added when all the transistors are conducting. During this state, energy is accumulated in the inductors and is transferred to the capacitors and output load within other states. As a result, the peak dc-link voltage is regulated only by adjusting the shoot-through duty cycle. This switching state is excluded for traditional VSIs because it causes a short circuit of the dc-link capacitors.

Considering all the time intervals presented above, the behavior of the qZS network can be represented by means of three equivalent circuits shown in Fig. 3. Accordingly, all the switching states can be separated into three main modes: zero state (Fig. 3a), active states (Fig. 3b) and shoot-through state (Fig. 3c) that can be applied within

Table 2
Switching states of transistors in 3P 3L NPC qZSI.

Switching states	Mode	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}
1		1	1	0	0	0	1	1	0	0	1	1	0
2		1	1	0	0	1	1	0	0	0	1	1	0
3		1	1	0	0	0	1	1	0	1	1	0	0
4		1	1	0	0	0	0	1	1	0	1	1	0
5		1	1	0	0	0	1	1	0	0	0	1	1
6		1	1	0	0	1	1	0	0	0	0	1	1
7		1	1	0	0	0	0	1	1	1	1	0	0
8		1	1	0	0	0	0	1	1	0	0	1	1
9		0	1	1	0	1	1	0	0	1	1	0	0
10		0	1	1	0	1	1	0	0	0	1	1	0
11		0	1	1	0	0	1	1	0	1	1	0	0
12		0	1	1	0	0	0	1	1	0	1	1	0
13	Active	0	1	1	0	0	1	1	0	0	0	1	1
14		0	1	1	0	1	1	0	0	0	0	1	1
15		0	1	1	0	0	0	1	1	1	1	0	0
16		0	1	1	0	0	0	1	1	0	0	1	1
17		0	0	1	1	0	1	1	0	0	1	1	0
18		0	0	1	1	1	1	0	0	0	1	1	0
19		0	0	1	1	0	1	1	0	1	1	0	0
20		0	0	1	1	0	0	1	1	0	1	1	0
21		0	0	1	1	0	1	1	0	0	0	1	1
22		0	0	1	1	1	1	0	0	0	0	1	1
23		0	0	1	1	0	0	1	1	1	1	0	0
24		0	0	1	1	1	1	0	0	1	1	0	0
25	Zero	0	1	1	0	0	1	1	0	0	1	1	0
26	Shoot-through	1	1	1	1	1	1	1	1	1	1	1	1

the zero state. However, such approach is valid for a three-phase symmetric system.

To estimate values of the passive components and recommend guidelines for semiconductor selection, the steady state analysis was performed. In the analysis, the voltage balance across the inductors and current balance across the capacitors were used. The operating period of the converter in the CCM is represented as

$$\frac{t_A}{T} + \frac{t_Z}{T} + \frac{t_S}{T} = D_A + D_Z + D_S = 1, \tag{1}$$

where D_A is the duty cycle of the active state, D_Z is the duty cycle of the zero state, and D_S is the duty cycle of the shoot-through state. T is a fundamental switching period. The sum of the capacitor voltages defines the peak of the dc-link voltage:

$$V_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4}, \tag{2}$$

where V_{C1}, V_{C2}, V_{C3}, V_{C4} are average voltages across the capacitors over one period. Taking into account that the qZS network is symmetric, it was assumed that $L_1 = L_3$, $L_2 = L_4$ and $C_1 = C_4$, $C_2 = C_3$. Accordingly, voltages are $v_{L1} = v_{L3}$, $v_{L2} = v_{L4}$, and $V_{C1} = V_{C4}$ $V_{C2} = V_{C3}$.

The voltage on the capacitors can be found from the voltage balance of the inductors over one switching period. Taking into account the conditions above, the voltages across the capacitors can be obtained as:

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{2 - 4D_S}, \tag{3}$$

$$V_{C2} = V_{C3} = \frac{V_{IN}(1 - D_S)}{2 - 4D_S}. \tag{4}$$

The final equation for the boost factor is obtained:

$$B = \frac{V_{DC}}{V_{IN}} = \frac{V_{C1} + V_{C2} + V_{C3} + V_{C4}}{V_{IN}} = \frac{1}{1 - 2D_S}. \tag{5}$$

Since the converter must operate both in the islanding mode and in the grid connected mode, the output phase to the neutral point voltage RMS value has to be maintained around $V_{OUT} = 230$ V. In the three-phase system, the phase to the neutral voltage is derived:

$$V_{OUT} = M\frac{V_{DC}}{2\sqrt{2}} = M\frac{V_{IN}}{2\sqrt{2}(1 - 2)D_S}. \tag{6}$$

Since the modulation index M has to be in a range of $M \le 1 - D_S$ and the output voltage is constant, dependences between the input voltage V_{IN} and the shoot-through duty cycle D_S are

$$V_{OUT} = \frac{(1 - D_S)V_{IN}}{2\sqrt{2}(1 - 2)D_S}. \tag{7}$$

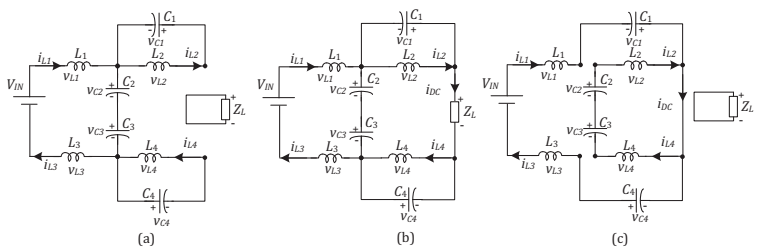

Fig. 3. Equivalent circuits of the 3P 3L-NPC qZSI: zero state (a), active state (b), shoot-through state (c).

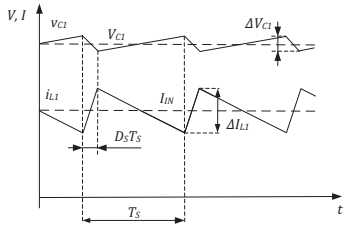

Fig. 4. Sketch of the input current ripple and voltage ripple on the capacitors.

2.2. qZS-network estimation

In a real system, the operating waveforms of the 3P 3L-NPC qZSI are distorted by the ripple, as shown in Fig. 4. At a symmetric three-phase load, the input current has high frequency ripple, which is connected with the high frequency shoot-through duty cycle switching.

The rising speed depends on the inductor and capacitor voltages. It means that the high frequency ripple of the current can be found from the shoot-through interval:

$$\Delta I_{L1} = \int_0^{T_S D_S} \frac{\mathrm{d}i_{L1}}{\mathrm{d}t}\mathrm{d}t = \int_0^{T_S D_S} \left(\frac{V_{IN} + V_{C1} + V_{C4}}{2L}\right)\mathrm{d}t = \left(\frac{V_{IN} + V_{C1} + V_{C4}}{2L}\right) T_S D_S, \quad (8)$$

where T_S is the switching period. In order to maintain the CCM operation of the converter, the input current ripple ΔI_{L1} should be smaller than the average input current I_{IN}. The average input current can be defined from the power balance:

$$P_{IN} = V_{IN}, \quad I_{IN} = P_{OUT}. \quad (9)$$

At the CCM condition with the predefined current ripple, from Eqs. (3), (8) and (9), it can be written as:

$$K_L \frac{\Delta I_{L1}}{I_{IN}} = \frac{4V^2\mathrm{OUT}(1 - 2D_S)}{(1 - D_S)LP_{OUT}} T_S D_S, \quad (10)$$

The minimum value of the inductance in order to guarantee a ripple in the inductor current to maintain the CCM operation of the proposed inverter can be defined as:

$$L \geq \frac{4V^2\mathrm{OUT}(1 - 2D_S)}{(1 - D_s)K_L P_{OUT}} T_S D_S. \quad (11)$$

Capacitor voltage ripple can be defined in a similar way:

$$\Delta V_{C1} = \Delta V_{C4} = \frac{1}{C_1}\int_0^{D_S T_S} i_C(t)\mathrm{d}t = \frac{1}{C_1}\int_0^{D_S T_S} i_{L1}(t)\mathrm{d}t. \quad (12)$$

Since the inductance current has linear character, expression (12) can be simplified:

$$\Delta V_{C1} = \Delta V_{C4} = \frac{1}{C_1} I_{IN} T_S D_S. \quad (13)$$

The required value of the capacitance of C_1 to maintain the desired voltage ripple factor K_{C1} can be obtained as:

$$K_{C1} = \frac{\Delta V_{C1}}{V_{C1}} = \frac{T_S P_{OUT}(1 - D_S)^2}{4C_1 V_{OUT}^2(1 - 2D_S)}, \quad (14)$$

As a result, the capacitor can be calculated as:

$$C_1 = C_4 \geq \frac{T_S P_{OUT}(1 - D_S)^2}{4K_C V_{OUT}^2(1 - 2D_S)}. \quad (15)$$

Capacitor voltage ripple on the capacitors C_2 and C_3 can be defined in a similar way:

$$\Delta V_{C2} = \Delta V_{C3} = \frac{1}{C_2}\int_0^{T_S D_S} i_C(t)\mathrm{d}t = \frac{1}{C_2}\int_0^{T_S D_S} i_{L2}(t)\mathrm{d}t. \quad (16)$$

Taking into account that inductors' currents are equal, the required value of the capacitance of C_2 and C_3 to maintain the desired voltage ripple factor K_{C2} can be obtained as:

$$K_{C2} \geq \frac{T_S P_{OUT}(1 - D_S)D_S}{4C_2 V_{OUT}^2(1 - 2D_S)}. \quad (17)$$

Finally, capacitance values for capacitors C_2, C_3 are defined as:

$$C_2 = C_3 \geq \frac{T_S P_{OUT}(1 - D_S)D_S}{4C_2 V_{OUT}^2(1 - 2D_S)}. \quad (18)$$

To demonstrate how the input voltage range influences the passive elements of the qZS network, from expressions (7), (11), (15), and (18), it can be written as:

$$L \geq \frac{2T_S V_{OUT} V_{IN}}{\sqrt{2}K_L P_{OUT}} \cdot \frac{2\sqrt{2}V_{OUT} - V_{IN}}{4\sqrt{2}V_{OUT} - V_{IN}} \quad (19)$$

$$C_1 = C_4 \geq \frac{2T_S P_{OUT}}{K_{C1} V_{IN}} \cdot \frac{1}{4\sqrt{2}V_{OUT} - V_{IN}}, \quad (20)$$

$$C_2 = C_3 \geq \frac{T_S P_{OUT}}{\sqrt{2}K_{C2} V_{OUT} V_{IN}} \cdot \frac{2\sqrt{2}V_{OUT} - V_{IN}}{4\sqrt{2}V_{OUT} - V_{IN}}, \quad (21)$$

Fig. 5 illustrates the dc-link voltage and values of passive elements as functions of the input voltage.

All dependences are presented in the relative units where one voltage unit corresponds to $2\sqrt{2}V_{OUT}$. Relative units of the passive elements are defined as:

$$L = \frac{4T_S V_{OUT}^2}{K_L P_{OUT}} = 1\ \text{p.u.} \quad (22)$$

$$C = \frac{T_S P_{OUT}}{K_C 4V_{OUT}^2} = 1\ \text{p.u} \quad (23)$$

where $K_C = K_{C1} = K_{C2}$ is a voltage ripple factor on the capacitors. It should be noted that in the buck mode, a converter works like a traditional VSI and an impedance network is not involved in its operation. Therefore, only the boost mode is considered in the figure. Solid lines show passive element values as a function of the input voltage under constant input power. At the same time, dotted lines illustrate similar dependences under constant input current that correspond to the PV curve. This figure shows that the highest inductance corresponds to the lowest input voltage. The same conclusion applies to the capacitors.

As a result, passive component values necessary to provide predefined voltage and current quality can be estimated.

2.3. Selection of semiconductors

Voltage stress is one of the key parameters for semiconductor selection. Voltage stress on the transistors, as well as on the diodes, is equal to half the dc-link voltage. As shown above and illustrated in Fig. 5a, the dc-link voltage depends on the input voltage:

$$V_{DC} = 4\sqrt{2}V_{OUT} - V_{IN}. \quad (24)$$

Similarly, voltage on the capacitors that defines the dc-link voltage can be derived:

$$V_{C1} = V_{C4} = \sqrt{2}V_{OUT} - \frac{V_{IN}}{2}. \quad (25)$$

$$V_{C2} = V_{C3} = \sqrt{2}V_{OUT}. \quad (26)$$

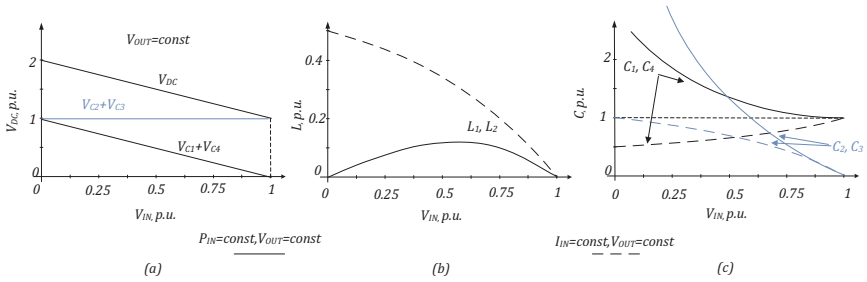

Fig. 5. 3P 3L NPC qZS inverter: dc-link and capacitors voltage (a), inductance (b) and capacitances (c) versus input voltage.

Table 3
Applicability of modulation methods to multilevel topologies.

Topology	NPC	Flying capacitor	Cascaded H-bridge
Modulation method			+
Space vector modulation	+	+	+
Level shifted PWM	+	+	+
Phase shifted PWM	–	+	+
Hybrid modulation	–	–	+
Selective harmonic elimination	+	+	+
Space vector control	0	+	+
Nearest level control	0	+	+

The main conclusion from the presented figure is that higher dc-link voltages correspond to the smallest input voltage. Thus, in order to provide the input voltage range from 300 V up to 800 V, semiconductors must withstand the dc-link voltage in a range of 650–1000 V. It means that the maximum voltage stress on the transistors and on all the diodes is equal to 500 V (half the dc-link voltage) plus the switching spike. At the same time, it is evident that the sum of the capacitor voltage $V_{C2} + V_{C3}$ is constant in the boost mode and can be used like a controlled value in a closed loop system. It should be mentioned that in the three-phase topology without the neutral point dc-link voltage, capacitor voltage can be reduced by means of third harmonic injections.

There are several appropriate semiconductor solutions. Classical IGBT with a 1200 V blocking voltage can be used. The main advantage of this solution is its reliability. The drawback lies in a low switching frequency that forces use of larger passive elements. Recently, MOSFETs based on SiC have appeared as a new family of fast high-voltage switches. Derived from experimental investigations [6,11] of the dc–dc and dc–ac converters based on the qZS network, it can be concluded that out of all solutions for the qZS diode, only Shottky diodes suit. Because of relatively high voltage, SiC based Shottky diodes can be used.

3. Special shoot-through modulation technique

3.1. Review of existing strategies

Several modulation techniques or shoot-through control methods for the three-phase two-level Z-source inverters have been reported [29–36]. These controls are mainly classified as: Simple boost control (SBC) [29], maximum boost control (MBC) [30], maximum constant boost control (MCBC) [31], and modified space vector modulation control (MSVMBC) [32]. Among other techniques, they have been used to control converters in such applications as PV solar energy and fuel cells [33,34].

MCBC has been selected because of its advantages over other control methods. Recent studies have focused on multilevel inverter topologies, modulation and control methods [37–44]. As a result, numerous modulation techniques have been proposed, each one featured by its advantages and disadvantages depending on the application.

A good comparison between different modulation methods is presented in [39]. The authors divide the modulation methods for a multilevel converter into two main groups: space vector based methods and carrier based methods. Space vector modulation (SVM) or multicarrier pulse width modulation (PWM) is recommended for high frequency applications. In the first case, the reference voltage is represented as a reference vector to be tracked by the power converter. All the discrete possible switching states are matched as state vectors. Finally, the reference voltage is calculated as a linear combination of these state vectors; an averaged output

Table 4
List of parameters used for simulation and experimental setup.

Parameters	Unit	Value in each working point		
		1	2	3
Inductors L_1, L_2, L_3 and L_4	(mH)		0.9	
Capacitors C_1, C_2, C_3 and C_4	(μF)		200	
W	(W/m^2)	1000	500	1000
Panels in series (Ns)			18	
Arrays in parallel (Np)	Unit		1	
Vpv	(V)	650	565	325
Ppv	(W)	3333	1534	1666
L_{f1}	(mH)		0.5	
L_{f2}	(mH)		0.2	
C_f	(μF)		0.47	
m		≃1	1	0.7
Third harmonic	%	0	19	19
D_S		0	0	0.3
Switching frequency (with shoot-through states generation)	(kHz)		100 kHz	

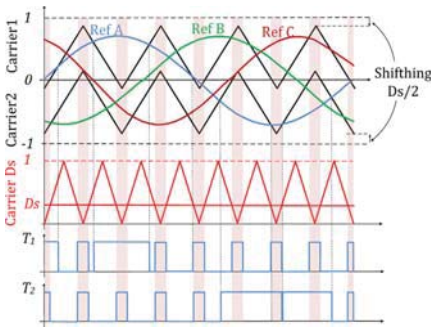

Fig. 6. Sketch of LS-PWM in phase disposition with MCBC.

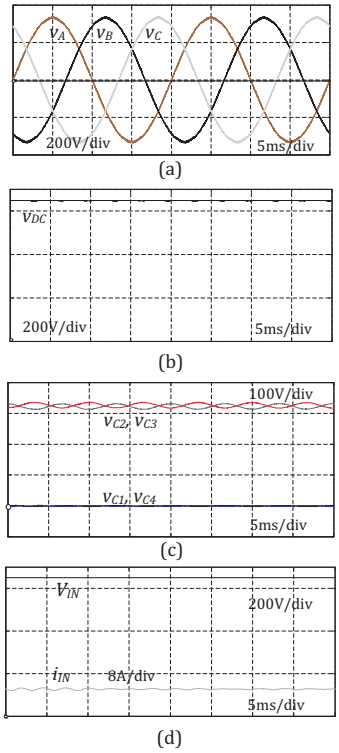

Fig. 7. Simulation waveforms for the first point in the VSI mode without the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

voltage is obtained equal to the reference in one switching period [43]. In the second case, the reference voltage is compared with multiple carriers to control each power switch. In this method, carriers can be arranged in phase shifted or level shifted dispositions.

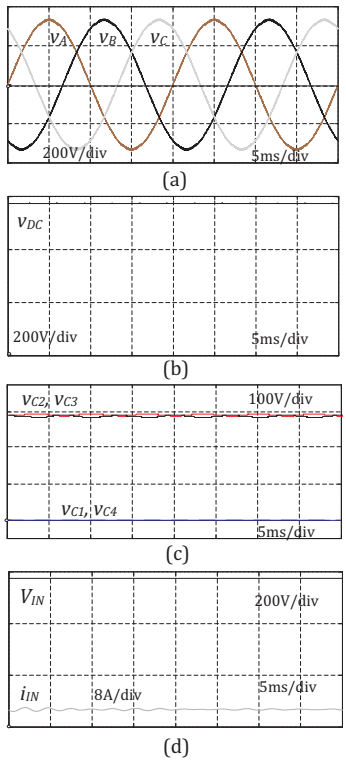

Fig. 8. Simulation waveforms for the second point in the VSI mode with the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

In addition, a table in [39] shows different levels of applicability of each modulation method to the multilevel inverter topologies reproduced in Table 3.

At the same time, several solutions based on the SVM control were designed for 3L ZSIs [45–49]. Early developments in switching signal generation for this inverter family are reported in [45]. To enhance the boost factor, the injection of the third harmonic offset [46] is also added to the reference signals. Further development of SVM techniques was devoted to simplify implementation and to improve the output voltage harmonic spectrum [48,49].

According to the aforementioned characteristics of each modulation method and their applicability to different topologies, a carrier-based level shifted PWM (LS-PWM) in phase disposition with MCBC as a novel solution for the 3P 3L NPC qZSI. This modulation technique is detailed below.

3.2. New carrier-based PWM control strategy

Fig. 6 shows a sketch of the novel LS-PWM in phase disposition with MCBC for the 3P 3L NPC qZS inverter using a frequency modulation index (mf) equal to 4.

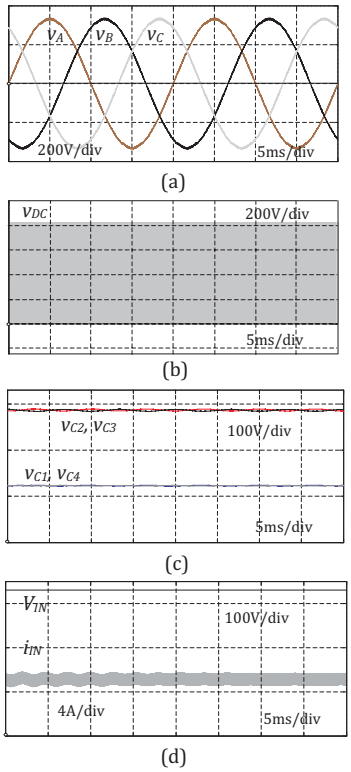

Fig. 9. Simulation waveforms for the third point with the third harmonic injection and shoot-through states generation: output voltages (a), dc-link voltage (b), input current and input voltage (c).

Three modulating waves (one per phase) and two triangular carriers (upper ∈[0,1] and lower ∈[−1,0]) were compared to obtain different normal states. Generation of the gate signals for transistors T_1 and T_2 is demonstrated in Fig. 6. It corresponds to the reference signal Ref A. T_3 and T_4 have their complementary state, respectively. The third harmonic injection is commonly used in a three-phase inverter system to increase the modulation index range M and in consequence, the system voltage gain range as well. According to [30], the maximum M is equal to $2/\sqrt{3} \approx 1.15$ when $1/6 \approx 0.19$ of the third harmonic is injected.

Another carrier signal (∈[0,1]), but at double frequency, is used to generate the shoot-through states (Sst) by means of comparison with the constant value of D_S. Operating in this way, uniformly distributed shoot-through states with the constant width during the whole output voltage period are achieved. Due to the insertion of the shoot-through states, the output average phase to neutral voltages is modified, which is necessary to solve the problem. In order to maintain the constant output average voltage, upper and lower carriers are displaced $D_S/2$ to assure the reference value.

At the same time, the proposed modulation technique has double switching frequency shoot-through generation, which allows reducing passive components of the impedance networks.

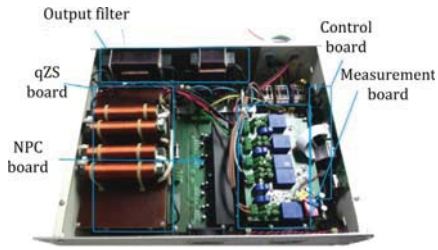

Fig. 10. Photo of the experimental prototype of the 3P 3L NPC qZSI.

It means that the converter can operate at lower switching frequency under the maximum power point and losses can be minimized. Voltage boost is not required in this point. At the voltage boost, the power is reduced and shoot-through generation frequency can be raised to shrink the passive elements of the qZS network.

4. Simulation and experimental study of the 3P 3L NPC qZSI

4.1. Simulation study

In order to verify the proposed concepts, a comprehensive simulation study was performed in the PSCAD simulation tool. Table 4 shows all the parameters used in the simulation and experimental studies. The LCL-filter was designed according to [50] in order to provide an 8% lower THD of the output current (voltage). Switching frequency was 100 kHz in the shoot-through states generation mode. At the same time, without shoot-through states generation, switching frequency was twice reduced, which corresponds to the proposed modulation technique.

Fig. 7 illustrates several simulation results for the first operating point: Fig. 7a – the waveforms of the output voltages; Fig. 7b – the dc-link voltage; Fig. 7c – voltages in the capacitors; Fig. 7d – input current and input voltage. In the first working point, the input voltage is equal to 650 V.

No voltage boost occurs, the third harmonic injection and shoot-through generation are not activated. A solar inverter works in the VSI mode. As can be seen, no ripples are present in the input current or the dc-link voltage because shoot-through switching states are not activated. Voltage on the capacitors C_1, C_4 is equal to zero.

Fig. 8 shows identical simulation results for the second operating point.

It can be seen that the input voltage is equal to 565 V. The third harmonic injection is present while shoot-through states generation is unactivated.

Fig. 9 depicts the main waveforms obtained for the third working point.

Table 5
Specification of the experimental prototype.

Parameter/component	Value/type
Output voltage (line to line)	400 V
Input-voltage range	300–800 V
Nominal power	3.5 kW
THD	≤8%
Control unit	Cyclon IV EP4CE22E22C8
Transistors driver	ACPL H342
Transistors	SiC C2M0080120D
Diodes	SiC C3D10065A
Current measurement	LEM LTS 15-NP
Voltage measurement	LEM LV25-P

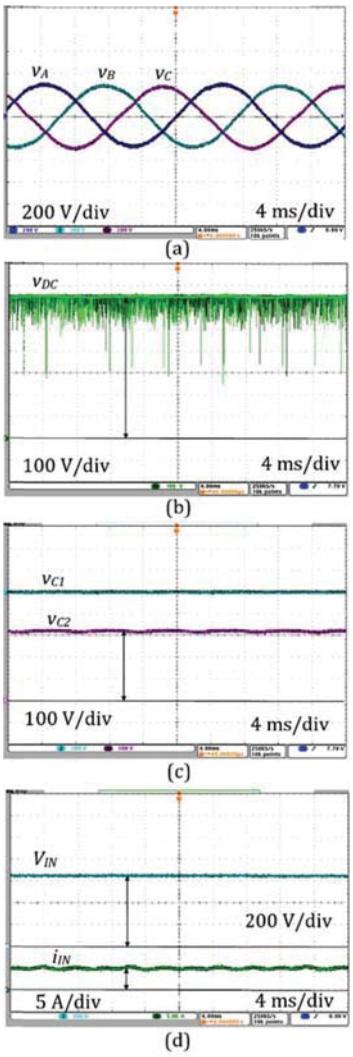

Fig. 11. Experimental waveforms for the first point in the VSI mode without the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

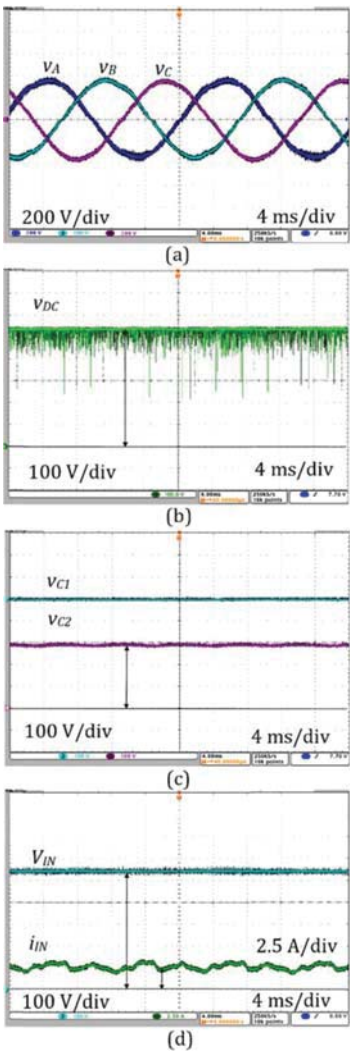

Fig. 12. Experimental waveforms for the second point in the VSI mode with the third harmonic injection: output voltages (a), dc-link voltage (b), input current and input voltage (c).

In this point, maximum boost capability is required by the third harmonic injection along with the shoot-through states to maintain 230 V phase to neutral voltages. Input voltage is equal to 365 V. The output voltage has very good quality. DC-link voltage has equally distributed shoot-through states. As a result, despite the low input voltage, the output voltage is equal to the nominal value.

4.2. Experimental study of the 3P 3L NPC qZSI

This section presents the experimental results of the topology described above. Fig. 10 shows the experimental prototype, which was finally assembled in a 3U box. It consists of four main PCB boards with external qZS inductors and output filters.

Our experimental study was conducted to confirm the simulation results and investigate the overall efficiency of the converter. Several operation points were tested in full accordance with the simulation results. Parameters of the passive components and case study points are listed in Table 4. Advanced specification of the experimental prototype is presented in Table 5. All measurements were made by a digital oscilloscope Tektronix MDO4034B-3,

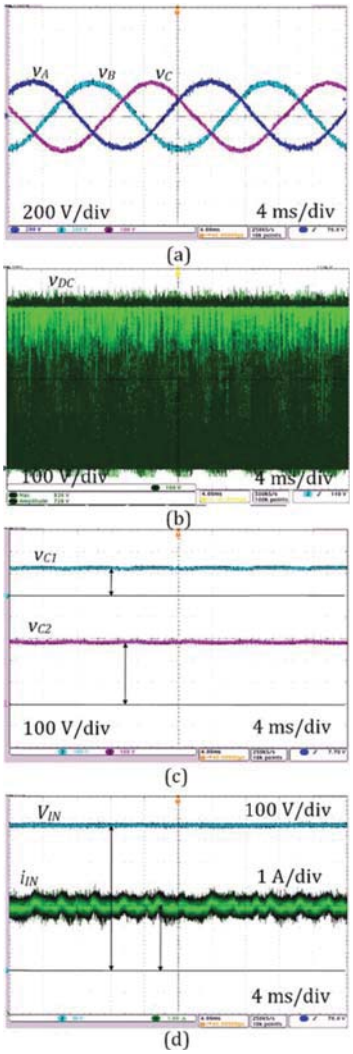

Fig. 13. Experimental waveforms for the third point with the third harmonic injection and shoot-through states generation: output voltages (a), dc-link voltage (b), input current and input voltage (c).

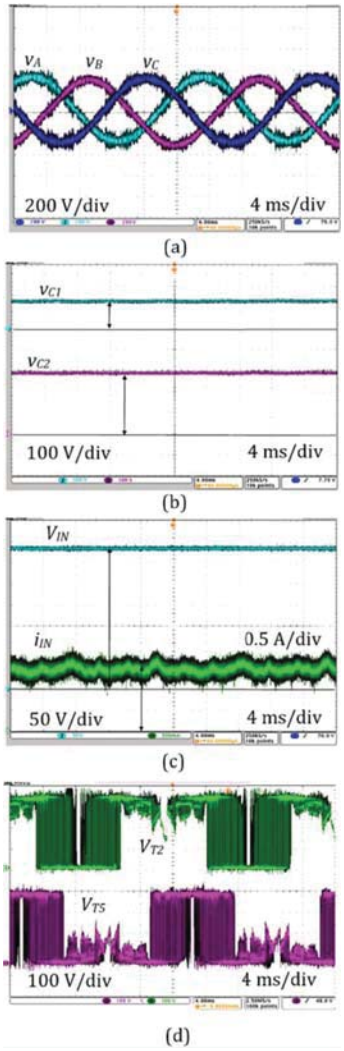

Fig. 14. Oscilloscope waveforms of the experimental prototype under light load operation: the output phase to the neutral voltage (a), voltage on the capacitors (b), input current and the input voltage (c), voltage stress on the semiconductors (d).

current probes Tektronix TCP0150, and voltage probes Tektronix TPA-BNC.

Fig. 11 shows several oscilloscope waveforms for the first operation point. The order of the measured parameters is in full correspondence with the simulation results depicted in Fig. 7. The voltage on the capacitors C_3 and C_4 is not shown since it coincidences with the voltage on the capacitors C_1 and C_2 correspondingly. It can be seen that no ripples are present in the input current or the dc-link voltage because shoot-through switching states are unactivated.

At the same time, Fig. 12 illustrates the experimental results for the second operation point. The results obtained are very similar to the simulation results shown in Fig. 8.

Finally, Fig. 13 shows our experimental results for the third operation point. Obviously, these are close to the simulation results in Fig. 9. In summary, it could be concluded that our experiment confirms the theoretical and simulation analyses.

Table 6 summarizes the comparison of the results obtained. It can be seen that our experimental results are in good agreement with the theoretical results. At the same time, some differences in

Table 6
Comparative analysis of theoretical (theor), simulation (sim) and experimental (exp) results.

Parameter	Unit	1			2			3		
		Theor	Sim	Exp	Theor	Sim	Exp	Theor	Sim	Exp
Average input current I_{IN}	(A)	5.12	5.1	5	2.71	2.7	2.7	5.12	5.1	5
Input current ripple ΔI_{L1}	(A)	0	0	0	0	0		0.96	1	0.9
Average voltage on the capacitors C_1, C_4	(V)	0	0	0	0	0		122	122	122
Voltage ripple ΔV_{C1} on the capacitors C_1, C_4	(V)	0	0	0	0	0		0.08	0.08	0.1
Average voltage on the capacitors C_2, C_3	(V)	325	325	324	282.5	283		284	284	283
Voltage ripple ΔV_{C2} on the capacitors C_2, C_3	(V)	0	0	0	0	0		0.08	0.08	0.1

the absolute values of the input current capacitor ripples relate to variations in the real passive elements. Further, it should be noted that simulation and experimental waveforms have some minor low frequency ripples, which can be explained by the resonance nature of any impedance network, especially with the high-Q circuit.

Fig. 14 shows additional experimental results under light load operation. Input power was about 450 W at the input voltage of 325 V. This operation is very similar to the third operation point that corresponds to the partial shadowing. In this case, low solar irradiation along with partial shadowing occur. Specifically, Fig. 14a shows oscilloscope waveforms of the output three-phase voltage. It can be seen that the quality of the output voltage is worse than in the previous case. The reason is that output filter was designed for the nominal power and cannot provide the same quality under light load operation. At the same time, it should be underlined that output voltage disturbances belong to the high switching harmonics. 50 kHz and higher switching harmonics are out of the measuring range by standards. Voltage on the capacitors (Fig. 14b) remains unchanged and is similar to Fig. 13c. Fig. 14c shows the input current and the input voltage. The average value of the input current is about 1.4 A at the high frequency ripple of about 0.9 A. It should be noted that input current still has CCM.

Voltage stress on the semiconductors is illustrated in Fig. 14d. It is evident that no significant spikes occur on the transistors, which confirms good dynamic behavior of the SiC semiconductors. Excellent dynamic performance of the chosen SiC semiconductors leads to a very small voltage switching spike, which enhances the reliability of the converter.

4.3. Study of power losses

Fig. 15 illustrates the estimated efficiency of the described inverter. The study was conducted by using the method of summation of losses and the support of a thermal camera (Fluke Ti10), as well as the measurement equipment listed in Section 4.2. Fig. 15a shows the thermal picture of the NPC board. Fig. 15b shows the qZS network board. Despite the maximum power, the temperature of the heat sink does not exceed 40 °C. Therefore, no external fans are required. Further, as it was expected, qZS diodes are the main source of losses, but the temperature of the semiconductor junction is quite low. Fig. 15c and d illustrates the final efficiency diagram based on the power dissipation in the power semiconductors and magnetic components, which was experimentally estimated. Fig. 15c shows the dependence of the efficiency versus the input voltage and the input power. It should be noted that this surface belongs to the constant irradiation level when the input voltage and power depend on the partial shadowing effect.

Fig. 15d shows the losses distribution for the expected MPP with a maximum efficiency (3.3 kW and 650 V input voltage). Losses in different semiconductor components were estimated by means of temperature measurement of heat sinks and the thermal resistances of thermofilm and heat sink from datasheet parameters. The magnetic losses calculation was obtained by means of subtraction from the overall efficiency the semiconductor losses. In this point, the converter works in the VSI mode with $D_S = 0$ and it can achieve an efficiency of 98.5%. In the worst case, the total efficiency was about 96.7%. The decrease in the efficiency is connected with the shoot-through states generation, which increases the switching losses in the transistors. In conclusion, transistor losses are about 28% of the total losses. At the same time, only two qZS diodes lead to 37% of the total losses, as shown in Fig. 15d.

Fig. 16 shows the comparison of the efficiency curves both with maximum input current and light load operation. Input current as well as output voltage were constant at each point but input voltage changed. In the first case (dotted line), input current is about 5 A, which corresponds to the maximum level. In the second case (solid

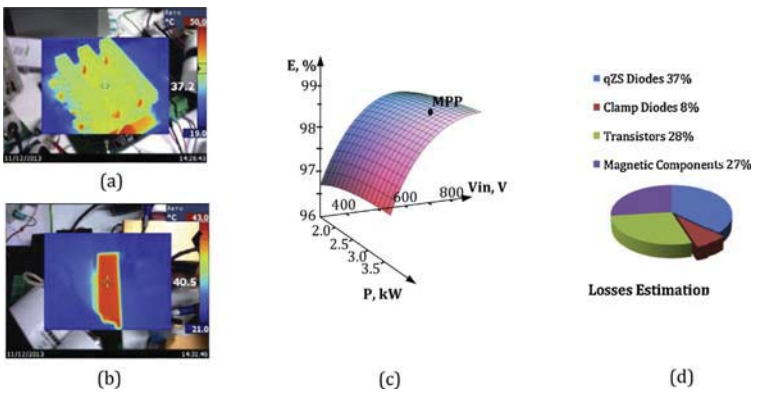

Fig. 15. Thermal pictures for the first operating point (a, b) and efficiency versus input voltage and input power (c), distribution of the losses for a maximum power point (d).

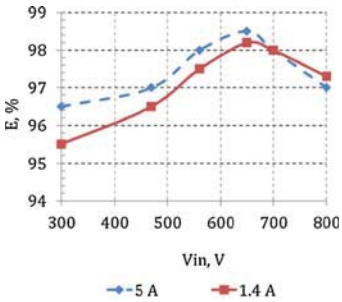

Fig. 16. Dependence of the efficiency on the input voltage with different input current levels.

line), input current is about 1.4 A, which corresponds to the light load operation.

It can be seen that in the second case, the efficiency was slightly worse, especially at the low input voltage level, with an efficiency of about 95.5%. At the same time, in the nominal input voltage point, the efficiency is almost equal, which corresponds to the MPP and is even slightly higher at the maximum voltage level. The results obtained agree with the expectation, since for any type of a converter, light load operation is often a problem from the efficiency point of view.

5. Conclusions

This paper proposes the 3P 3L NPZ qZSI as a novel solution for PV applications. The converter combines advantages of the qZSI and 3L NPC VSI topologies. Low voltage stress on the switches, single-stage buck-boost power conversion, continuous input current, short-circuit immunity, and reduced output voltage and current THD are the main benefits. Thanks to the modern SiC semiconductors, high switching frequency is achievable. Therefore, a more compact impedance source network and low pass output filter are used. All these benefits could finally help to develop a more compact, lightweight and reliable inverter with improved performance.

A special new carrier-based modulation technique for the three-phase 3L topology with double frequency and uniformly distributed shoot-through generation was developed. The simulation and experimental results proved all theoretical expectations. Finally, efficiency measurement confirmed an outstanding performance of the inverter. In the nominal operation point, an efficiency higher than 98% and in the shoot-through generation mode, not lower than 95.5% was achieved.

Acknowledgments

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CCM Operation Analysis of the Single-Phase Three-Level Quasi-Z-Source Inverter

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***Abstract* – This paper presents a CCM analysis of a new modification of a three-level single phase neutral-point-clamped inverter. The proposed topology combines advantages of the three-level neutral-point-clamped full-bridge inverter with those of the quasi-Z-source inverter. The three-level neutral-point-clamped quasi-Z-source inverter is especially suitable for renewable energy sources. The steady-state analysis of a three-level neutral-point-clamped quasi-Z-source inverter in the case of the continuous conduction mode is presented. The conditions of the continuous conduction mode are obtained and analyzed.**

***Keywords* – Three-level neutral-point-clamped inverter, continues conduction mode, quasi-Z-source inverter.**

I. Introduction

A three-level neutral-point-clamped (3L-NPC) inverter (Fig. 1*a*) has a number of advantages over the two-level voltage source inverter, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased *dv/dt*, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage. As a drawback, in contrast to the two-level voltage source inverter, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per phase-leg. The 3L-NPC can normally perform only the voltage buck operation. In order to ensure voltage boost operation an additional DC/DC boost converter should be used in the input stage [1-2].

To obtain buck and boost performance the focus is on a quasi-Z-source inverter (qZSI, Fig. 1*b*). The qZSI was first introduced in [3]. The qZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter [3-11]. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the DC-link capacitors. Thus, the qZSI has excellent immunity against the cross conduction of the top and bottom-side inverter switches. The possibility of using shoot-through eliminates the need for dead-times without having the risk of damaging the inverter circuit.

Recently, a new modification of the qZSI was proposed: a three-level neutral point clamped quasi-Z-source inverter (3L-NPC qZSI). This topology combines advantages of the three-level neutral-point-clamped full-bridge inverter with those of the quasi-Z-source inverter having the buck-boost capability of the input voltage and the enhanced output voltage quality [12, 13].

Thanks to its specific properties the 3L-NPC qZSI is especially suitable as power conditioner for the renewable energy systems, where the continuous conduction mode operation (CCM) is a very important issue. During the CCM the input current never drops to zero, thus featuring the reduced stress of the input voltage source, which is especially topical in such demanding applications as power conditioners for fuel cells and solar panels. The opposite case, the discontinuous conduction mode (DCM) in the converter evokes additional losses in the system and increases the operating range of the components. It is particularly relevant in single phase inverters where consumption of instantaneous power is variable, leading to variable input current. As a result, the CCM condition is not easily achievable and has not been observed in similar converter topologies [6, 7].

This paper presents the steady-state analysis of a single phase 3L-NPC qZSI in the case of the CCM and discusses some design guidelines in order to maintain the CCM operation.

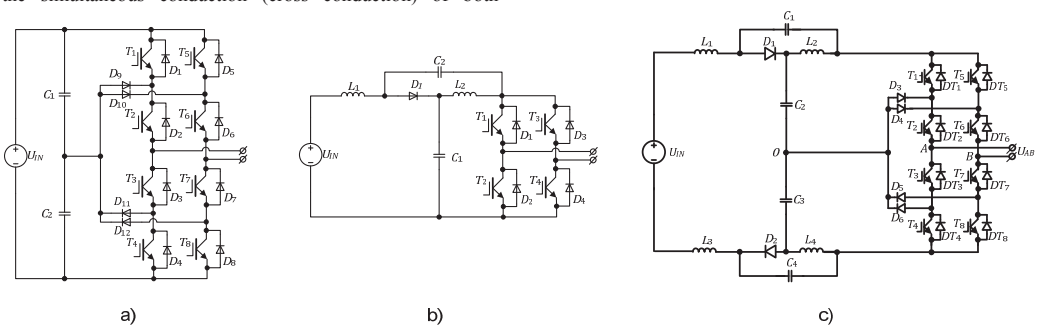

Fig. 1. Topologies of the 3L-NPC (a), qZSI (b) and 3L-NPC qZSI.

II. General Description and Steady-State Analysis of 3L-NPC qZSI

Fig. 1*c* illustrates the proposed topology of a 3L-NPC qZSI. Each leg of the 3L-NPC qZSI consists of two complementary switching pairs and four anti-parallel diodes. Advantages of this topology over the traditional two-level voltage source inverter are: continuous input current, use of shoot-through, lower switching losses, and balanced neutral-point voltage.

Shoot-through states are equally distributed over the operating period of the inverter. The inverter output voltage has three different levels: 0, $B\cdot(U_{IN}/2)$ and $B\cdot U_{IN}$ in the positive and negative directions, where B is the inverter boost factor. The shoot-through vector is generated separately. Finally, the shoot-though vector is mixed with other control signals.

In general, the operating period of the 3L-NPC qZSI in the continuous conduction mode (CCM) may be divided into 8 time intervals, as shown in Fig. 2. Transistor states for each time interval are depicted in Fig. 3. As it can be seen, all the switching states can be separated into three main modes: zero state (Fig 3*a*), active states (Fig 3*c*-*h*) and shoot-through state (Fig 3*b*). On the other hand, active states are separated on the three submodes.

An equivalent scheme for zero-state intervals is shown in Fig. 3*a*. Equations that describe the behavior of the converter in this mode are as follows:

$$U_{IN} - L_1\frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3\frac{dI_{L3}}{dt} = 0\,, \tag{1}$$

$$U_{C1} + L_2\frac{dI_{L2}}{dt} = 0\,, \tag{2}$$

$$L_4\frac{dI_{L4}}{dt} + U_{C4} = 0\,, \tag{3}$$

$$-I_{ZL}Z_L = 0\,, \tag{4}$$

$$I_{L1} = I_{L3}\,, \tag{5}$$

$$I_{L1} + C_1\frac{dU_{C1}}{dt} - I_{L2} - C_2\frac{dU_{C2}}{dt} = 0\,, \tag{6}$$

$$C_3\frac{dU_{C3}}{dt} + I_{L4} - C_4\frac{dU_{C4}}{dt} - I_{L3} = 0\,, \tag{7}$$

$$C_2\frac{dU_{C2}}{dt} - C_3\frac{dU_{C3}}{dt} = 0\,, \tag{8}$$

$$U_{OUT} = I_{ZL}Z_L\,. \tag{9}$$

An equivalent scheme for the shoot-through intervals is shown in Fig. 3*b*. Equations that describe the behavior in this mode are as follows:

$$U_{IN} - L_1\frac{dI_{L1}}{dt} + U_{C1} + U_{C4} - L_3\frac{dI_{L3}}{dt} = 0\,, \tag{10}$$

$$U_{C2} - L_2\frac{dI_{L2}}{dt} = 0\,, \tag{11}$$

$$U_{C3} - L_4\frac{dI_{L4}}{dt} = 0\,, \tag{12}$$

$$I_{L1} = I_{L3}\,, \tag{13}$$

$$I_{L1} + C_1\frac{dU_{C1}}{dt} = 0\,, \tag{14}$$

$$C_3\frac{dU_{C3}}{dt} + I_{L4} = 0\,. \tag{15}$$

The first equivalent scheme for the active state is shown in Fig. 3*c*. It corresponds to the case when the output voltage is equal to half of the DC-link voltage. The middle point is clamped through the load to the high side of the DC-link. Equations (16) to (25) describe the behavior in this mode:

$$U_{IN} - L_1\frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3\frac{dI_{L3}}{dt} = 0\,, \tag{16}$$

$$U_{C1} + L_2\frac{dI_{L2}}{dt} = 0\,, \tag{17}$$

$$L_4\frac{dI_{L4}}{dt} + U_{C4} = 0\,, \tag{18}$$

$$U_{C2} - L_2\frac{dI_{L2}}{dt} - U_{OUT} = 0\,, \tag{19}$$

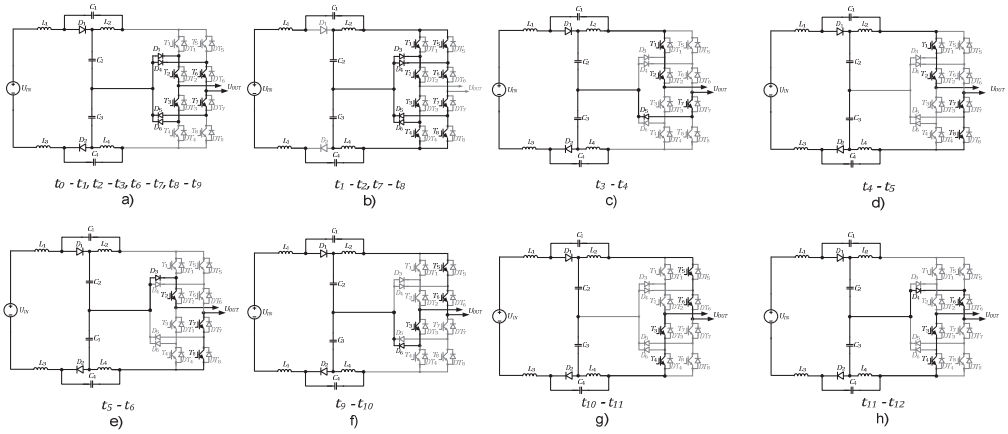

Fig. 2. Transistor states for each time interval.

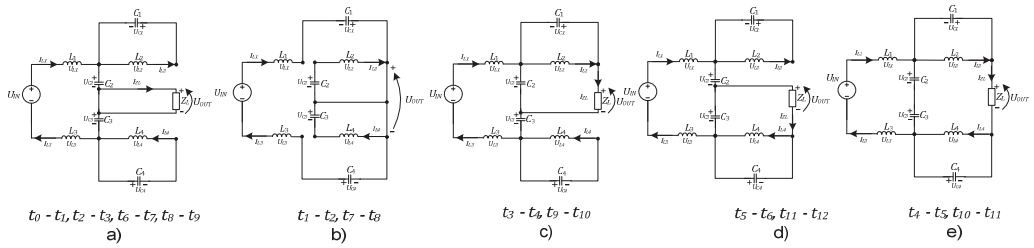

Fig. 3. Equivalent schemes of main operating modes.

$$I_{L1} = I_{L3}\,, \tag{20}$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0\,, \tag{21}$$

$$I_{L2} - C_1 \frac{dU_{C1}}{dt} - I_{ZL} = 0\,, \tag{22}$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0\,, \tag{23}$$

$$C_2 \frac{dU_{C2}}{dt} - C_3 \frac{dU_{C3}}{dt} + I_{ZL} = 0\,, \tag{24}$$

$$U_{OUT} = I_{ZL} Z_L\,. \tag{25}$$

The second equivalent scheme for the active state is shown in Fig. 3*d*. It corresponds to the case when the output voltage is equal to half of the DC-link voltage and the middle point is clamped through the load to the low side of the DC-link. Equations (26) to (35) describe the behavior in this mode:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3 \frac{dI_{L3}}{dt} = 0\,, \tag{26}$$

$$U_{C1} + L_2 \frac{dI_{L2}}{dt} = 0\,, \tag{27}$$

$$L_4 \frac{dI_{L4}}{dt} + U_{C4} = 0\,, \tag{28}$$

$$U_{C3} - U_{OUT} - L_4 \frac{dI_{L4}}{dt} = 0\,, \tag{29}$$

$$I_{L1} = I_{L3}\,, \tag{30}$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0\,, \tag{31}$$

$$I_{ZL} - I_{L4} + C_4 \frac{dU_{C4}}{dt} = 0\,, \tag{32}$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0\,, \tag{33}$$

$$C_2 \frac{dU_{C2}}{dt} - C_3 \frac{dU_{C3}}{dt} - I_{ZL} = 0\,, \tag{34}$$

$$U_{OUT} = I_{ZL} Z_L\,. \tag{35}$$

The third equivalent scheme for the active state is shown in Fig. 3*e*. It corresponds to the case when the output voltage is equal to the DC-link voltage. Equations (36) to (45) describe the behavior of the converter in this mode:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3 \frac{dI_{L3}}{dt} = 0\,, \tag{36}$$

$$U_{C1} + L_2 \frac{dI_{L2}}{dt} = 0\,, \tag{37}$$

$$L_4 \frac{dI_{L4}}{dt} + U_{C4} = 0\,, \tag{38}$$

$$U_{C3} + U_{C2} - L_2 \frac{dI_{L2}}{dt} - U_{OUT} - L_4 \frac{dI_{L4}}{dt} = 0\,, \tag{39}$$

$$I_{L1} = I_{L3}\,, \tag{40}$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0\,, \tag{41}$$

$$I_{ZL} - I_{L4} + C_4 \frac{dU_{C4}}{dt} = 0\,, \tag{42}$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0\,, \tag{43}$$

$$I_{L2} - C_1 \frac{dU_{C1}}{dt} - I_{ZL} = 0\,, \tag{44}$$

$$U_{OUT} = I_{ZL} Z_L\,. \tag{45}$$

To simplify the analysis it was assumed that the input capacitors and inductors are identical, thus:

$$L_1 = L_3, \qquad L_2 = L_4\,, \tag{46}$$

$$C_1 = C_4, \qquad C_2 = C_3\,. \tag{47}$$

The operating period of the converter in the CCM could be represented as

$$\frac{t_N}{T} + \frac{t_S}{T} = D_N + D_S = 1\,. \tag{48}$$

where D_N is the duty cycle of the non-shoot-through and D_S is the shoot-through duty cycle.

In the steady state the average voltage of the inductor over one switching period is zero and the voltages across the capacitors are constant. Thus, by Eqs. (1) to (45), the voltages across the capacitors can be found:

$$U_{C1} = U_{C4} = \frac{D_S \cdot U_{IN}}{2 - 4 \cdot D_S}\,, \tag{49}$$

$$U_{C2} = U_{C3} = \frac{U_{IN} \cdot (D_S - 1)}{4 \cdot D_S - 2}\,. \tag{50}$$

The peak DC-link voltage is the sum of all the capacitor voltages:

$$U_{DC} = U_{C1} + U_{C2} + U_{C3} + U_{C4} = \frac{U_{IN}}{1 - 2 \cdot D_S}\,. \tag{51}$$

Taking into account the maximum possible value of the modulation index $M=1-D_S$, the boost factor of the 3L-NPC

qZSI can be estimated as

$$B = \frac{U_{OUT\_MAX}}{U_{IN}} = \frac{U_{DC} \cdot (1 - D_S)}{U_{IN}} = \frac{1 - D_S}{1 - 2 \cdot D_S}, \quad (52)$$

where U_{OUT_MAX} is an amplitude value of the output voltage.

III. CCM Condition and Some Design Guidelines for the 3L-NPC qZSI

In an ideal case, the DC-link voltage and the input current of the 3L-NPC qZSI are constant. The main problem lies in the floating instantaneous consuming power that evokes current fluctuations in the corresponding capacitors. A simplified equivalent scheme of the qZS network is shown in Fig. 4*a*. The capacitors and inductors are represented as ideal voltage and current sources, correspondingly. The idealized operating waveforms of the 3L-NPC qZSI are shown in Fig. 4*b*.

In a real system the operating waveforms are distorted by the ripple as shown in Fig. 4*c*. As it can be seen, the DC-link voltage has low frequency fluctuation (100 Hz) caused by instantaneous output power. As a result, it causes low frequency input current fluctuations. Also, it should be noticed that the input current has high frequency ripple. It is connected with the high frequency shoot-through duty cycle switching.

In order to eliminate low frequency fluctuations in the system it is necessary to maintain constant voltages across the capacitors despite the AC component present in the DC-link current.

Capacitor voltage ripple can be expressed as

$$\Delta U_{C1} = \Delta U_{C4} = \frac{1}{C_1} \int_0^{T/4} i_C(t)dt = \\ = \frac{1}{C_1} \int_0^{T/4} \frac{P_{OUT}}{U_{DC}} \cdot sin(2 \cdot \frac{2\pi}{T} \cdot t)dt = \frac{T \cdot P_{OUT}}{2\pi \cdot C_1 \cdot U_{DC}}, \quad (53)$$

where T is the period of the sinusoidal output voltage. The required value of the capacitance of C_1 to maintain the desired voltage ripple factor K_C can be obtained using Eqs. (49), (52) and (53):

$$K_C = \frac{\Delta U_{C1}}{U_{C1}} = \frac{T \cdot P_{OUT} \cdot (1 - D_S)^2}{2\pi \cdot C_1 \cdot U_{OUT\_MAX}^2 \cdot D_S}, \quad (54)$$

where K_C is the voltage ripple factor.

As a result, the capacitor can be calculated:

$$C_1 \geq \frac{T \cdot P_{OUT} \cdot (1 - D_S)^2}{2\pi \cdot K_C \cdot U_{OUT\_MAX}^2 \cdot D_S}. \quad (55)$$

Capacitance values for capacitors C_2, C_3 could be defined similarly:

$$C_2 \geq \frac{T \cdot \mathrm{P_{OUT}} \cdot (1 - D_S)}{2\pi \cdot K_C \cdot \mathrm{U_{OUT\_MAX}^2}}. \quad (56)$$

A decrease in speed is defined by the equivalent schemes and it depends on the load resistance R. The rising speed depends on the inductor and capacitor voltages. It means that high frequency ripple of the current can be found from the shoot-through interval.

From Eq. (10) we obtain:

$$\Delta I_{L1} = \int_0^{T_S \cdot D_S} \frac{dI_{L1}}{dt} \cdot dt = \int_0^{T_S \cdot D_S} (\frac{U_{IN} + U_{C1} + U_{C4}}{2 \cdot L}) \cdot dt = \\ = (\frac{U_{IN} + U_{C1} + U_{C4}}{2 \cdot L}) \cdot T_S \cdot D_S, \quad (57)$$

where T_S is the switching period. In order to maintain the CCM operation of the converter the input current ripple ΔI_{L1} should be smaller than the average input current I_a. The average input current can be defined from the power balance:

$$P_{IN} = U_{IN} \cdot I_a = P_{OUT}. \quad (58)$$

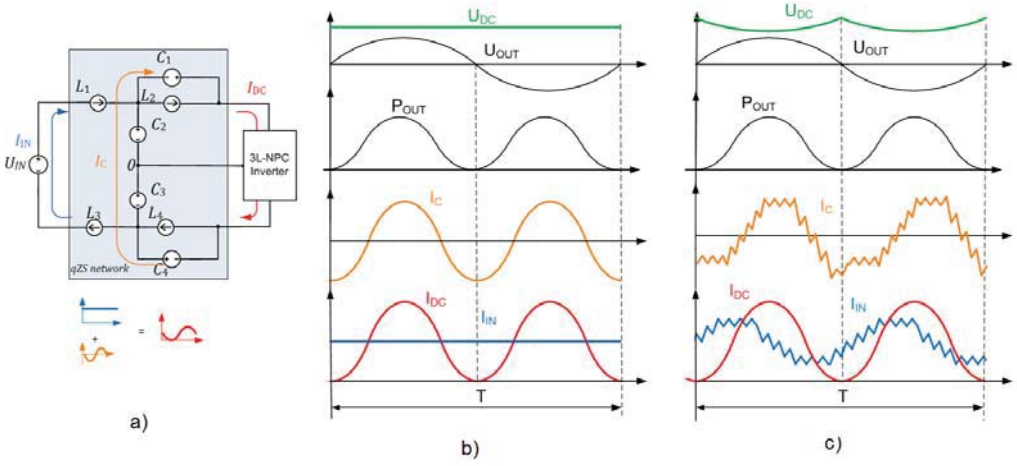

Fig. 4. Equivalent scheme and diagrams in the CCM.

Taking into account the CCM condition:

$$K_{\mathrm{L}} = \frac{\Delta I_{L1}}{I_a} = \frac{U^2{}_{OUT\_MAX} \cdot (1-2\cdot D_S)}{2\cdot(1-D_S)\cdot \mathrm{L}\cdot \mathrm{P}_{\mathrm{OUT}}} T_{\mathrm{S}} \cdot D_S\,, \quad (59)$$

and from Eqs. (49), (53) and (54) we can express:

$$L \geq \frac{U^2{}_{OUT\_MAX} \cdot (1-2\cdot D_S)}{2\cdot(1-D_S)\cdot K_L \cdot P_{OUT}} T_S \cdot D_S\,. \quad (60)$$

It means that we can define the minimum value of the inductance in order to maintain the CCM operation of the proposed inverter.

IV. Simulation Results

In order to verify theoretical background several simulations have been carried out. The first results cover the case with the output power of about 1 kW. Fig. 5 shows the obtained simulation results, listed from top to bottom: input current and input voltage (Fig. 5*a*), voltage across the capacitors (Fig. 5*b*), and output voltage before and after the filter (Fig. 5*c*). It is seen that inverter operates in the CCM and capacitor voltage ripple is about 10%. The capacitance value selected for $C_1 \ldots C_4$ was 2.5 mF and inductance value set for $L_1 \ldots L_4$ was 0.25 mH.

Next, the simulation was done for the light load and full power operating points. Fig. 6 shows the input current and capacitor voltage for 100 W and 5 kW (Figs. 6*a* and *b*, correspondingly). The main conclusion is that the CCM is unachievable with low output power.

It can be concluded that the capacitor value in a real system has to be larger than analytically predicted by (55) that is connected with power losses in the real system. Fig. 7 shows the dependences of the capacitor value that is necessary in order to obtain a voltage ripple lower than 10%. There are three cases presented: first is the theoretical prediction assuming ideal components and other two belong to the cases with winding resistances of the inductors of 0.01 Ω and 0.25 Ω, respectively. The main conclusion is that the capacitance value of the capacitors has to be increased with the losses due to the voltage drop in the DC-link and the requirement to keep the amplitude of the output voltage constant.

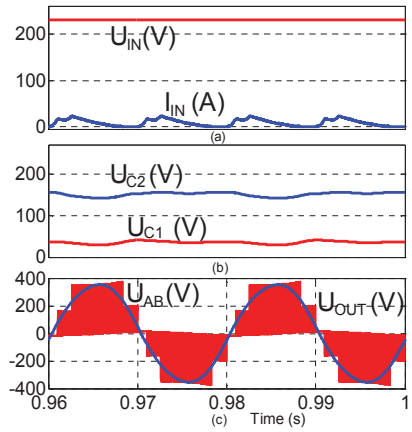

Fig. 5. Simulation results for 1 kW output power.

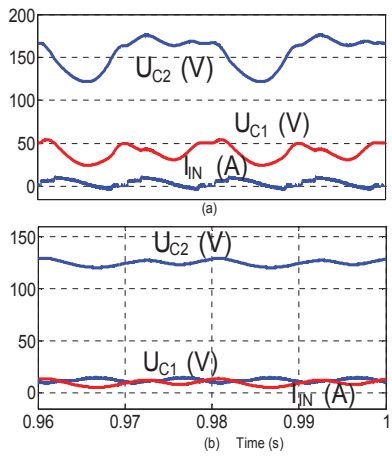

Fig. 6. Simulation results for 100 W (a) and 5 kW (b) output power.

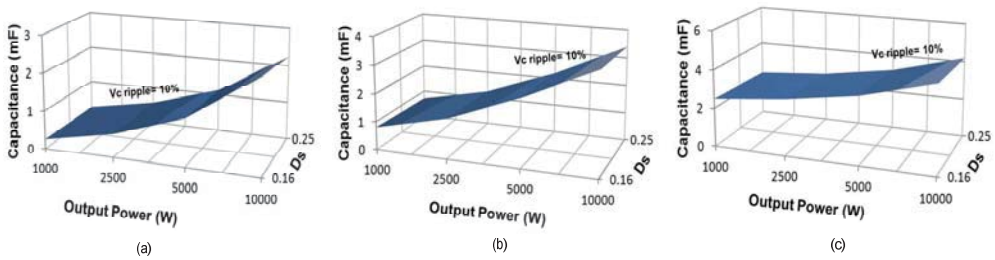

Fig. 7. Dependences of capacitance value C_1 on P_{OUT} and D_S.

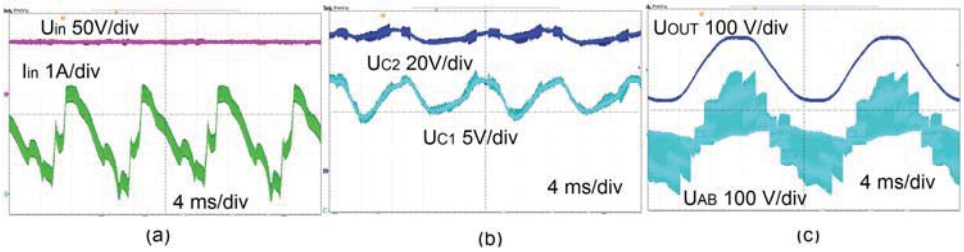

Fig. 8. Experimental results for 200 W output power.

V. Experimental Verification

To verify the above presented assumptions a 500 W experimental setup was assembled. System parameters and component values used in the experiment are presented in Table I.

TABLE I. System Parameters and Component Values Used for the Experiment

Input DC voltage U_N	130 V
Output AC voltage U_{OUT}	110 V (RMS)
Capacitance value of the capacitors C_1, C_4	1160 uF
Capacitance value of the capacitors C_2, C_3	920 uF
Inductance value of the inductors L_1 ... L_4	160 uH
Inductance of the filter inductor L_0	4.4 mH
Capacitance of the filter capacitor C_0	240 uF
Switching frequency	50 kHz

The control system is based on the FPGA board with EP2C5T144C8 from Altera. The ACPL-H312 drivers were chosen for a MOSFET transistor drive. Fig. 8 presents the experimental results. The input voltage was 130 V and output RMS voltage was 110 V. Carrier frequency was set to 50 kHz.

Fig. 8*a* shows the input current and voltage waveforms. It can be seen that the input current is on the border between the CCM and DCM. The voltages across the capacitors of the ZS network are shown in Fig 8*b*. As it can be seen, the capacitor voltages have a ripple of about 30%. The output voltage waveforms before and after the LC-filter are shown in Fig. 8*c*.

VI. Conclusions

The proposed single phase 3L-NPC qZSI is a combination of the quasi-Z-source inverter and the three-level NPC inverter. The 3L-NPC qZSI derives advantages from both topologies: it can buck and boost the input voltage; it has excellent short circuit immunity, due to the multilevel topology the higher power density is achievable.

In order to reduce the low frequency fluctuations of the DC-link voltage in a 3L-NPC qZSI large values of the capacitors are required. At the same time it is practically impossible to eliminate low frequency input current ripple completely, especially during the light load operating point. Such an effect will disappear in a symmetrically loaded three-phase system, because it is connected with the consumption of floating instantaneous power in a single-phase system. At the same time high frequency input current ripple is defined by the inductance value and switching frequency. Since the MOSFET transistors can be used in such topologies the switching frequency can be high and as a result, the value of the inductance can be significantly decreased.

Acknowledgement

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Single Phase Three-Level Quasi-Z-Source Inverter With a New Boost Modulation Technique

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***Abstract*— This paper describes a new modulation technique for a single phase three-level neutral-point-clamped qZS inverter. The proposed converter is intended for applications that require input voltage gain and high quality of the output voltage. The simulation and experimental results are presented and discussed.**

I. Introduction

A three-level neutral-point-clamped (3L-NPC) inverter has many advantages, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased *dv/dt*, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage, in contrast to the two-level voltage source inverter. However, as a drawback, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per phase-leg than the two-level voltage source inverter. The 3L-NPC can normally perform only the voltage buck operation. In order to ensure voltage boost operation an additional DC/DC boost converter should be used in the input stage [1-2].

To obtain buck and boost performance the focus is on a quasi-Z-source inverter (qZSI). The qZSI was first introduced in [3]. The qZSI can buck and boost DC-link voltage in a single stage without additional switches.

The qZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the DC-link capacitors. Thus, the qZSI has excellent immunity against the cross conduction of top and bottom-side inverter switches. The possibility of using shoot-through eliminates the need for dead-times without having the risk of damaging the inverter circuit. The input voltage is regulated only by adjusting the shoot-through duty cycle. In addition, the qZSI has a continuous mode input current (input current never drops to zero), which makes it especially suitable for renewable energy sources (e.g. fuel cells, solar energy, wind energy etc.). The main drawback of the qZSI is its poor performance in the case of small loads and relatively low switching frequency. In these conditions the qZSI starts to work in a discontinuous conduction mode, which causes an over-boost effect and leads to instabilities [3-7].

A three-level neutral-point-clamped quasi-Z-source inverter (3L-NPC qZSI,) proposed recently is a new modification of the qZSI. The new converter combines the advantages of the two topologies described above.

Fig. 1 illustrates the proposed topology of a 3L-NPC qZSI. Each leg of the 3L-NPC qZSI consists of two complementary switching pairs and four anti-parallel diodes. As an advantage, this topology can have continuous input current, the possibility to use shoot-through, lower switching losses and balanced neutral-point voltage in comparison with the traditional two-level voltage source inverter.

The inverter output voltage has three different levels: 0, $B\cdot(U_{IN}/2)$ and $B\cdot U_{IN}$ in the positive and negative directions, where B is the inverter boost factor. The shoot-through vector is generated separately during zero states. Finally, the shoot-though vector is mixed together with other control signals.

As a result, such topology is suitable for photovoltaic applications because the boost capability and the shoot-through duty cycle allow compensating the influence of the irradiance and temperature changes on the input voltage.

At the same time the shoot-through switching state demands new approaches in the modulation technique in order to combine the boost factor with the best possible voltage quality.

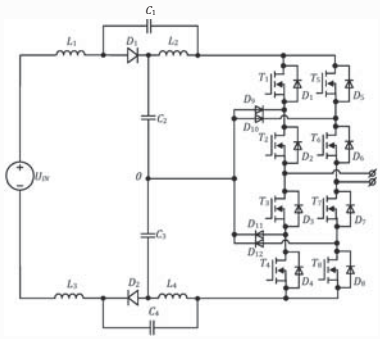

Fig. 1. Three-level neutral-point-clamped quasi-Z-source inverter (3L-NPC qZSI).

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This paper is an attempt to improve the voltage quality of the 3L-NPC qZSI by a new modulation technique.

II. NEW MODULATION TECHNIQUE

There are several pulse width modulation (PWM) techniques that could be applied for the 3L-NPC qZSI [4], [11]-[14].The core idea of these methods is presented in Fig. 2. All of them generate the shoot-through states when the output voltage is in the zero state (U_{AB} = 0) in order to maintain constant and unaltered normalized average voltage per switching period whereas the shoot-through states are carefully and centrally added to the active states that enable the number of higher harmonics to be kept to a minimum.

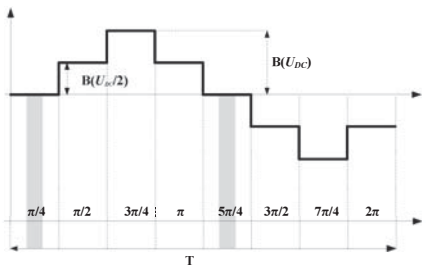


Fig. 2. Output voltage waveform of the traditional shoot-through PWM for the 3L-NPC qZSI.

Using these PWM techniques for the 3L-NPC qZSI, the U_{AB} has only two zero states per period and shoot-through states can only be placed during these two intervals ([0, π/4] and [π, 5π/4]).

These techniques present some problems, such as a larger size of the passive elements, more input current ripple and capacitor voltage disbalance.

A. Description of General Principles

Fig. 3*a* shows a sketch of the proposed modulation technique.

One modulating sinusoidal wave and four triangular carriers are compared to obtain the different states of T_1, T_2, T_5 and T_6 and T_3, T_4, T_7 and T_8 have the complementary state of the other, respectively.

Carrier$_1$ is used to generate the shoot-through states in comparison with a constant value that includes the desired D_s value. Operating in this way, uniformly distributed shoot-through states with the constant width during the whole output voltage period can be achieved.

In order to compensate the average voltage U_{AB} when the shoot-through states are applied, leg *B* must compensate this situation through the change of the voltage U_{B0}. Fig. 3*b* shows how we can obtain this compensation.

During the positive semi-cycle, leg *B* has to produce $U_{B0} = -U_{dc}/2$ more times to restore the average voltage U_{AB}. This is produced through *carrier*$_4$ displacement that generates the pulses of T_6. During the negative semi-cycle the same situation is produced. Leg *B* has to produce $U_{B0} = +U_{dc}/2$ more times to restore the average voltage U_{AB}. This is produced through *carrier*$_3$ displacement that controls the pulses of T_5.

The resulting waveform of the output voltage before the output filter is shown schematically in Fig. 3*c*.

B. Boost Regulation Capability

In the proposed modulation technique the desired boost is reached because the shoot-through states are distributed with a constant width during the whole output voltage period and the qZ stage is working at the maximum frequency. Furthermore, by this technique we can use the ratio between the modulation index (*M*) and the maximum shoot-through duty cycle D_{S_MAX} (1) and the ratio between *B* and D_s (2):

$$D_{S\_MAX} \le 1 - M\,, \tag{1}$$

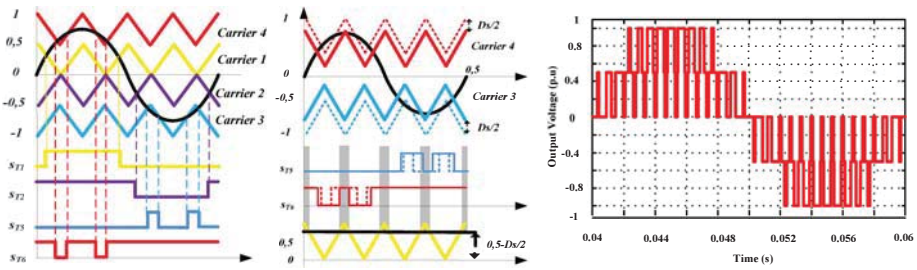
$$B = \frac{U_{DC}}{U_{IN}} = \frac{1}{1 - 2 \cdot D_S}\,. \tag{2}$$

As a result, taking into account (1) the maximum value of the output voltage we obtain

$$U_{MAX\_OUT} = U_{IN} \cdot M \frac{1}{(1 - 2 \cdot D_S)}\,. \tag{3}$$

Using the maximum possible value of the modulation index, the amplitude of the output voltage can be estimated as

$$U_{MAX\_OUT} = U_{IN} \cdot \frac{1 - D_S}{(1 - 2 \cdot D_S)}\,. \tag{4}$$



(a) (b) (c)

Fig. 3. Sketch of the proposed modulation technique with uniformly distributed shoot-through states and constant width.

III. Simulation and Experimental Verification of The Proposed Modulation Technique

To verify the proposed modulation technique a small power scaled experimental board was assembled. Preliminary verification was done by help of a simulation model assembled in the SimPowerSystems of Matlab/Simulink.

A. System Parameters

The values of the parameters of the qZS network and the output filter are presented in Table I.

TABLE I. System Parameters Used for Simulations and Experiments

Control Unit (FPGA)	Cyclone II EP2C5T144C8
Driver Chip	ACPL-H312
Input DC voltage U_N	130 V
Output AC voltage U_{OUT}	130-160 V
Capacitance value of the capacitors C_1, C_4	240 uF
Capacitance value of the capacitors C_2, C_3	1180 uF
Inductance value of the inductors L_1 ... L_4	160 uH
Inductance of the filter inductor L_0	4.4 mH
Capacitance of the filter capacitor C_0	240 uF
Switching frequency	25 kHz

The control system is based on the FPGA board with EP2C5T144C8 from Altera. The ACPL-H312 drivers were chosen for a MOSFET transistor drive.

B. Simulation Results

Our first simulation results were obtained from a case without a shoot-through station. Fig. 4 presents the results of the simulation. The simulation waveforms correspond to the operating point with 130 V input DC voltage and 130 V output AC voltage. Carrier frequency was set up to 25 kHz.

Fig. *4a* shows the input current and voltage waveforms. It can be seen that the input current has a discontinuous behavior.

The voltages across the capacitors of the ZS network are shown in Fig 4*c*. The DC-link is shown in Fig 4*b*. As it can be seen, capacitor voltages are not stable enough in order to provide a constant level of the DC-link voltage.

Voltage and current across transistor T1 are shown in Fig. 4*d*. At the same time the voltage and current across transistor T5 are shown in Fig. 4*e*. It is shown that despite the fact that transistors are on top of the different legs they are not equally loaded. This relates the modulation technique. According to the proposed algorithm, leg A is in response for output voltage sign and leg B is in response for sinusoidal waveform of output voltage. The output voltage waveforms before and after the LC-filter are shown in Fig. 4*f*. The THD of the output voltage is about 5.5%. It is evident that in this case the quality of the output voltage is not sufficient. It is because of the disbalance of the DC-link voltage caused by the uneven distribution of power consumption in the load. The moment of time with the maximum value of the output voltage corresponds to the maximum power consumption. As a result, the input current and capacitor voltage have significant fluctuations.

One of the ways to improve the quality of the output voltage is to increase passive element values. It is a regressive way. The other approach is to embed a shoot-through station that is equally distributed during the full duty cycle. This modulation technique was developed specially for our study purposes.

Our second simulation results were obtained from a case with a shoot-through station. Fig. 5 represents the similar results of the simulation that correspond to the operating point with 130 V input voltage and 160 V output AC voltage. The shoot-through duty cycle D_s=0.16 has the same carrier frequency. It is evident that the input current is closer to a continuous mode. It should be noted that the amplitude of the current has slightly decreased. As it can be seen, capacitor voltages are more stable as compared to the previous case. As a result, the THD of the output voltage has improved up to 1.5%.

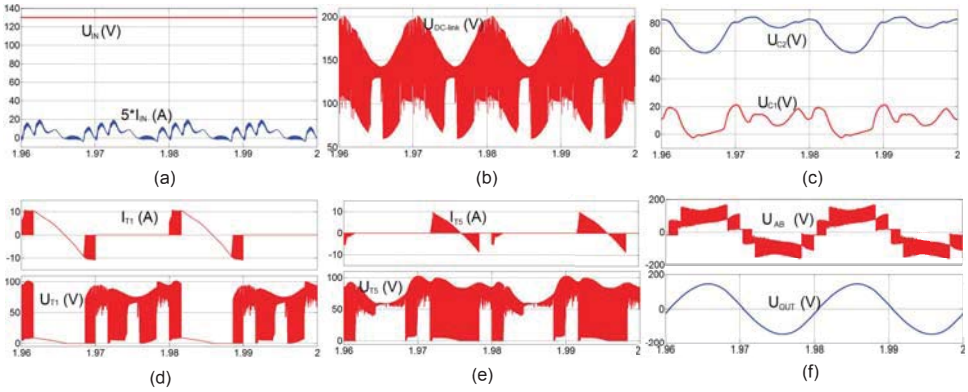


Fig. 4. Simulation results of NPC qZSI without shoot-through states.

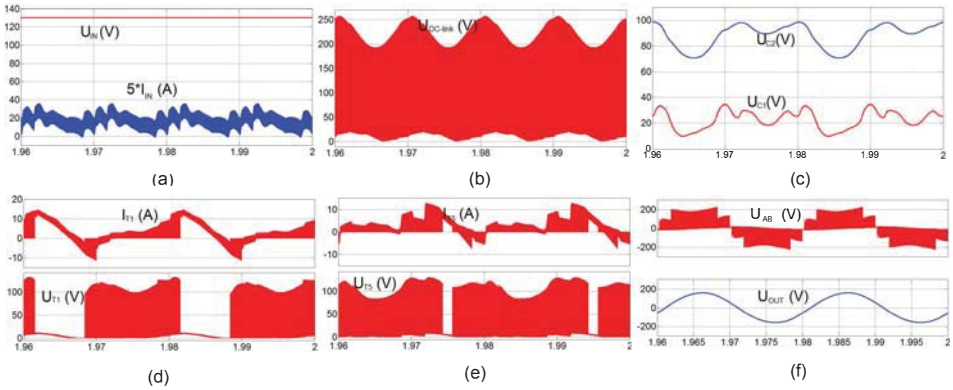


Fig. 5. Simulation results of NPC qZSI with the shoot-through duty cycle D_s=0.16.

In the further investigation, focus was on the simulation study of dependences between the shoot-through duty cycle versus the output voltage quality (THD) and the boost capability (B), shown in Fig. 6.

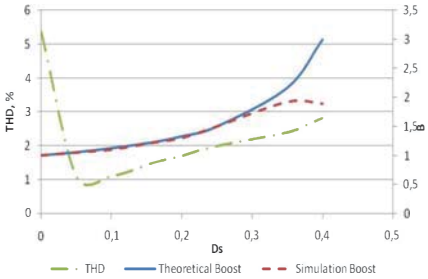


Fig. 6. Simulation results of the shoot-through duty cycle D_s versus THD and the boost capability B.

From Fig. 6 it is evident that there are some optimal operation points with the highest output voltage quality and the maximum boost factor. The highest output voltage quality was achieved with D_S equal to 0.05 and the maximum boost factor was obtained with D_S equal to 0.35. Also, from Fig. 6 it is evident that the behavior of the boost factor is similar to the theoretically estimated value Eq. (4), especially in the domain with a low shoot-through duty cycle value. Differences in the quantities are connected to the losses in the components and the discontinuous current mode that is a common tendency with the qZS family converters.

C. *Experimental Results*

To verify the proposed modulation technique and the results of the simulation a small power laboratory prototype was assembled.

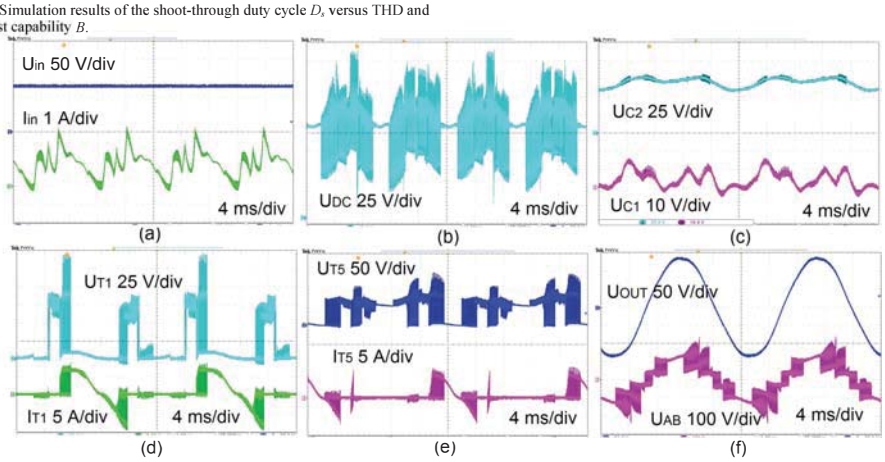


Fig. 7. Experimental results of the NPC qZSI without shoot-through states.

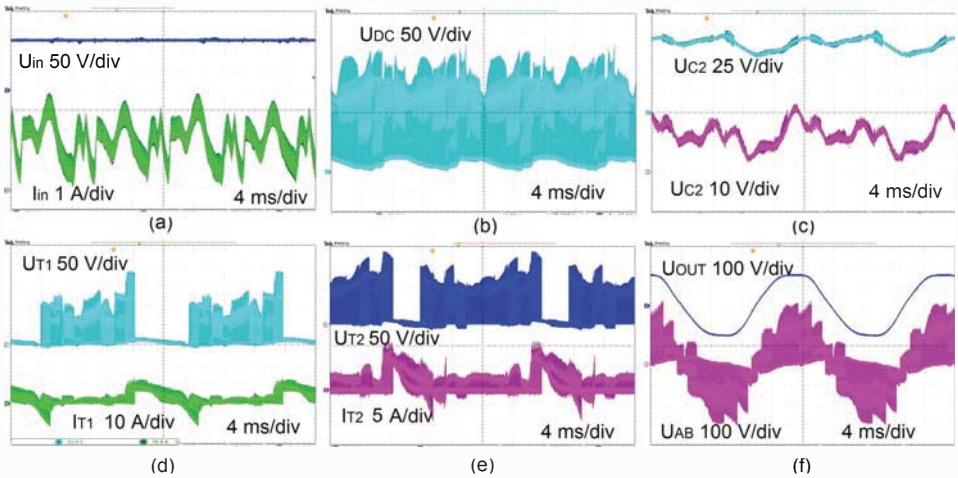


Fig. 8. Experimental results of the NPC qZSI with the shoot-through duty cycle D_s=0.16.

Experimental investigations were carried out according to the simulation. Fig. 7 presents the results of the experiment without a shoot-through station. The input current and voltage waveforms are shown in Fig. 7*a*. It is seen that the input current has significant ripple and a discontinuous behavior.

The voltages across the capacitors *C1* and *C2* of the ZS network are shown in Fig 7*c*. The capacitors *C3* and *C4* have similar voltage diagrams. The DC-link is shown in Fig 7*b*. As it can be seen, capacitor voltages are not stable enough to provide a constant level of the DC-link voltage. The voltage on the capacitor *C1* is dropping up to below zero.

Voltage and current across transistor T1 are shown in Fig. 7*d*. At the same time, the voltage and current across transistor T5 are shown in Fig. 7*e*. It is proved that despite the fact that transistors are on top of the different legs they are not equally loaded.

The output voltage waveforms before and after the LC-filter are shown in Fig. 7*f*. The THD of the output voltage is about 14%. It is evident that in this case the quality of the output voltage is not good enough.

In general, experimental results proved the expected converter behavior.

Fig. 8 represents similar results with the shoot-through duty cycle D_s=0.16.

Fig. 8*a* shows the input current and voltage waveforms. It is evident that the input current is on the boundary between the CCM and DCM. Voltage and current across transistors T1 and T5 are shown in Figs. 8*d* and 8*e*, respectively. The voltages across the capacitors of the ZS network are shown in Fig 8*c*. As can be seen, capacitor voltages are more stable than in the previous case. As a result, the THD of the output voltage is improved up to 4%. The output voltage waveforms before and after the LC-filter are shown in Fig. 8*f*.

The shoot-through duty cycle equalized the asymmetrical switching of the transistors. As a result, the behavior of the converter becomes stable and predictable. In this case, our experimental results are in good agreement with the simulation. In conclusion, it should be noted that the chosen transistor drivers that were not used before in such topologies are a good solution when the shoot-through duty cycle is present.

The diagrams presented above show that the main problem lies still in the DCM that evokes fluctuations of the input current. It is also evident that as a result of the DCM of the input current, the oscillating processes that happen in the qZS network do not evoke a constant behavior of the DC-link voltage. The DC-link voltage is significantly dropping during maximum output power consumption and rising during minimum output voltage. It has a significant influence on the quality of the output voltage that can be improved by increasing the capacitor value.

Further experimental investigation of the proposed modulation technique was carried out according to Fig. 6. Dependences between the shoot-through duty cycle versus the quality of the output voltage (THD) and the boost capability (B) are shown in Fig. 9.

It is evident that shoot-through improves the quality of the output voltage. At the same time, with a further increase of the shoot-through duty cycle boost factor *B*, a simultaneous increase occurs with THD. It is additionally illustrated in Fig. 10 where output voltages before and after the LC-filter for different D_S are shown. The best output voltage waveform is achieved with the lowest D_S. Its increase leads to the increase of the DC- link fluctuations that spoil the output voltage waveform. At the same time, it is not a drawback of the proposed modulation technique because it depends on the values of the passive components of the qZS network.

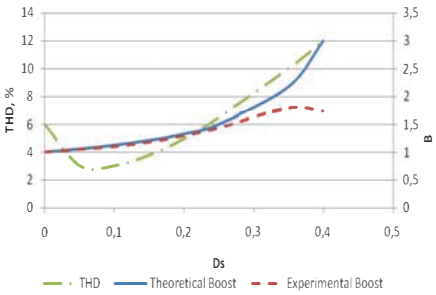


Fig. 9. Experimental results of the shoot-through duty cycle D_s versus THD and the boost capability B.

IV. CONCLUSIONS

This paper describes an NPC qZSI with a new modulation technique of the distributed shoot-through duty cycle. The theoretical and experimental results prove that the proposed modulation technique is relevant because of its ability to combine the necessary boost factor with the good quality of the output voltage.

As a result, the topology of the discussed DC/AC converter becomes more suitable for photovoltaic or fuel cell applications where controlled boost capability with a good output voltage quality are required.

Distributed shoot-through duty cycle allows balancing of the DC-link voltage and a decreasing value of passive components.

Further improvements require that the discontinuous input current mode be eliminated and DC-link voltage stabilized. A solution could be to develop a closed loop control system with an additional shoot-through duty cycle regulation capability. At the same time this problem will disappear in a three- phase system with a symmetrical load where instantaneous power consumption is constant.

Thus, the proposed modulation technique can be especially beneficial in a three-phase system.

ACKNOWLEDGEMENT

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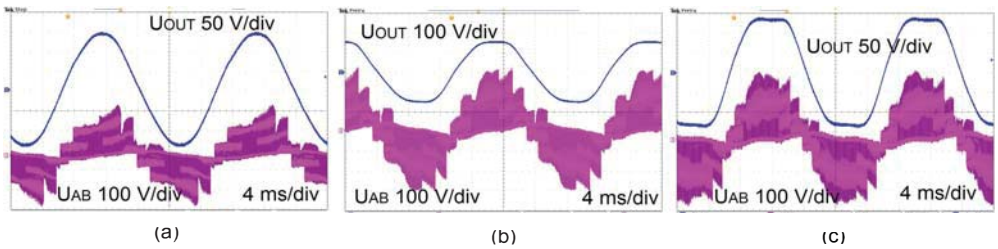

Fig. 10. Experimental output voltage waveforms with different D_S: a) D_S=0.08; b) D_S=0.16; c) D_S=0.25.

[Paper -h] Carlos Roncero Clemente, Enrique Romero Cadaval, Pedro Roncero Sánchez and Eva González Romera, *"Comparison of Two Power Flow Control Strategies for Photovoltaic Inverters"*. IEEE 38th Annual Conference of the IEEE Industrial Electronics Society, IECON 2012. Montreal (Canada). 2012.

Comparison of Two Power Flow Control Strategies for Photovoltaic Inverters

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***Abstract*- High penetration levels of distributed photovoltaic inverters on electrical distribution grids and due to the main points demanded in the latest issues of grid codes such as the reactive power injection during transient grid faults (voltage sags) and their disconnection in order to avoid the islanding phenomena, a suitable control algorithm combination is needed to provide an optimum operation at the electrical grids where they are connected, improving the power quality and the power supply continuity. This paper is devoted to the comparison through simulation of two power flow control strategies for 100 kW photovoltaic inverters in order to analyze the advantages and disadvantages of each one. The first one is based on the modulation index and the disphase controls of the reference signal face to the point of common coupling voltage. The second one is based on a synchronous reference frame with the voltage at the point of common coupling using i_d and i_q current component controllers.**

***Keywords* – Pulse width modulation inverter, PI control, Photovoltaic cells, Power system, Generators, Power conversion, Solar energy, Load flow control.**

I. INTRODUCTION

Photovoltaic solar energy is one of the most relevant distributed energy resources taking an important part in this new scenario [1].

This fact presents several challenges and opportunities for the electrical companies [2] that try to achieve an optimum operation control of their grids in order to improve the power quality and to assure the power supply continuity.

Due to these high penetration levels of photovoltaic plants and their inverters, new regulations [3] have been established. These regulations have as main deal that these inverters work providing support and stability during grid fault events and the necessity of injected reactive power in order to restore the voltage at the point of common coupling (PCC) should be noted when voltage sag occurs.

Another important aspect is the anti-islanding algorithms that the inverters have incorporated in order to disconnect the photovoltaic plant when a grid fault occurs and prevent several damages. The low effectiveness of these algorithms in multi-inverter environments [4] must to be taken into account to achieve suitable control algorithms for the actual situation.

This paper is devoted to simulation study of two power flow control strategies in order to photovoltaic inverters could generate the suitable active or reactive power. The first strategy is based on controlling active and reactive power through the modulation index and the disphase of the reference signals. The second one is based on using a synchronous reference frame with the voltage at the point of common coupling through controlling i_d and i_q current components in order to inject the desired active or reactive power.

Firstly, the description of the studied system using PSCAD/EMTDC [5] as simulation tool will be shown. After that, the analysis, explanation and simulation of two power control techniques will be exposed and finally, each technique have been studied and evaluated in order to show the advantages, disadvantages and capabilities to achieve all the demanded performances.

II. GRID-CONNECTED PHOTOVOLTAIC SYSTEM DESCRIPTION

Fig. 1 shows the grid-connected photovoltaic system scheme. All of the different stages will be explained below.

A. Solar Array Model

Several models have been proposed for solar panel simulation [6]-[10]. Most of them model the solar cell as an electrical equivalent circuit and some parameters are needed such as: junction resistor between P-N unions, the contact resistor between cells and metal parts (R_s) and the resistor for shunt currents (R_{sh}). In [6]-[8], even the diode factor and the effective cell area are necessaries.

Due to these parameters are not providing by the solar panel manufacturers in datasheets, the use of these models are difficult for the engineers and users. Because of that, a model based on I-V exponential curve [11] has been used for this simulation study. This curve is provided in datasheets, and the model only need the curve and the parameters V_{oc}, I_{sc}, I_{MPP}, V_{MPP}, which are defined in Table I. The influence of temperature and irradiance over them is considered and its information is also provided by the manufacturers [11].

The expressions and equations that describe this model based on I-V exponential curve are detailed in [11] and the simulated I-V and P-V curves of Shell SP 150-P [12] solar panel are shown in Fig. 2 and Fig. 3, respectively. The values of V_{oc}, I_{sc}, I_{MPP} and V_{MPP} have been achieved with an error less than 1%. With a suitable series-parallel association, the photovoltaic system DC voltage and the power of the plant can be achieved. In this study, a 100 kW photovoltaic plant has been simulated and all of the parameters in standard conditions are shown in Table I.

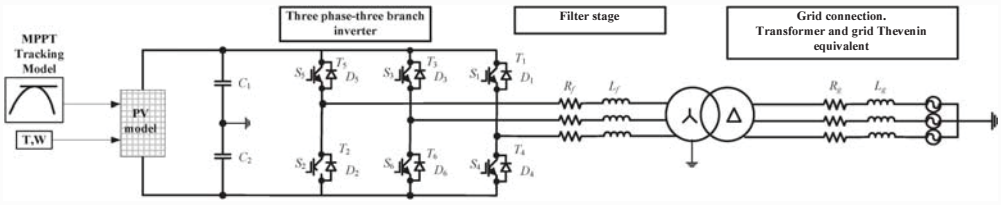

Fig. 1. Grid-connected photovoltaic system scheme.

TABLE I. PHOTOVOLTAIC PLANT PARAMETERS

Parameter	Description	Value
V_{oc}	Open circuit voltage (V)	43.4
I_{sc}	Short circuit current (A)	4.8
I_{MPP}	Maximum power point current (A)	4.4
V_{MPP}	Maximum power point voltage (V)	34
N_S	Series connected panel	34
N_p	Parallel connected panel	20
U_{DC}	Maximum power point DC voltage (V)	1156
S_{MAX}	Maximum power (kW)	101
$U_{DC,MAX}$	Maximum DC voltage (V)	1475.6

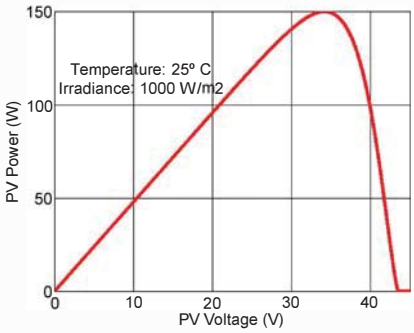

Fig. 3. P-V curve.

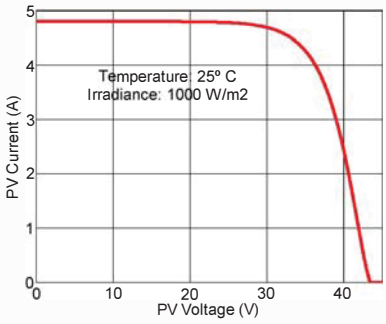

Fig. 2. I-V curve.

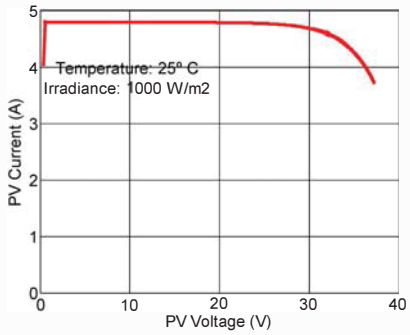

Fig. 4. MPP tracking. I-V curve.

B. *Maximum Power Point Tracking (MPPT)*

Due to the high cost of the solar panels, the maximum power point (*MPP*) operation is necessary. Power depends of the temperature (*T*) and irradiance (*W*) and the *MPP* must be tracked.

Three MPPT algorithms are emphasized due to their capabilities: perturb and observe (P&O), incremental conductance [13] (InC) and methods based on *dP/dV* or *dP/dI* controls. *dP/dI* method has been used in this study on account of different characteristics such as: simple structure, low value of measured variables that are needed, convergence speed, etc. The slope of the P-V curve is calculated using this method and the inverter is feed back in order to adjust the inverter duty cycle and the *MPP* could be reached. The photovoltaic plant work region using this algorithm is shown in Fig. 4 and Fig. 5. In [14], the implementation using Simulink/Matlab is detailed.

C. *Three-Phase Three-Branch Inverter*

A 100 kW three-phase three-branch inverter injects the produced solar energy into the electrical grid. The DC bus middle point is connected to the ground. Capacitors demand the solar array energy fluctuation and their value are 15 mF.

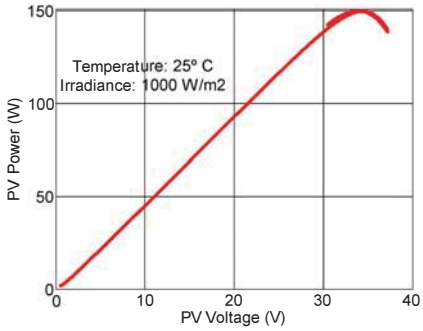

Fig. 5. MPP tracking. P-V curve.

The IGBTs switching signal generation of each branch and the reactive power controls will be explained in Section III.

D. Filter Stage

Inductor filter has been calculated according to [15] and current ripple, fast and control criteria have been considered. The filter inductor value is 500 µH.

E. Grid connection. Transformer and Grid Thevenin equivalent.

Photovoltaic inverter is connected to the grid through an elevator transformer and the electrical grid has been modelled as Thevenin equivalent. Table II shows the parameters used to simulate these elements.

III. Active and Reactive Power Control Strategy Based on Modulation Index and Phase Angle

A. Synchronous Generator Equations:

In traditional power systems, active and reactive power flows are controlled using high power synchronous generators. Generated active power by means of a cylindrical rotor synchronous generator is (1):

TABLE II. GRID CONNECTION SIMULATION PARAMETERS

Grid equivalent Thevenin	RMS Voltage: U^{L-L}	20 kV
	Short-circuit power: *Scc*	2 MVA
	Frequency: *f*	50 Hz
Power transformer	Nominal power: S_n	250 KVA
	Nominal winding voltages	0.4/20 kV
	Positive secuence reactance: X_d	0.04 pu
	Open circuit losses	0.003 pu
	Copper losses	0.005 pu

$$P_G = \frac{U_{gen} U_g}{X_S} \sin\delta, \tag{1}$$

where P_G is the generated active power by means of a synchronous generator, U_{gen} is the line to neutral synchronous generator voltage, U_g is the line to neutral grid voltage, X_s is the synchronous reactance, δ is the angle between U_{gen} and U_g. Reactive power is given by (2):

$$Q_G = \frac{U_g (U_{gen} \cos\delta - U_g)}{X_S}. \tag{2}$$

If we taking on that δ angle is closed to zero, equations (1) and (2) are transformed in (3) and (4):

$$P_G = \frac{U_{gen} U_g}{X_S} \delta, \tag{3}$$

$$Q_G = \frac{U_g U_{gen} - U_g^2}{X_S}. \tag{4}$$

Therefore, the control variables are (5) and (6):

$$P_G = P_G(U_{gen}, \delta), \tag{5}$$

$$Q_G = Q_G(U_{gen}). \tag{6}$$

B. Three-phase Inverter Equations

The RMS line-to-neutral voltage in a three-phase inverter is given by (7):

$$U_{L-N} = m \frac{U_{DC}}{2\sqrt{2}}, \tag{7}$$

where *m* is the reference voltage modulation index. The control variable is shown in (8):

$$U_{L-N} = U_{L-N}(m). \tag{8}$$

Using expressions (5), (6), (7) and (8) as well as $U_{L-N} = U_{gen}$, the relationships (9) and (10) are obtained:

$$P_G = P_G(m, \delta), \tag{9}$$

$$Q_G = Q_G(m), \tag{10}$$

where δ represent the disphase between sinusoidal pulse width modulation (SPWM) reference and the voltage in point of common coupling (PCC).

C. Proportional-Integral Controllers

In order to adjust the injected active and reactive powers by the three-phase inverter by means of control variables *m* and δ of the SPWM, Proportional-Integral controllers have been used. In Fig. 6 we can see a sketch of the control system.

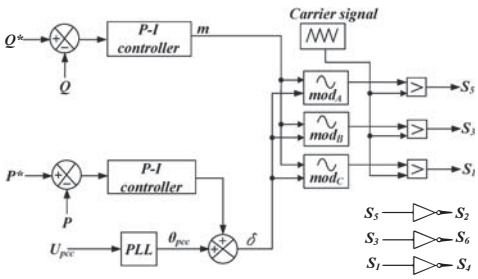

Fig. 6. P-Q control scheme by means of modulation index and δ.

IV. Active and Reactive Power Control Based on I_D and I_Q Controls

A. Grid Connected System Model

Fig. 7 shows a single-phase grid connected system sketch. The inverter has been modelled as an ideal sinusoidal voltage source *u,* and *r* and *L* represent the resistance and inductor of the output filter. Due to the system is a three-phase three-wire inverter, sums of phase currents and zero sequence components are zero.

This system could be represented as state-space model as (11):

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -r/L & 0 & 0 \\ 0 & -r/L & 0 \\ 0 & 0 & -r/L \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/L \end{bmatrix}\begin{bmatrix} e_a - v_a \\ e_b - v_b \\ e_c - v_c \end{bmatrix}, \quad (11)$$

where e_a, e_b and e_c are the line-to-neutral inverter voltages, v_a, v_b and v_c are the line-to-neutral grid voltages and i_a, i_b and i_c are the line currents respectively.

B. Continuous Time State Equations to Control Active and Reactive Power

In order to control the injected instantaneous active and reactive power by the photovoltaic inverter using this control strategy, Park transformation has been used [16] as well as synchronous reference frame (*d-q*) with the grid voltage vector ($\vec{v}$) [17]. If the reference frame (*d-q*) has the same frequency than the grid frequency ($\omega_c = \omega_{red}$) and the *d* axis is aligned with the grid vector voltage, the *q* component will be zero. By this way, the expressed variables in *a, b, c* frame are transformed in (12), (13) and (14), and the grid voltage is synchronous and in quadrature with them:

$$\vec{i} = i_d + j i_q \quad (12)$$

$$\vec{e} = e_d + j e_q \quad (13)$$

$$\vec{v} = v_d . \quad (14)$$

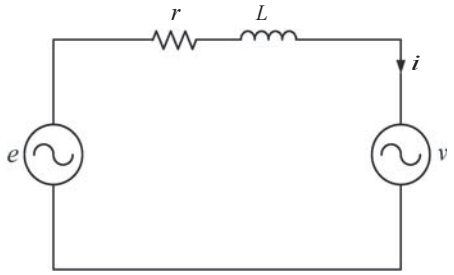

Fig. 7. Grid-connected single-phase inverter sketch.

After that the space transformation, model (11) could be expressed as (15), where active and reactive powers are expressed as (16) (17) [18]:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -r/L & \omega_{red} \\ -\omega_{red} & -r/L \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/L \end{bmatrix}\begin{bmatrix} e_d - v_d \\ e_q \end{bmatrix} \quad (15)$$

$$p = v_d i_d \quad (16)$$

$$q = -v_d i_q . \quad (17)$$

Therefore, if the space grid voltage vector ($\vec{v}$) is known, active and reactive power control can be achieved through current components at *d-q* frame.

C. Control System Design in Continuous Time

In the modeled system in equation (15) i_d, i_q are the state variables, e_d, e_q are the input variables and v_d is disturbance that could be measured. Equation (15) can be divided in (18) (19):

$$\frac{di_d}{dt} = -\frac{r}{L} i_d + u_d , \quad (18)$$

$$\frac{di_q}{dt} = -\frac{r}{L} i_q + u_q , \quad (19)$$

where u_d, u_q are independent variables in order to control i_d and i_q respectively.

e_d and e_q are represented in (20) as a function of the independent variables (u_d, u_q) and the state variables (i_d,i_q):

$$\begin{bmatrix} e_d \\ e_q \end{bmatrix} = B^{-1}\begin{bmatrix} u_d \\ u_q \end{bmatrix} - B^{-1} A \begin{bmatrix} i_d \\ i_q \end{bmatrix}, \quad (20)$$

where *A*, *B* matrixes are defined as (21) (22):

$$A = \begin{bmatrix} 0 & \omega_{red} \\ -\omega_{red} & 0 \end{bmatrix}, \quad (21)$$

$$B = \begin{bmatrix} 1/L & 0 \\ 0 & 1/L \end{bmatrix}. \quad (22)$$

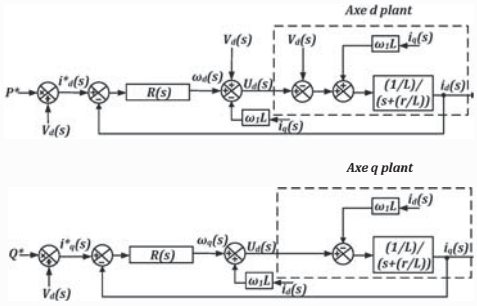

Fig. 8. *d-q* axes control sketch.

Equation (20) has been used as control equation in the system control as Fig. 8 shows. In this paper, a state feedback control has been used through proportional-integral controllers on i_d and i_q currents [18]. A study of the closed-loop system has been developed in order to tune the controllers and a quickly response has been looked for.

V. SIMULATION RESULTS

The injected active power by the grid-connected three-phase photovoltaic inverter using each control strategy is shown in Fig. 9 and Fig. 10 respectively. Reference active power in both cases is: from 0.05 s to 1.5 is 100 kW, from 1.5 s to 3 s is 50 kW and after that system is returned to the initial state. Using the first strategy, we obtain 25 % as maximum peak (M_p) and with the second one, only a 7% as maximum peak is obtained. Time to reach the steady state (t_s) is 0.5 s and 0.15 s using each control strategy respectively. Because of that, the time response is better in the second case.

Fig 11 and Fig. 12 show the injected reactive power by the grid-connected three-phase photovoltaic inverter in each case with a reference reactive power is from 1.5 s to 3 s of 50 kVAr and zero the rest time assuring equation (22):

$$Q \leq \sqrt{S^2 - P^2}\,. \tag{23}$$

A better time response is again obtained using the second strategy whit lesser t_s (0.03 s face to 1 s) in comparison with the first strategy. Also in Fig. 13 and Fig. 14 we can see the evolution of all the control variables in both cases.

VI. CONCLUSIONS

Two controls strategies to control active and reactive power by a three-phase photovoltaic inverter have been described and compared by simulation in this paper.

The first strategy is based on modulation index and δ angle controls, while the second one is based on using a synchronous reference frame (*d-q*) with the grid voltage vector ($\vec{v}$) and i_d-i_q controls. Better time response using the second strategy has been demonstrated by simulation. It is due to first strategy is based on steady-state equations and it is not possible develop the control design for any method and controllers have to be tuning using try-error methods.

Furthermore, as it is shown in equation (9) and (10), *P-Q* controls are not independent and it causes a slower response.

On the other hand, dynamic models that allow control designs are possible using the second strategy and faster and more stables responses are obtained. Also an independent *P-Q* control is achieved using this method.

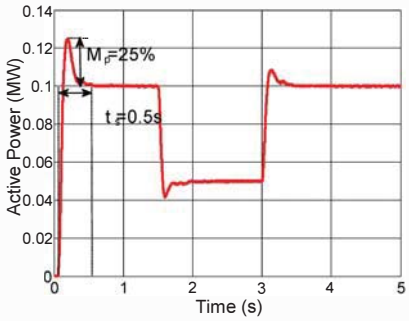

Fig. 9. Injected active power using control strategy based on modulation index and δ controls .

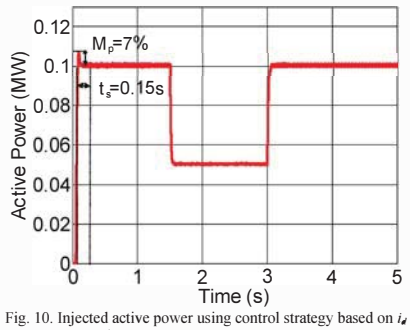

Fig. 10. Injected active power using control strategy based on i_d and i_q current controls.

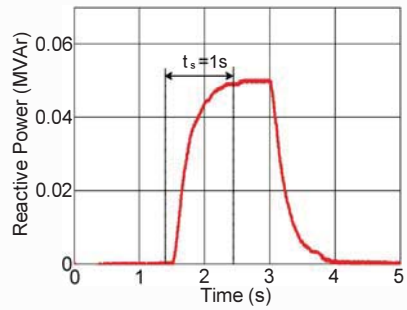

Fig. 11. Injected reactive power using control strategy based on modulation index and δ controls .

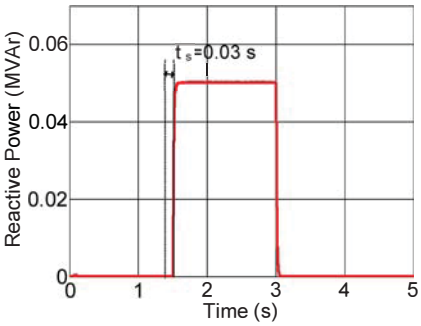

Fig. 12. Injected reactive power using control strategy based on i_d and i_q current controls.

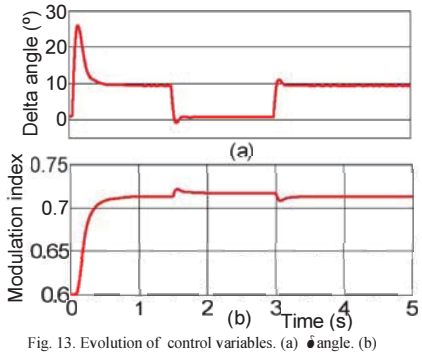

Fig. 13. Evolution of control variables. (a) δ angle. (b) Modulation index.

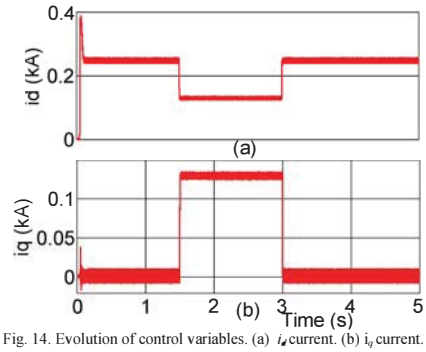

Fig. 14. Evolution of control variables. (a) i_d current. (b) i_q current.

Nevertheless, faster methods as the second one presented could cause damaging transient effects into the grid that they are connected as transient overvoltages [19] and making difficult the flow power control by the electrical companies. Because of that, the use of the first presented method could be interesting due to the slower behavior of this strategy.

ACKNOWLEDGMENT

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[Paper -i] Carlos Roncero-Clemente, Enrique Romero-Cadaval, Oleksandr Husev, Dmitri Vinnikov and Serhii Stepenko, *"Grid-Connected PV System Based on a Single-Phase Three-Level qZS Inverter"*. IEEE 39th Annual Confer-ence of the IEEE Industrial Electronics Society, IECON 2013. Vienna (Austria). 2013.

Grid-Connected PV System Based on a Single-Phase Three-Level qZS Inverter

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***Abstract*— This paper describes the operation of a grid-connected PV system based on a single-phase 3L-NPC qZSI using PSCAD as simulation tool for modelling the system: PV array, single-phase 3L-NPC qZSI, filter stage and electrical grid. The control system considers a maximum power point tracking algorithm, a phase loop locked for synchronization with the grid voltage, a control strategy to inject current in phase with the voltage at the point of common coupling and the modulation technique that also take into account shoot-through duty cycle. Simulation results are provided in order to show the viability of using this topology for PV energy systems connected to the electrical grid.**

Keywords—Photovoltaic systems; PSCAD; Pulse width modulation converters; Power system simulation.

I. INTRODUCTION

Several factors such as an electrical consumption increase, the electrical market liberalization, the need to reduce CO_2 emissions and the new technological development are boosting the distributed generation (GD) with renewable energies. Photovoltaic solar energy is one of the most relevant renewable distributed energy sources [1], as a consequence, in many cases, of profitable incentive policies. R&D activities focus on improving the efficiency, profitability and the manufacture of photovoltaic (PV) equipment and systems. This includes the development of solar cells no longer based on multi-or-single crystalline silicon, PV modules including building-integrated PV modules and PV inverters among others.

PV industry aims to reduce the cost associated with PV inverters by increasing the overall performance. In order to achieve its goal, innovative ideas in terms of circuit topologies and control solutions are carried out. At the same time current trend in multilevel inverter topologies [2] indicates the preference of using multiple numbers of power devices of smaller rating instead of one device of large rating with has as consequences higher power quality, higher voltage capability, better electromagnetic compatibility and lower switching losses among others. Also new industry applications for multilevel inverters are emerging, in particular, for interfacing renewable energy sources.

Solar energy production is well known that depends of solar irradiance (W) and temperature (T). Unfavorable conditions of these variable parameters generate a low value of the DC-link voltage which causes a worse working point, reducing the effectiveness of the solar energy use due to control strategies involved in the PV traditional inverter topologies. Because of that a DC/DC boost converter [3] should be used in the input stage increasing the complexity of the system and reducing the overall performance.

Z-Source Inverter (ZSI) [4] and quasi-Z-Source Inverters (qZSI) [5] have been proposed to compensate this situation due to its boosting capabilities. qZSI inherits the advantages provided by ZSI and also gets smaller passive component rating and continuous input current mode.

The modern Three-Level Neutral-Point-Clamped quasi-Z-Source Inverter (3L-NPC qZSI) topology proposed in [6] has both advantages of multilevel and qZS topologies which make it especially suitable for PV applications. Due to 3L-NPC qZSI topology is rather recent, it has only been analyzed in not-grid-connected electrical systems and it is necessary to study a wide range of aspects: synchronization with the grid voltage, maximum power point tracking (MPPT), anti-islanding detection and reactive power control when this topology is working connected to the electrical grid. Some of these matters are prescribed by regulations.

This paper describes the operation of a grid-connected PV system based on a single-phase 3L-NPC qZSI using PSCAD as simulation tool. The descriptions of the different implemented systems such as: PV panel model, MPPT algorithm, synchronization with grid voltage, control strategy to generate the reference signal and modulation technique (with shoot-through duty cycle (D_s)). Simulation results are also provided in order to show the viability of using this topology for PV energy systems connected to the electrical grid.

II. DESCRIPTION OF THE MODEL

Fig. 1 depicts the power stage of the modeled grid-connected PV system based on a single-phase 3L-NPC qZSI. PV panel array is feeding a 3L-NPC qZSI that injects current into the electrical grid considered it as Thevenin equivalent. The output filter is an inductance in series which includes the effects from transformer and grid impedance in order to simplify the simulation study.

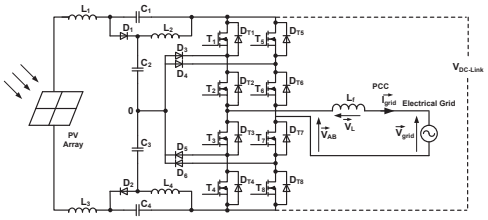


Fig. 1. Power stage of the grid-connected PV system based on a single-phase 3L-NPC qZSI.

The inductor filter has been calculated according to [7] taking into consideration current ripple, rapidity and control possibility guidelines.

Following section describes each element of the PV system based on a single-phase 3L-NPC qZSI both power stage and control stage being modeled.

A. PV Array Model

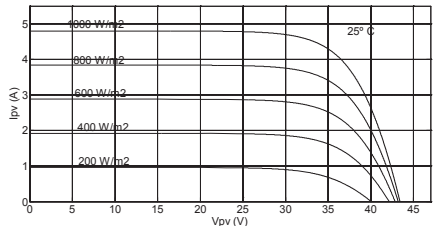
The behavior of solar panels is well-known. They provide a limited voltage and current following an exponential I-V curve. Designing simulation models for PV modules is a very useful but not easy task to deal with studies regarding PV plants such as integration to the grid, designing control strategies for inverters, analysis of new inverter topologies, etc.

Several models have been proposed for PV panel simulation. Most of them model each solar cell as equivalent circuit, which consists of a current source anti-parallel with a diode, a shunt resistance and a series resistance. Such model is widely used in research works and in commercial simulation software (for instance in PSCAD library), however, it has the disadvantage of requiring unknown parameters, as series and shunt resistances even the diode factor which are not provided by manufacturers [8]. Due to this disadvantage for users and engineers, a mathematical PV model based on the exponential I-V curve has been chosen for this work. This math model follows the equation (1):

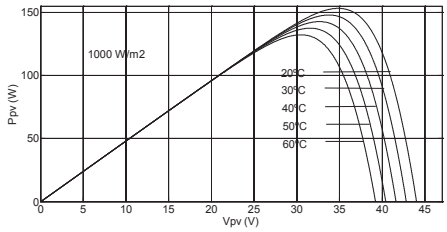
$$I_{pv,TW} = I_{sc,TW}\left(1 - B_1 \cdot e^{\frac{V_{pv,TW} - V_{oc,TW}}{\tau_1}} - B_2 \cdot e^{\frac{V_{pv,TW} - V_{oc,TW}}{\tau_2}}\right) \quad (1)$$

where $I_{pv,TW}$ and $I_{sc,TW}$ are the current and short-circuit current provided by the PV panel in specific conditions of W and T. $V_{pv,TW}$ and $V_{oc,TW}$ are the voltage and open-circuit voltage provided by the PV panel in specific conditions of W and T as well. The parameters B_1, B_2, τ_1 and τ_2 have as goal to reproduce the exponential shape of one specific panel curve in different condition with high accuracy, where these parameters are obtained only from manufacturer specifications in typical datasheets. Mathematical foundation is detailed in [9].

The obtained I-V and P-V family curves of panel Shell SP150-P in different T and W conditions after implementation and modeling in PSCAD are showed in Fig. 2 (a) and Fig. 2 (b) respectively. For this simulation study the PV array configuration is composed by 4 strings of 20 panels.



(a)



(b)

Fig. 2. (a) I-V curves in different conditions of W. (b) P-V curves in different conditions of T.

B. MPPT algorithm

Tracking the MPP of a PV array is necessary due to the high cost of solar panels being an essential task of PV inverters. In this way, many MPPT algorithms have been proposed in the literature [10]. Those methods vary in complexity of implementation, sensors required, convergence speed, cost, range of effectiveness and hardware implementation among others [10].

Three MPPT algorithms are emphasized due to their capabilities: perturb and observe (P&O), incremental conductance (InC) and method based on *DP/dV* or *dP/dI* feedback, being some of the most traditional. P&O has been used for this modeling study for several reasons: it has a simple structure which allows an easy implementation, only two sensors are needed (to measure I_{pv} and V_{pv}) and it can be used for digital or analogical systems among others.

The explanation of this method is as follows [10]: a perturbation is involved in the reference current of the PV array (I^*_{pv}) which causes a perturbation in the V_{pv} and subsequent the PV array power (P_{pv}) is modified. By means of the increment of the I^*_{pv} when the operation is on the left of the MPP, the P_{pv} is decreased and the P_{pv} is increased if the operation is on the right of the MPP. The same reasoning is possible when the I^*_{pv} is decreased.

It should be noted that other variables could be used to produce the perturbation on the P_{pv} such as V^*_{pv} or shoot-through duty cycle (D^*_s). If one perturbation in one direction produce and increment of the P_{pv}, next perturbation should be in the same direction and if it does not occur, the perturbation

TABLE I
SUMMARY OF MPPT ALGORITHM BASED ON P&O

Perturbation	Change in Power	Next Perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

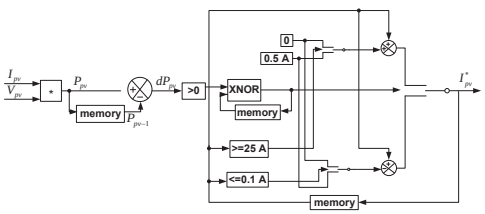


Fig. 3. Implementation scheme of MPPT based on P&O in the modeling process.

has to be reverse. In Table I the aforementioned process is summarized.

In our case of modelling we have chosen I^*_{pv} to produce the perturbation on P_{pv} and the implementation scheme used in PSCAD is depicted in Fig.3. The process summarized in Table I is easily carried out using a XNOR gate and also two I^*_{pv} limits have been inserted in order to avoid convergence problems. In our PV array configuration where the I_{pv} at the MPP is 17.6 A (4 panel in parallel) at standard condition, the upper limit is 25 A and the lower limit is 0.1 A. The perturbation size is 0.5 A bringing to the system towards an operation point near to the MPP as Fig. 4 shows. Due to this reason some amount of energy is wasted [11] but, some papers propose methods to improve the performance using adaptative perturbation sizes.

C. Control Strategy. Reference Generation

The goal of this simulation study regarding injecting power into the grid is carrying it out with unitary power factor, that is, injecting a sinusoidal current in phase with the voltage at the point of common coupling (PCC). It will be achieved by means of controlling the output voltage between branches of the 3L-NPC qZSI.

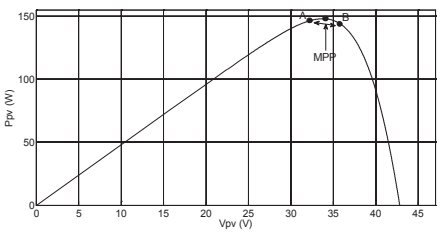


Fig. 4. Operation of MPPT based on P&O.

First of all it is necessary to perform a power balance between DC and AC sides to obtain the injected RMS reference current (I^*_{grid}) into the grid. This is carried out by means of (2):

$$I^*_{pv} V_{pv} = I^*_{grid} V_{grid} \,. \tag{2}$$

To explain the control strategy and generate the reference to be tracked is necessary to consider the variables defined in Table II. To realize a more precise approach, we will take into account the resistance of the filter inductance (R_f). The filter inductance (L_f) which includes the impedances of transformer and grid is considered as constant to simplify the study.

Such variables are represented in the equivalent scheme of the output filter (Fig. 5 (a)) and its vector diagram in a *d-q* frame (Fig. 5 (b)). The *d* component of this frame will be synchronized with the voltage at the PCC.

According to the vectors diagram from Fig. 5 (b) one has (2):

$$\vec{V}^*_{AB} = \vec{V}_{grid} + \vec{V}^*_R + \vec{V}^*_L \tag{2}$$

that could be expressed in a *d-q* frame as (3):

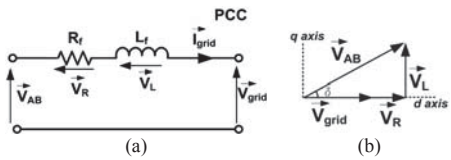
$$\vec{V}^*_{AB} = V_{grid}\vec{u}_d + V^*_R\vec{u}_d + V^*_L\vec{u}_q \tag{3}$$

where $\vec{u}_d$ and $\vec{u}_d$ are unitary vectors in the *d* and *q* directions.

To obtain the unitary vectors, a phase locked loop (PLL) is required. In this work, the PLL available in PSCAD simulation tool library has been used. It generates a ramp

TABLE II
RELEVANT VARIABLES INVOLVED IN THE CONTROL STRATEGY

Variable	Description
$\vec{V}^*_{AB}$	Reference output voltage vector of the fundamental component in terminals of the 3L-NPC qZSI. Voltage between branches.
$\vec{V}^*_L$	Reference voltage drop vector in the filter inductance.
$\vec{V}^*_R$	Reference voltage drop vector in the resistance of the filter inductance.
$\vec{I}^*_{grid}$	Reference injected current vector to the grid.
$\vec{V}_{grid}$	Voltage grid vector. Voltage at the PCC.



(a) (b)

Fig. 5. (a) PCC equivalent scheme. (b) Vectors diagram.

signal (θ) which varies between 0° and 360°, synchronized or locked in phase with the instantaneous voltage at the PCC $v_{grid}(t)$.

The RMS value of $\vec{V}^*_{AB}$ can be calculated as (4):

$$V^*_{AB} = \sqrt{(V_{grid} + V^*_R)^2 + (V^*_L)^2} \tag{4}$$

where voltages V_{grid} is RMS value of voltage at PCC, V^*_R and V^*_L are RMS values of the references voltages of $\vec{V}^*_R$ and $\vec{V}^*_L$, voltage drop at the filter resistance and inductance respectively.

At the same time, peak value of V^*_{AB} is related to the modulation index (m) and the DC-link voltage ($V_{DC\text{-}LINK}$) by (5):

$$m = \frac{\sqrt{2}V^*_{AB}}{V_{DC-LINK}} \tag{5}$$

and if m is expressed as (6) one has:

$$m = \sqrt{2}\frac{\sqrt{(V_{grid} + I^*_{grid}R)^2 + (\omega L I^*_{grid})^2}}{V_{DC-LINK}} \tag{6}$$

where $V_{DC\text{-}LINK}$ is the measured DC-link voltage. Thus, the modulation index m has been calculated to obtain the desired amplitude of $\vec{V}^*_{AB}$ according to the vectors diagram of Fig. 6 (b).

To calculate the angle (δ) of $\vec{V}^*_{AB}$, a unitary vector in the direction of such vector is calculated as (7):

$$\vec{u} = \frac{(V_{grid} + I^*_{grid}R)\cdot\vec{u}_d + (\omega L I^*_{grid})\cdot\vec{u}_q}{\sqrt{(V_{grid} + I^*_{grid}R)^2 + (\omega L I^*_{grid})^2}}. \tag{7}$$

Thus, the unitary reference instantaneous voltage (v^*_{AB}) is generated and it will be used in the shoot-through sinusoidal pulse width modulation with the properly m and its phase $\vec{u}$.

D. Modulation Technique

There are two kinds of switching signals to generate separately in a grid-connected 3L-NPC qZSI. On one hand it is necessary to generate the normal switching signals ($S_{i,n}$) in order to track the reference signal v^*_{AB} aforementioned. On the other hand the shoot-though states (S_t) must to be added carefully in order to boost the input PV voltage (V_{pv}) when it would be necessary, for instance when W decreases.

Some requirements are demanded when shoot-through states are generated, for instance do not affect to the average output voltage and they have to be uniformly distributed during the whole output voltage period with constant width. These features produce several advantages such as minimum ripple of the input current, minimum value of the passive elements, reduction the THD of the output voltage and allow obtaining the desired boost factor.

In this simulation the modulation technique proposed in [12] has been used to achieve the aforementioned features. Fig.6 shows the implementation scheme of this modulation technique followed in PSCAD and in Fig.7 normal switching states and shoot-through states are displayed.

E. Modeling of the Power Stage

The full switching model of the 3L-NPC qZSI has been carried out in PSCAD as electrical model by adding electrical components. This kind of modelling is useful to analyse the full behaviour of the converter and all its measurements even

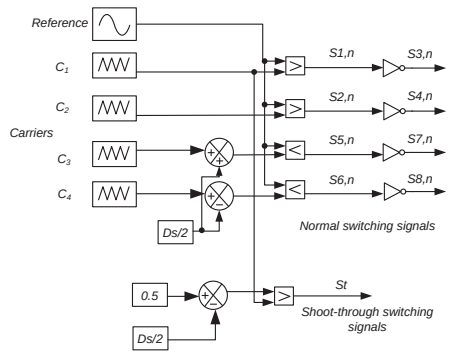


Fig. 6. Implementation sketch of the modulation technique.

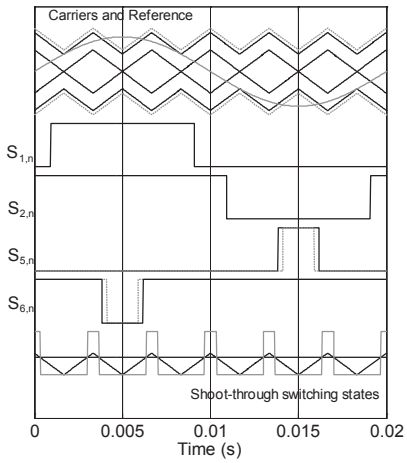


Fig. 7. Normal and shoot-through switching states.

at the expense of higher simulation times and data file sizes. However, to analyse other capabilities, an average model of the power stage could be used. Value of passive elements will be provided in next section.

III. Simulation Results

In order to validate the full system operation, a simulation study was performed. Used values in the simulation for each component of the system are showed in Table II. Values of passive elements of qZ network have been calculated according to guidelines provided in [13].

Shoot through switching states are added to the normal states in order to increase the input voltage. D_s has to assured equation (8) [14]:

$$D_s \leq 1 - m. \tag{8}$$

The minimum value of D_s is determined according to next reasoning. Voltage between terminals of an inductor is (9):

$$v_L(t) = L\frac{di(t)}{d(t)} \tag{9}$$

TABLE II
Used Values for Simulation Study

Parameter	Unit	Element	Value
Inductors L_1,L_3	(mH)	qZ network	0.29
Inductors L_2,L_4	(mH)		0.29
Capacitor C_1,C_4	(mF)		4
Capacitor C_2,C_3	(mF)		1.3
W	(W/ m^2)	PV array model	1000
T	(º C)		25
Open circuit voltage V_{oc}	(V)		43.4
Short circuit current I_{sc}	(A)		4.8
Maximum power point voltage V_{MPP}	(V)		34
Maximum power point current I_{MPP}	(A)		4.41
Panels connected in series N_s			20
Series connected in parallel N_p			4
Perturbation size ΔI^*_{pv}	(A)	MPPT algorithm	0.5
Time between perturbations	(s)		0.1
L_f	(mH)	Filter stage	4
V_{grid}	(V)	Electrical grid	230
Shoot-through duty cycle D_s		Modulation technique	0.1
Switching frequency f_{sw}	(kHz)		50

where $v_L(t)$ is the instantaneous value of the voltage in the inductance, L is the inductance value and $i(t)$ is the current across the inductance.

In our case, according to the equivalent scheme in Fig. 5 (a) it also can be obtained as (10):

$$v_L(t) = v_{AB}(t) - v_{grid}(t) \tag{10}$$

where $v_{AB}(t)$ is the instantaneous voltage between branches and $v_{grid}(t)$ is the instantaneous grid voltage.

In order to assure the control in the inductance and be able to inject the desired current for every value of $v_{grid}(t)$, equation (11) must be satisfied:

$$V_{DC-LINK} > \sqrt{2}V_{grid}. \tag{11}$$

In the 3L-NPC qZSI, expression (11) could be expressed as (13) taking into the account equation (12) [14]:

$$V_{DC-LINK} = \frac{V_{IN}}{1-2D_S}, \tag{12}$$

$$\frac{V_{IN}}{1-2D_S} > \sqrt{2}V_{grid}. \tag{13}$$

Operating with equation (13) we can obtain expression (14):

$$D_S > \frac{1}{2} - \frac{V_{IN}}{2\sqrt{2}V_{grid}}, \tag{14}$$

which assures that the injected current control can be carried out successfully.

In Fig. 8 we can see the I^*_{pv} provided by the MPPT which reach the steady state after connection of the inverter to the grid at second 5. I^*_{pv} reaches the proper value according to I_{MPP} per panel and four series connected in parallel.

Fig. 9 depicts $v_{DC-LINK}$ where a pulsation at 100 Hz can be appreciated due to the single phase power system. Also, $v_{DC-LINK}$ is going to zero during the whole period. In Fig. 10 we can see instantaneous voltage between branches v_{AB}.

In Fig. 11 the injected current in phase with the voltage at the PCC are showed. It can be appreciated a proper

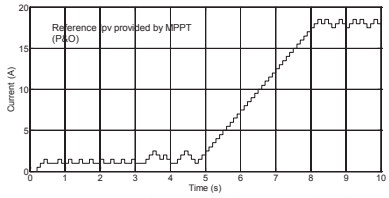


Fig. 8. Reference current obtained by the MPPT algorithm based on P&O.

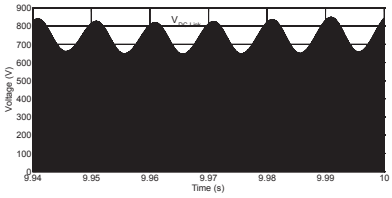


Fig. 9. DC-Link voltage ($v_{DC\text{-}LINK}$).

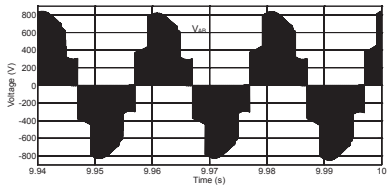


Fig. 10. Voltage between branches (v_{AB}).

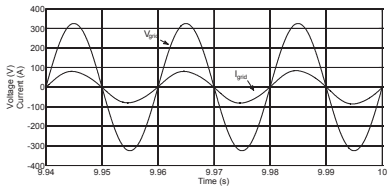


Fig. 11. Output current and voltage at PCC.

synchronization between both signals. Finally, in Fig. 12 the evolution of the control variable *m* is represented. Once the PV system has reached the steady state, *m* is near to 0.8 which accomplish equation (8).

IV. Conclusions

In this paper, a grid-connected PV system based on a single phase 3L-NPC qZSI has been simulated by means of PSCAD. The model includes the PV array, MPPT algorithm, single phase 3L-NPC qZSI with an inductance filter, phase locked loop for synchronization with electrical grid, control strategy to inject current in phase with the voltage at the PCC and the modulation technique including shoot-through states. The proper operation of such model has been demonstrated by simulation of a 12 kW PV system.

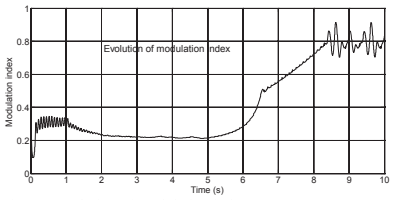


Fig. 12. Evolution of modulation index *m*.

Also a guideline to calculate the minimum value of D_s that assures the proper control of the injected current has been proposed.

Acknowledgment

This research work has been supported by "Ministerio de Economía y Competividad", "Fondos FEDER", "Junta de Extremadura", "Consejería de Empleo, Empresa e Innovación" and "Fondo Social Europeo". The work has been developed under the Project SIDER (TEC2010-19242-C03) and the grant BES-2011-043390. This study was also co-financed by Estonian Ministry of Education and Research (projects SF0140016s11 and B23) and by Estonian Research Council (Grant G8538).

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[Paper -j] Carlos Roncero-Clemente, Oleksandr Husev, Enrique Romero-Cadaval and Dmitri Vinnikov, *"P and Q Control Strategy for Single Phase Z/qZ Source Inverter Based on d-q Frame"*. 23rd IEEE International Symposium on Industrial Electronics, ISIE 2014. Estambul (Turkey). 2014.

P and Q Control Strategy for Single Phase Z/qZ Source Inverter Based on *d-q* Frame

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***Abstract*—This paper explains a new control strategy for controlling active and reactive powers in a single phase Z or qZ source inverter to increase the active functions of these converters when they are interfacing with distributed energy resources. The proposed strategy is based on a *d-q* synchronous reference frame and it is validated by simulation in a single phase three-level neutral-point-clamped topology. Both steady and transient states are studied under different conditions.**

Keywords—power electronic converters; power control; distributed power generation; power system simulation

I. INTRODUCTION

High-penetration levels of distributed inverters on an electrical distribution grid present changes and possibilities in the management of the grid [1]. Those inverters mainly interact with distributed energy resources, for instance, photovoltaic (PV) panels. For long years, they just extracted the maximum power from the PV panels and injected it into the grid [2] with the reference of unitary power factor. New trends about controlling photovoltaic inverters propose to integrate to them active functions [3]. In this way, inverters will become active devices of the electrical grid, ensuring local support, quality warranties and security of supply. Some of these new demanded active functions (even some of them by regulation [4]) are power flow control (P and Q), voltage level at the point of common coupling (PCC) control, active filtering capabilities [5], integration with the energy resource (MPP tracking, energy storage [6-8] ,…) and communication compatibilities among others.

Controlling the power flows by inverters is one of those main issues, in both transient (e.g., during voltage sags) and steady conditions [9] (e.g., restoring the voltage level at the PCC). The extra-capacity of inverters [1] and, in the case of PV distributed plants, the limitation of active energy production, can be used as solutions for this requirement. In this way, inverters can generate or consume reactive power (Fig. 1) providing the required local support and control.

At the same time, PV industry aims to reduce the cost associated with PV inverters by increasing the overall performance. In order to achieve its goal, innovative ideas in terms of circuit topologies are carried out, and Z-Source Inverter (ZSI) [10] and quasi-Z-Source Inverter (qZSI) [11] topologies are quite appropriates for PV applications due to their boosting capabilities. qZSI inherits the advantages provided by ZSI as well as gets smaller passive component rating and continuous input current mode.

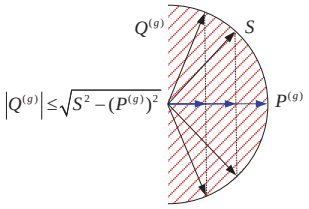

Fig. 1. Inverter capacity.

Also current trend in multilevel inverter topologies [12] indicates the preference of using multiple numbers of power devices of smaller rating instead of one device of large rating with has as consequences higher power quality, higher voltage capability, better electromagnetic compatibility and lower switching losses among others. Also new industry applications for multilevel inverters are emerging, in particular, for interfacing renewable energy sources.

Due to the aforementioned causes, this paper proposes a new control strategy for controlling P and Q injected powers for Z or qZ source inverters based on a synchronous reference frame *d-q* [13-14]. As the original *d-q* and *p-q* theories are applicable to three-phase three-wire or four-wire systems and cannot be used directly for a single phase system, some approaches [15-16] to expand the three-phase *d-q* theory to single phase systems have been taken into account. In this way, the proposed control strategy is validated by simulation in a Three-Level Neutral-Point-Clamped qZSI (3L-NPC qZSI) topology proposed in [17] (Fig.2) under different conditions.

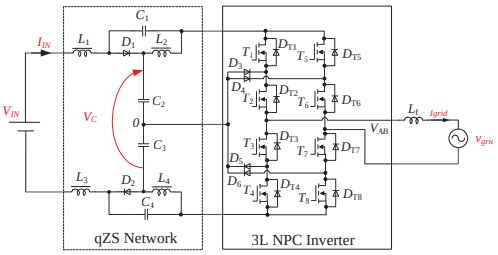

Fig. 2. 3L NPC qZS inverter connected to the grid.

II. Proposed Single Phase Active and Reactive Power Control Strategy

This section explains the basis of the proposed control scheme as new active function for Z or qZ single phase inverter. For controlling P and Q it is used a synchronous reference frame *d-q*. First of all, the expressions for single phase systems to transform time varying signals (voltages and currents) to *d-q* components are showed. Afterward, the full control strategy to generate the references of the converter to track the desired P and Q values is detailed.

A. Theoretical Aspects of the Single Phase Rotating D-Q Reference Frame Transformation

As aforementioned, the original *d-q* transformation from *abc* coordinates (time varying signals) can only be used in three phase systems [18]. It has been widely used in active filters and reactive power compensators because the fundamental frequency components are mapped to DC values. The linear transformation from *abc* time varying signals to synchronous reference *d-q* components is given by (1) [19]:

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin\omega t & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ \cos\omega t & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

where $\theta = \omega t$ and ω = electric system pulsatance.

The three-phase *abc* vector (currents or voltages) can also be transformed to rotating *d-q* components if previously they are transformed by using an orthogonal *α-β* stationary frame [20] (expression (2)) and then to synchronous frame *d-q* with expression (3):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{\sqrt{2}}{3}\begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \quad (3)$$

Expression (3) comes from make rotating the *α-β* stationary frame at the fundamental frequency, so two orthogonal components are required to obtain the resulting *d* and *q* values. It is the main problem to use this theory in single phase circuits where just one phase signal (current or voltage) is available.

Different approaches have been developed to obtain the necessary orthogonal component and, in this way, *d-q* theory will be applied in single phase studies.

[21] proposes the orthogonal imaginary circuit concept with the main idea of obtaining two variables, the real one (voltage or current) and an imaginary one, with equal characteristics but shifted 1/4 of period of the real one.

From the practical point of view, if we measure the real signal to be transformed to the *d-q* rotating frame, just using a time delay method (storing the value) we can obtain the imaginary component and in this way, the measured signal is the *α* component and the delayed signal is the *β* component. This fact is illustrated in Fig. 3 a).

Mathematical foundations for the case where the real signal is a sine are as follows (example for voltage signal):

$$\begin{aligned} v_r &= v_\alpha = V\sin(\omega t + \varphi) \\ v_i &= v_\beta = V\sin(\omega t + \varphi - \pi/2) = -V\cos(\omega t + \varphi). \end{aligned} \quad (4)$$

To obtain the DC values in a *d-q* rotating frame from AC signals (Fig. 3 b) is necessary to use the linear transformation (5):

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \quad (5)$$

If the real signal is considered as cosine, the linear transformation would be different [22] (replacing sin (ωt) with cos(ωt) and cos (ωt) with -sin(ωt)).

If one transforms equations (4) by means of linear transformation (5):

$$\begin{aligned} v_d &= V\sin(\omega t + \varphi)\sin(\omega t) - V\sin(\omega t + \varphi - \pi/2)\cos(\omega t) = \\ &= V\cos(\varphi) \\ v_q &= V\sin(\omega t + \varphi)\cos(\omega t) + V\sin(\omega t + \varphi - \pi/2)\sin(\omega t) = \\ &= V\sin(\varphi), \end{aligned} \quad (6)$$

it is obtained the DC components of the original AC signals at the fundamental frequency in the synchronous *d-q* frame.

Finally, the inverse linear transformation from *d-q* signals to *α-β* is given by (7):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \sin\omega t & \cos\omega t \\ \cos\omega t & -\sin\omega t \end{bmatrix}\begin{bmatrix} v_d \\ v_q \end{bmatrix}. \quad (7)$$

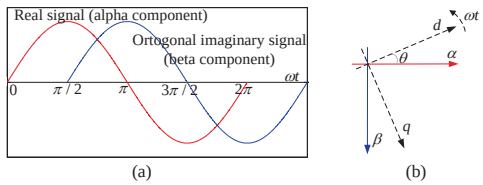

Fig. 3. a) Real and imaginary signals. b) *αβ* to rotating *dq* reference frame transformation.

B. *Control Strategy based on Controlling d-q Voltage Components*

Fig. 4 illustrates the proposed control strategy to obtain the *d-q* reference voltage components of the inverter, in order to control P and Q by means of controlling *d-q* components of the injected current into the grid.

A single-phase phase locked loop (PLL) is needed to obtain the phase information (θ angle) of the grid voltage at the PCC. This angle is used by the linear transformations (5) and (7), direct and inverse respectively to transform from α-β stationary frame signals to synchronized *d-q* signals and vice versa. In addition, if the *d-q* frame has the same frequency than the grid frequency, and the *d* axis is aligned with the grid voltage vector, the *q* component of grid voltage will be zero.

As aforementioned, to make possible the control in a *d-q* rotating frame are necessaries two orthogonal components in a stationary frame. The orthogonal (the imaginary one) component is obtained by delaying a quarter of period at the fundamental frequency [21] the measured signals of grid voltage and grid current.

The full control system uses two control loops in a coupled way, regulated by PI controllers. The internal control loop regulates the error (reference less measured) of the *d* component of the grid current by acting over *d* and *q* component of the inverter reference voltage. It means that this PI controller adjusts the amplitude of the reference signal. The external control loop regulates the error of the *q* component of the grid current and acts just over *q* component of the of the inverter reference voltage. This controller adjusts the phase of the reference signal.

Obtained reference values of *d-q* components of the inverter reference voltage, it is known the minimum value of the required DC-Link voltage. This reference value ($V_{c,ref}$) is compared with the measured DC-Link voltage (V_c) to determine the work mode of the inverter. If $V_{c,\,ref}$ is bigger than V_c, the boost mode is activated and a third control loop is involved. The shoot-through duty cycle (D_s) is adjusted by the third PI controller. In this case, the reference signal ($V_{AB,\,control}$) of the sinusoidal pulse width modulation block (SPWM) [23] is obtained by (8):

$$V_{AB,control} = \frac{(1-D_S)\, v_{mod}}{V_{C,ref}}\,, \tag{8}$$

where v_{mod} is the inverter reference voltage, obtained by using the inverse transformation (7) in the *d-q* inverter reference voltage components.

If $V_{c,\,ref}$ is less than V_c, the inverter works in buck mode so it is not necessary to use the third control loop because *Ds* will be equal to zero. In this case, the reference signal of the SPWM block is given by (9):

$$V_{AB,control} = \frac{v_{mod}}{V_C}\,. \tag{8}$$

III. Simulation Results

In order to validate the control strategy for controlling P and Q in a single phase Z/qZ source inverter topology, a simulation study was performed in PSCAD/EMTDC. The proposed control strategy is implemented in a single phase 3L-NPC qZSI connected to the grid.

Steady and transient responses are analyzed in order to demonstrate that this strategy is suitable in any condition (with constants or variables references) of P, Q and input voltage (V_{in}) (in this way, three PI controllers are tested) so, this section is divided in two.

Another important aspect is that PI controller of the internal loop must be faster than PI controller of the external loop. It has been taken into account to tune them by means of manually methods.

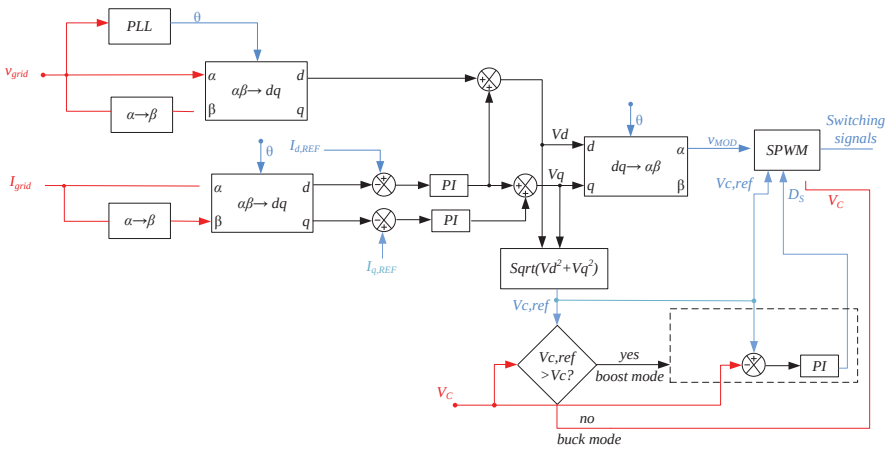

Fig. 4. Proposed P and Q control scheme for single phase z source or qZ source inverter based on rotating *d-q* reference frame.

A. *Steady Responses*

Table I shows the different parameters that have been used in this case of the simulation study.

TABLE I
USED VALUES FOR SIMULATION STUDY

Parameter	Unit	Value		
Inductors $L_1,\ldots, L_4$	(mH)	0.29		
Capacitor C_1,C_4	(mF)	4		
Capacitor C_2,C_3	(mF)	1.3		
Grid RMS voltage	(V)	230		
Input voltage	(V)	240		
K_p of controllers (for I_d, I_q and D_s)		0.005	0.005	0.35
t_i of controllers (for I_d, I_q and D_s)		0.02	0.25	0.08
Switching frequency	(kHz)	50		
Simulation step	(µs)	0.25		

Values of passive elements of qZ network are calculated according to guidelines provided in [24] and also, the converter is working in boost mode as generalization.

Fig. 5 represents the different obtained waveforms in steady state when $I_{d,ref}$ is equal to 5 A and $I_{q,ref}$ is equal to 0 A. a) input current (I_{in}) and voltage (V_{in}), b) DC-Link voltage ($V_{DC\text{-}Link}$), c) voltages in capacitors (V_c), d) output inverter voltage (V_{AB}), e) grid voltage (V_g) and injected current (I_g) and f) *d* and *q* components of the injected current.

We can see in Fig. 5 a) that the converter is working in continuous mode (input current never crosses the zero) and due to the low value of V_{in}, $V_{DC\text{-}Link}$ (Fig 5 b), is going to zero because shoot-thought states are applied. A ripple at 100 Hz is appreciated in both signals, due to the single-phase power pulsation.

Fig 5 c) shows how the input voltage is boosted according

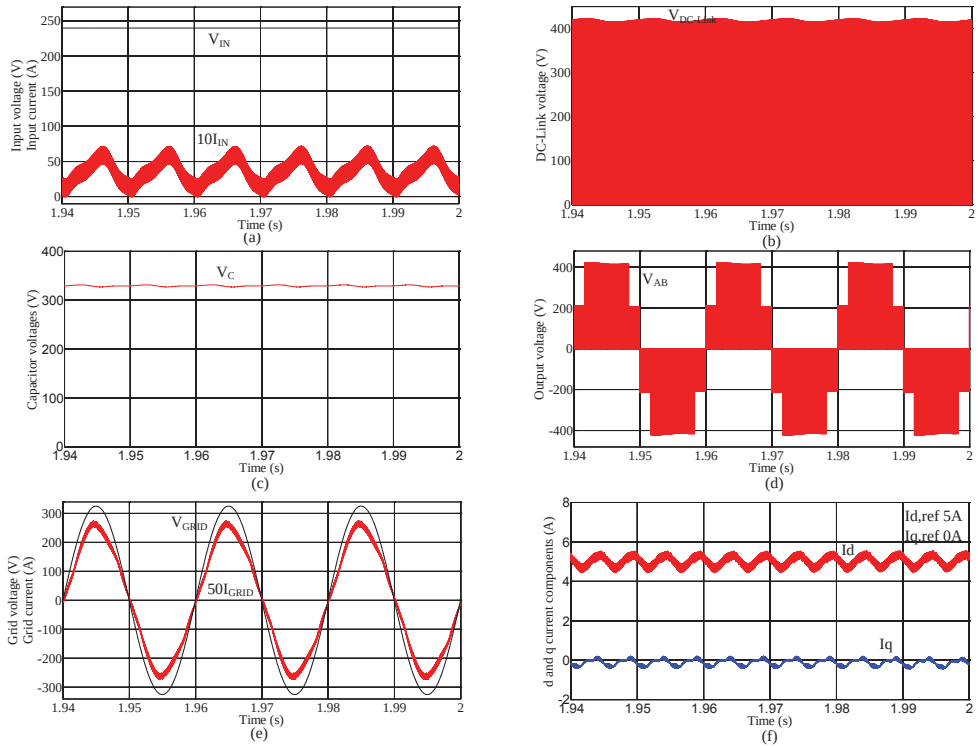

Fig. 5. Simulation results in steady state. a) Input current and voltage. b) DC-Link voltage. c) Voltages in capacitors C_2 and C_3. d) Output voltage V_{AB}. e) Grid current and voltage. f) d and q components of grid current.

to equation (9) [23]:

$$V_C = M \cdot B \cdot V_{IN} = \frac{1-D_S}{1-2D_S} V_{IN} \,, \tag{9}$$

where M is de modulation index and B is the boost factor. Finally, Fig. 5 e) and f) show that the references of $I_{d,ref}$ and $I_{q,ref}$ are tracked successfully.

B. Transient Responses

Fig. 6 shows the response of the system in different dynamic conditions. Fig. 6 a) and b) show the starting of the described case in section A. We can appreciate the evolution of D_s and $V_{AB,control}$ in 6 a) and evolution of I_d and I_q components of injected current in 6 b). Once the D_s reaches the steady state (second 0.5), PI controllers of I_d and I_q start to converge. Internal controller for I_d shows a faster response according to tuning procedure.

The second transient situation is represented in Fig. 6 c) and d), with the evolutions of D_s and $V_{AB,control}$, and evolutions of I_d and I_q components respectively, when a step in V_{IN} from 240 V to 500 V is applied in second 1.5. The converter change from boost to buck mode and the references of I_d and I_q are properly tracked in both points. This case is related with PV applications, where V_{IN} can change in a fast way. In order to make the evolution of D_s faster than in previous case, the t_i of its controller has been tuned in 0.02.

Finally, steps in $I_{d,ref}$ and $I_{q,ref}$ can be observed in Fig. 6 e) and f) respectively. $I_{d,ref}$ is changed from 5 A to 7 A and $I_{q,ref}$ from 0 A to 2 A, at the second 1.5. In both cases, the references are tracked with high accuracy and velocity.

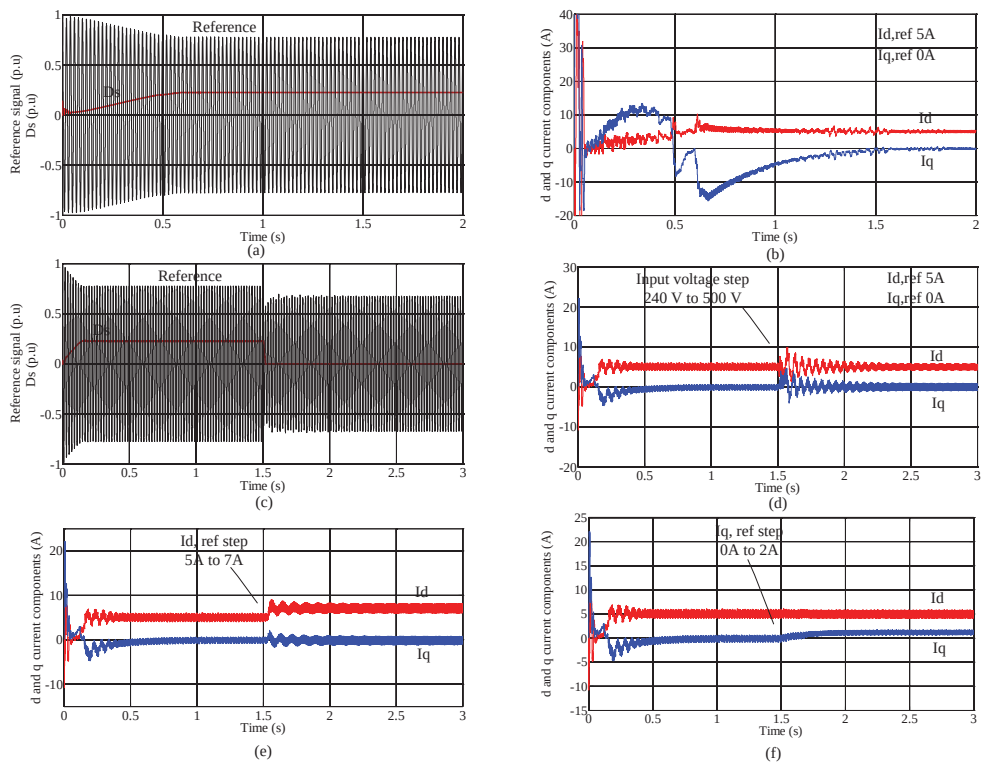

Fig. 6. Transient responses in different cases. a) Reference signal and D_s evolutions during grid connection transients. b) *d* and *q* grid current components at the same situation. c) Reference signal and Ds during an input voltage step. d) *d* and *q* grid current components during an input voltage step. e) *d* and *q* grid current components during a $I_{d,ref}$ step. f) *d* and *q* grid current components during a $I_{q,ref}$ step.

IV. CONCLUSIONS

This paper has proposed a new control strategy for single phase Z/qZ source inverter based on a *d-q* synchronous reference frame. The control strategy generates the *d-q* reference voltage components of the inverter in order to control P and Q power flows. This task is a new demanded active function for grid-connected inverter and, in this way, distributed energy resources will support to the electrical grid at the PCC, taking part as active equipments.

The proposed strategy is validated by simulation in PSCAD/EMTDC and different dynamic conditions were tested with satisfactory results, analyzing the response of each variable involved in the control system.

Future research activities will be devoted to experimental validations in a real prototype, and developing other active functions for these topologies, as active filtering capabilities.

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Simulation Study of the Grid-Connected Single-Phase Impedance-Sourced NPC Inverter with Different Control Methods

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***Abstract*—Focus is on three operation strategies for a grid-connected three-level neutral-point-clamped quasi impedance source inverter in a single-phase application. Each control scheme was implemented in the PSCAD/EMTDC simulation tool and underwent different tests, which involved some steps in the reference values and in the perturbations applied to the system. A comparison according to their responses was based on different criteria, such as rise time, settle time, overshoot and steady state error, in order to determine which would be more suitable for such application.**

Keywords—pulse width modulation inverters; photovoltaic systems; PSCAD; power system control; distributed power generation

I. INTRODUCTION

Shortage of fossil fuels and the necessity of reducing CO_2 emissions among other reasons have significantly grown the number of inverter-based distributed generator (DG) connected to the low-voltage distribution network. Many of them interact with renewable energy sources (RESs) such us photovoltaic (PV) modules (Fig. 1 shows the installation). For a long time, PV inverters' function was merely to inject power into the main grid with a unitary power factor as the control reference [1] but under new trends and policies for PV plants they are integrated as active and smart devices [2]-[3]. As a burning ambition, this current philosophy contributes to the change from the traditional and linear power systems to the smartgrid and microgrid [4] concepts. In this way, PV inverters would be able to contribute to the local voltage support, improve the power quality and give rise to flexibility and security of supply. Some of those new demands for inverters are power flow controls [5], voltage level restoration at the point of common coupling [5]-[6] (PCC), active filtering capabilities [7], integration with energy storage systems [8], and communications compatibilities.

Concurrently, innovative ideas in terms of inverter circuitries have emerged during the last years. Some of them seem quite suitable for PV applications because they can step up the DC input voltage in a single power conversion stage by means of the shoot-through switching states, known as Z-source inverter (ZSI) family and its derivations [9]-[11].

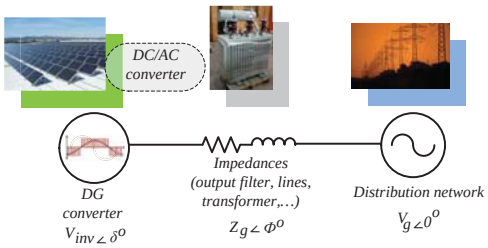

Fig. 1. Basic scheme of a grid-connected photovoltaic inverter.

Furthermore, ZSI family has been integrated with multilevel bridges to acquire their intrinsic advantages [12]. However, because of the relatively early stage, only few studies deal with the grid-connected integration with closed loop control systems, which basically must provide coexistence of an operation strategy of the inverter, a maximum power point tracking (MPPT), a DC-link voltage control method and a special modulation technique to embed the shoot-through states into the normal ones. For instance, a control strategy for the injected current in a grid-connected three-phase ZSI based on proportional-resonance and repetitive controllers is detailed in [13] in order to deliver a balanced set of current into a distorted system. A grid-connected three-phase PV quasi ZSI with a battery storage system is studied in [14]. The proposed control structure is based on a *d-q* rotational synchronous reference frame and a shoot-through control method to extract the maximum power for the PV array. A decoupling active and reactive power control is described in [15] for an application similar to that in [14].

In the particular case of grid-connected single-phase multilevel impedance family inverters (Fig. 2), some previous studies have dealt with the control system design [16]. As the original *d-q* and *p-q* theories were developed to three-phase three-wire or four-wire systems, they cannot be used directly for single-phase systems. Nevertheless, some approaches [17]-[18] to expand the three-phase *d-q* theory to single-phase systems can be found in the literature.

In section II, three different closed loop control systems with shoot-through regulation are proposed and schematically

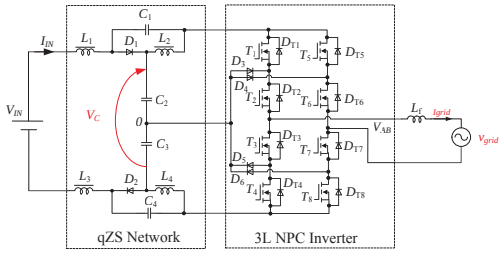

Fig. 2. Single phase 3L NPC qZS grid-connected inverter.

explained for a single-phase three-level neutral-point-clamped qZSI (3L NPC qZSI) [19]. Next, the simulation study and the results obtained for each control structure are shown with emphasis on the system dynamics. Finally, different responses in each situation based on different criteria, such us rise time, overshoot and settling out to a steady state, are compared.

II. Schemes and Explanations of the Proposed Control Methods

In general, all inverter control strategies can be classified according to the controlled parameters: output voltage or current control, stationary or rotating reference frame and direct or indirect power control. In the PV inverter with intermediate boost, the DC-DC converter control system is divided as well. ZSIs are considered as single-stage converters, but with regard to the control system, they are considered as a two-stage structure due to the shoot-through duty cycle (D_S) with its additional control parameters.

Several approaches applied to grid-connected PV ZSIs are described in [20]-[24]. Their treatment in the shoot-through control is similar. By means of the MPPT block, the reference PV voltage (input voltage) is obtained. Taking into account that the capacitor voltage (V_C) remains constant, D_S is defined as [20]-[21]:

$$D_s = \frac{V_C - V_{IN}}{2V_C - V_{IN}}. \tag{1}$$

At the same time, voltage error on the capacitor (or DC-link) along with the PI controller are used for the power references. Stable capacitor voltage means balanced power between the demanded power from the PV panel and that injected to the grid. Usage grid voltage shape as reference shape for current provides only active power at the PCC. The main drawback of such approach lies in the low dynamic performance.

Another control strategy based on the *d-q* rotation frame, however different from those above, was proposed in [16] for a single-phase application. As mentioned earlier, based on the *d-q* theory, the three-phase system was developed, where the concept of orthogonal imaginary circuit was used. The main idea is to obtain two variables, the real one (measured voltage or current) and an imaginary one, with equal characteristics but

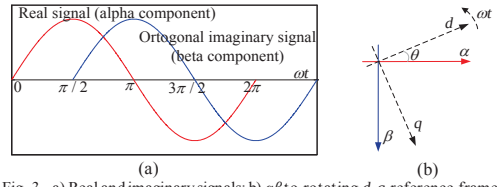

Fig. 3. a) Real and imaginary signals; b) $\alpha\beta$ to rotating *d-q* reference frame transformation.

shifted 1/4 of the period of the real one. In this way, the measured signal is α component and the delayed signal is β component. This fact is illustrated in Fig. 3 a) and b). Shoot-through control strategy is different as well. D_S is regulated depending on the *d* and *q* components of the reference voltage ($V_{d,ref}$ and $V_{q,ref}$). The sketch of the grid side control shown in Fig. 4 a) is slightly modified as compared to that in [16].

According to this scheme, the control of active and reactive powers is carried out by two integral (*I*) regulators, which operate in a coupled way. Control action derived from the *q* current component error ($I_{q,ref}$-I_q) acts over the *d* and *q* component of the inverter reference voltage ($V_{d,ref}$ and $V_{q,ref}$). It means that this *I* controller adjusts the amplitude of the reference signal. Control action derived from the *d* current component error ($I_{d,ref}$-I_d) acts just over the *q* component $V_{q,ref}$, adjusting the phase of the inverter reference voltage. This reasoning is derived from the well known electrical relationships (between *P*-δ and *Q*-*V*). In addition, feedforward loops from the grid voltage are included to smooth the connection of the inverter to the grid, which avoids undesirable transients. Finally, as the *d-q* frame has the same frequency as the grid frequency, and the *d* axis is aligned with the grid voltage vector, the *q* component of the grid voltage will be zero [25].

When $V_{d,ref}$ and $V_{q,ref}$ are determined, the minimum value of the required DC-link voltage can be calculated. This reference value ($V_{c,ref}$) is compared with the measured DC-Link voltage (V_c) to activate or not to activate the $D_{s,ref}$, depending on whether the boosting voltage is needed or not, respectively. Shoot-through duty cycle is adjusted by the third *I* controller. Finally, the scaled reference signal as an input for the Sinusoidal Pulse Width Modulation (SPWM) block [19]-[25] is obtained:

$$v_{control} = \frac{(1 - D_{S,ref})\, v_{ref}}{V_C}. \tag{2}$$

Fig. 4 b) shows a variant of the previous operation strategy by decoupling the active and reactive power control loops. In this proposal, control actions from ($I_{d,ref}$-I_d) and from ($I_{q,ref}$-I_q) are added to the $V_{d,grid}$ and $V_{q,grid}$ feedforward loops respectively, to generate the inverter reference signal. This approach is based on the following equations:

$$P = V_d I_d, \tag{3}$$

$$Q = -V_d I_q. \tag{4}$$

DC-link voltage control is exactly the same as in the previous case. Fig. 4 c) depicts a modification of the control strategy for the DC-link voltage control.

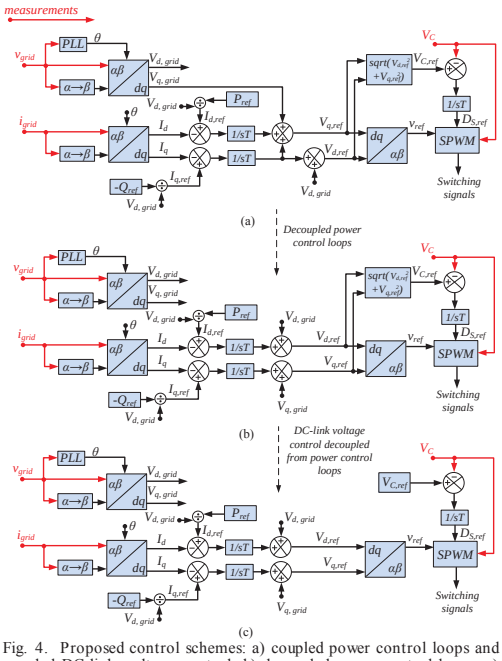

Fig. 4. Proposed control schemes: a) coupled power control loops and coupled DC-link voltage control; b) decoupled power control loops; c) decoupled DC-link voltage control.

In this case, this control loop is independent of the power controllers, and the DC-link voltage reference is given by a predefined value. In our case, this value ($V_{c,ref}$) is fixed at 350 V to assure the control of the injected current into the single-phase grid.

III. Simulation Study and Transient Responses

To validate and compare the three different control strategies described in section II, a comprehensive simulation study was performed in the PSCAD/EMTDC tool. The values of the passive elements of the qZ network and the output filter of the single-phase 3L-NPC qZSI were calculated according to the guidelines in [19] and [26].

The parameters for the PI controller were obtained similarly to [27] using the Ziegler-Nichols method based on the response curve [28]. All the different values and parameters used during the simulations are shown in Table I. As can be seen, the values of the PI controller are the same for all the proposed control schemes. The reason is in the same control object that mainly defines the dynamic behavior of the overall system.

As the main goal of this work is to analyze the system responses in dynamic conditions, different events were programmed. From the off-grid situation, the inverter is connected to the grid at second 0.2. Then, steps in $I_{d,ref}$ and $I_{q,ref}$ are implemented at seconds 0.5 and 1.2 respectively, in order to inject active and reactive power (2 A). Finally, the input voltage is suddenly reduced with a step as well, from 365 V to 295 V, because the boundary between the buck and the boost working mode is around 325 V (peak value of the grid voltage). With all these events it is possible to analyze all the control loops based on integral controllers.

TABLE I
Values for Simulation Study

Type	Simulation values			
	Parameter	Unit	Value	
Quasi-impedance network	Inductors $L_1,\ldots,L_4$	(mH)	0.29	
	Capacitor C_1,C_4	(mF)	4	
	Capacitor C_2,C_3	(mF)	1.3	
	Series resistance of L_i	(Ohm)	0.05	
Output filter	Inductor L_f	(mF)	2.2	
Grid impedance	Series resistance and inductance (R_g and L_g)	(Ω) (mF)	0.05	1.5
Electrical values	Input voltage V_{in}	(V)	365	
	Grid RMS voltage V_g	(V)	230	
Power controllers (scheme a)	Time constant for I_d	(s)	0.05	
	Time constant for I_q	(s)	0.05	
Power controllers (scheme b)	Time constant for I_d	(s)	0.05	
	Time constant for I_q	(s)	0.05	
Power controllers (scheme c)	Time constant for I_d	(s)	0.05	
	Time constant for I_q	(s)	0.05	
DC-link controller (scheme a)	Time constant for V_C	(s)	0.08	
DC-link controller (scheme b)	Time constant for V_C	(s)	0.08	
DC-link controller (scheme c)	Time constant for V_C	(s)	0.065	
Simulation parameters	Switching frequency	(kHz)	50	
	Simulation step	(μs)	0.25	

Different responses under described conditions are depicted in Fig. 5 a), b) and c). From top to bottom, the evolution of the grid injected currents (I_d and I_q components) for each control strategy is revealed.

Fig. 6 shows the evolution of different inverter parameters during the full simulation time. In a) the input voltage (green line) is represented, which is common in any developed simulation, allowing comparison under equal conditions. Capacitor voltage (V_c) is represented in the same picture (red line). Evolution of the shoot-through duty cycle is presented in b), and, c) and d) show the output voltages (V_{ab}) before filtering when D_s is zero and maximum, respectively.

Fig. 6 illustrates the control strategy presented in 4 b). For the other control schemes (Fig. a) and c)), waveforms are quite similar.

IV. Comparison and Discussion

Starting from the first event (inverter is connected to the grid), one can observe that it is produced at second 0.2. For each operation strategy, this process is really smooth (Fig. 5 a), b) and c)), mainly derived from the aforementioned grid voltage feedforward loops and well-tuned integral controllers (by means of the trial and error method). Those facts avoid undesirable transient currents on the inverter trip. From 0.2 to 0.4 s, the inverter is considered to be in a floating situation for all cases (P=0 and Q=0).

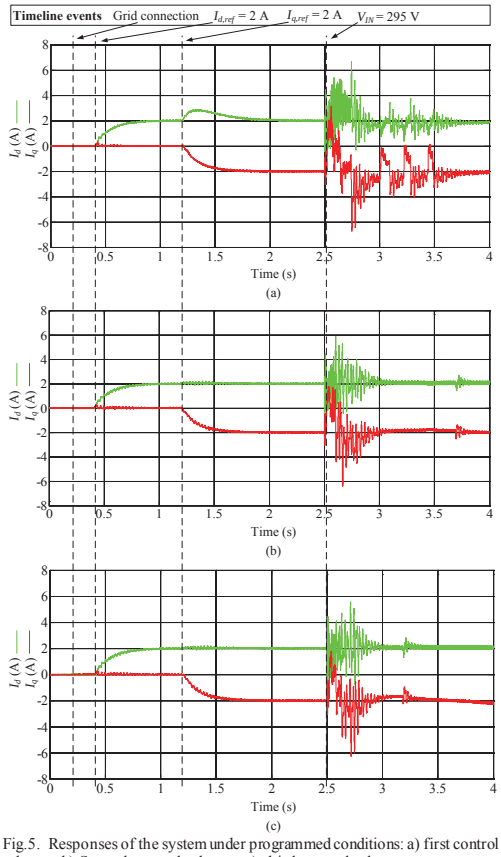

Fig.5. Responses of the system under programmed conditions: a) first control scheme; b) Second control scheme; c) third control scheme.

At second 0.4, a step in $I_{d,ref}$ is applied (From 0 A to 2 A) and this new reference is tracked with high accuracy by any control strategy (green lines in Fig. 5). In addition, it is possible to see that the influence on the I_q component is negligible (red lines). It is produced because the control actions in the direct component of the current act in one component of the inverter reference voltage.

At second 1.2 a new reference step is programmed in $I_{q,ref}$ (from 0 to -2 A). The new reference is tracked properly again in all cases but, for the first control strategy, it presents a coupling in the power loops. It is due to the control action over I_q error added to both components of the reference inverter voltage, in order to increase the modulation index of v_{ref}. This coupling is not presented for schemes b) and c), where merely one inverter component is affected by the current error.

Finally, at second 2.5 a perturbation in the input voltage (step from 365 V to 295 V) is applied. It will force the converter to change from the buck to the boost mode. In the case of the first control strategy, longer transients both to I_d and to I_q are observed before reaching again the steady state in both components. This undesired situation happens because the DC-link voltage control and power control loops are strongly coupled, therefore their influence is high. This transient is shorter in Fig. 5 b) and c) because of a lower coupling between the power control loops and between those ones and DC-link voltage control loop. In addition, a smaller ripple in I_d and I_q current components is observed in Fig. 5 b) and c) than in Fig. 5 a) at the end of the simulated time, which is also connected with the coupling between the control loops.

A quantitative comparison for each response presented in Table II is based on different parameters, such as rise time, overshoot, settling time, transient duration and steady state error. It will help to understand the previous discussion better.

Fig. 6 a) shows the input voltage (green line) and the capacitor voltage (red line) in the case of the control strategy in Fig. 4 b). When the input voltage step is applied, the converter changes from the buck to the boost mode and in this last situation, the capacitor voltage acquires the minimum required value to assure the desired active and reactive power. This situation also happens with the first control scheme but not with the last one, where a predefined $V_{c,ref}$ is given and obviously it will be greater than in the other controls.

TABLE II
Response Parameters

Type	Parameter	Unit	Loop I_d	Loop I_q	Loop V_c
Control scheme (frigure a)	Rise time	s	0.357	0.353	0.63
	Overshoot	%	0	0	0
	Settling time	s	0.6	0.581	1.271
	Steady state error	A	0	0	0
	Main features: 1) Strong coupling between power loops and between DC-link and power loops. 2) Minimum DC-link voltage.				
Control scheme (figure b)	Rise time	s	0.346	0.342	0.6
	Overshoot	%	0	0	0
	Settling time	s	0.5918	0.571	0.5
	Steady state error	A	0	0	0
	1) Insignificant coupling between power loops and strong between DC-link and power loops. 2) Minimum DC-link voltage.				
Control scheme (figure c)	Rise time	s	0.346	0.342	0.05
	Overshoot	%	0	0	0
	Settling time	s	0.5918	0.571	0.75
	Steady state error	A	0	0	0
	1) Insignificant coupling between power loops and strong between DC-link and power loops. 2) Not minimum DC-link voltage.				

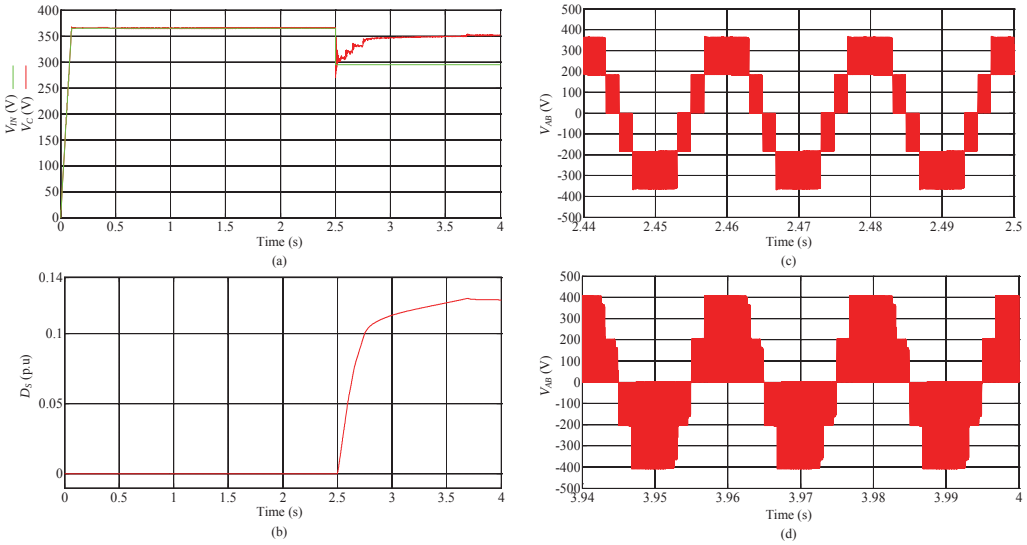

Fig. 6. Different magnitudes obtained with the second control scheme: a) input voltage (green line) and capacitor voltage (red line); b) shoot-through duty cycle; c) output voltage without shoot-through states; d) output voltage with shoot-through states.

The shoot-through duty cycle shown in Fig. 6 b) produces the aforementioned capacitor voltage evolution. The output inverter voltage under the shoot-through states illustrated in Fig. 6 d) (boost mode) is compared to that with the inverter working in the buck mode (Fig. 6 c). According to Fig. 6 a) and d), the maximum value of Vab is larger than that of Vc during the boost operation, since Vc matches with the average value of the DC-link voltage.

V. CONCLUSIONS

Different operation strategies for a single-phase 3L NPC qZS inverter for grid-connected applications have been proposed and compared in this paper. The control scheme shown in Fig. 4 a) demonstrates a strong coupling between its power control loops and between the DC-link voltage control loop. However, it works with a minimum value. Then, decoupled power control loops with a better dynamic response and the minimum value maintenance of the DC-link voltage were considered. Finally, in the last scheme, the DC-link control loop was found independent of the power control loops, in spite of the increasing the DC-link voltage level. All the control systems were tested in simulation under different dynamic conditions. Further research will focus on the converter and its control systems during transient events in the main grid and on the experimental validation of the ideas and conclusions derived from this work.

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Operation Strategy and Shoot-Through Indirect Control Method for Three-Phase Z-Source Inverters

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***Abstract*—This paper proposes a new operation strategy for a three-phase inverter based on impedance-source network in grid connected applications as well as an indirect control method of the dc-link voltage. The strategy is based on a *d-q* synchronous reference frame and it is mainly intended for photovoltaic applications at high switching frequency. Both control systems are explained in detail and the problems and influences between them are also described. The strategy and the indirect control method of the dc-link voltage are validated and discussed by PSCAD/EMTDC simulations with a three-phase three-level neutral-point-clamped quasi-impedance-source inverter.**

Keywords*—power electronic converters; power control; distributed power generation; power system simulation; photovoltaic systems; pulse width modulation converters.

I. Introduction

Lack of conventional energy sources and concern about environmental pollution have produced a fast rise in the number of inverter-based Distributed Generators (DGs) connected to the low-voltage distribution network [1]. Many of them interact with Renewable Energy Sources (RESs), such us Photovoltaic (PV) modules [2] and wind turbines [3], and are presented in any Energy Storage System (ESS) [4]. Fig. 1 shows an electrical representation of the fact mentioned.

Industry and research are aiming at cost reductions and enhanced performance of the energy conversion process, with a focus on the inverter topologies. Attention is on PV inverters, which are traditionally characterized by two-stage converters composed by a dc-dc boost converter and the Voltage Source Inverter (VSI) [5] or the Current Source Inverter (CSI). New impedance-source network based topologies [6] provide a single-stage conversion, which allows the following: voltage boost/buck, extended range of operation, low cost and high efficiency, strong electromagnetic immunity, no need for dead time, minimum number of semiconductor devices, improved reliability and performance, and short-circuit protection among other advantages. On the other hand, the relatively youth of those Z-Source Inverters (ZSIs) makes the design of their control stage complex[7] where basically must coexist an operation strategy of the inverter, a dc-link voltage control method and special modulation techniques to embed the shoot-through states.

For the first key element, it is possible to design an operation strategy based on the traditional approaches, depending on the applications (PV inverters [8], DG, vehicle to grid (V2G) [9], excitation field for synchronous machines [10], ESS [11], uninterruptible power supply and active filtering among others). To distinguish grid-connected PV applications, operation strategies based on the *d-q* synchronous reference frame seems to be the most popular [8]-[12].

In the second aspect, previous works divide the dc-link voltage control (or shoot-through duty cycle (D_s) regulation) into direct or indirect control [13], depending on whether the dc-link voltage is sensed or not, respectively (see Figs. 2*a* and 2*b*). Finally, special modulation techniques have been proposed to deal with classical switching states along with shoot-through states. A detailed comparison and a review are provided in [14].

The complexity of control design lies in the interdependence of the aforementioned elements and the control parameters. A change in one parameter influences the other ones and vice versa [7].

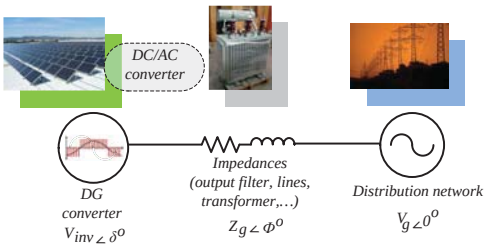

Fig. 1. DG interfaced converter connected to the distribution network.

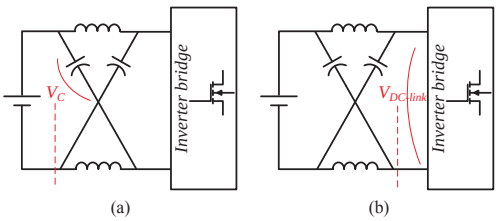

Fig. 2. Controls of dc-link voltage. a) Indirect method. b) Direct method.

This paper presents a novel operation strategy to inject the desired active (P) and reactive power (Q) by a three-phase ZSI in the grid-connected mode with an indirect control of the dc-link voltage. As the studied application is devoted to the PV, the control system has been validated by simulation in a three-phase Three-Level Neutral-Point-Clamped Quasi-Z-Source Inverter (3L NPC qZSI) [15]. The Quasi-Z-Source (qZS) network works with continuous input current (from PV modules). At the same time it has an advantage of using a multilevel inverter bridge [16].

Section II contains a description of the proposed strategy along with the indirect control of the dc-link voltage. Section III describes the simulation study and the results obtained. In the final part, conclusions, future challenges and problems to be solved are emphasized.

II. Proposed Operation Strategy with Shoot-through Indirect Control Method

As it was previously cited, inverter operation strategies for Z-source topologies can be derived from the traditional approaches for conventional topologies.

In the same way, P and Q can be controlled by using the d-q theory [8]-[12] to generate the reference signals of the manipulated variables. Grid voltages and currents (v_{grid} (a,b,c) and i_{grid} (a,b,c)) are sensed and converted into dc d-q values by means of Clarke and Park transformations. If the d-q frame has the same frequency as v_{grid} (a,b,c) and the d axis is aligned with the grid vector voltage, the q voltage component will be zero [17]. Operating in this way, the expressed variables in abc are transformed in:

$$\vec{i}_{grid} = I_{d,grid} + jI_{q,grid}\,, \tag{1}$$

$$\vec{v}_{inv} = V_{d,inv} + jV_{q,inv} \quad \text{and} \tag{2}$$

$$\vec{v}_{grid} = V_{d,grid}\,. \tag{3}$$

To make those transformations, a Phase-Locked-Loop (PLL) or a synchronization method is required [18]. In addition, P and Q are expressed as [19]:

$$P = V_{d,grid} I_{d,grid}\,, \tag{4}$$

$$Q = -V_{d,grid} I_{q,grid}\,. \tag{5}$$

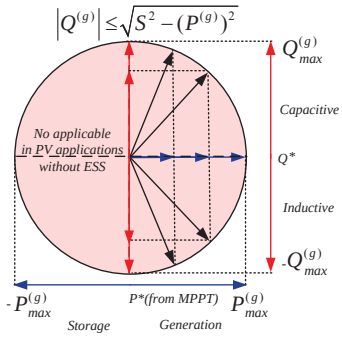

Fig. 3. Power operation regions for PV inverters.

In grid-connected PV applications, reference active power (P^*) is usually given by a Maximum Power Point Tracker (MPPT) (Fig. 3). On the other hand, reference reactive power (Q^*) must be limited by the rated current of the semiconductors according to the highlighted equation of Fig. 3. Two PI controllers are involved to track P^* and Q^* by acting over the manipulated variables ($V^*_{d,ref}$ and $V^*_{q,ref}$, respectively) to produce the desired voltage signals (using back Clarke and Park transformations). Finally, a $V_{d,grid}$ feedforward loop is added to make easier the synchronization process. Some studies report a PQ decoupling control [12].

This approach was neglected for the reasons shown in the case of study in the next section. Full operation strategy can be followed on the block diagram of Fig. 4.

Once the desired voltage signals to control the power are obtained, it is easy to determine the minimum required value of the dc-link voltage. Therefore, it is hard to sense such voltage in experimental applications (shoot-through states produce a square waveform), V_c (it is a constant waveform) is commonly used to control the dc-link voltage (called as indirect voltage control). Both waveforms are depicted in Figs. 5*a* and 5*b*, respectively. Disadvantages of this approach are that peak dc-link voltage is uncontrollable and the dynamic response produced in the system is deteriorated [13].

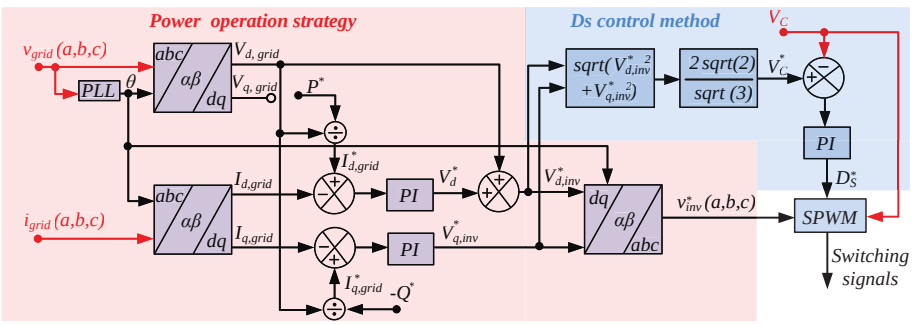

Fig. 4. Power operation strategy and the proposed shoot-through control method.

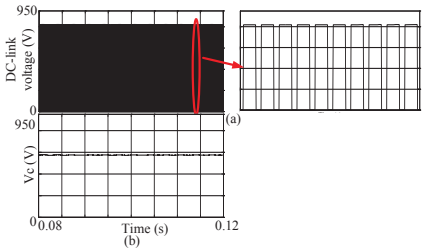

Fig. 5. Waveforms in the dc-link voltage control. a) Direct method (square wave due to the shoot-through states). b) Indirect method.

By direct and quadrature inverter reference voltages derived from the power control loops, V^*_c with the procedure in Fig. 4 can be composed. Finally, a third PI-based on the control loop is intended to manipulate D^*_s, which assures the required dc-link voltage by boosting (if it is necessary) V_{in}.

III. SIMULATION STUDY

To validate the explained operation strategy along the indirect dc-link voltage control, a simulation study based on PSCAD/EMTDC was performed. All the details of the study are explained in this section.

The chosen topology is a three-phase 3L NPC qZSI based on two symmetrical qZS networks [15]-[20]. Besides the advantages inherited from ZSIs, the qZSIs have such merits as continuous input current and a common dc rail between the source and the inverter bridge. Therefore, qZSIs suit very well for RESs, in particular for PV systems. Moreover, due to this inverter bridge, the power source can be single or separated by means of the neutral point, which allows different PV module series-parallel associations. Finally, the multilevel branches will have lower voltage stress on the semiconductors and fast MOSFETs can be used, which leads to high switching frequency and higher power density [20]. The latter reasons are connected with future experimental set-ups. The schematic of this full topology is depicted in Fig. 6.

To generate the switching signals (active states, zero states and shoot-through states) an Alternative Phase Opposition Disposition (APOD) Pulse Width Modulation (PWM) scheme [21] was used in these simulations. Three modulating waves ($Ref_{,a}$, $Ref_{,b}$ and $Ref_{,c}$) and two modified references (MR_1 and MR_2) are compared with two vertically disposed, 180 º phase-shifted carriers in order to obtain the different states of each switch (T) in each branch (a, b and c). Fig. 7 a) depicts the sketch of this modulation technique using a frequency modulation index (m_f) equal to 21 and Fig. 7 b) shows the details in a certain switching period.

Values of passive elements of the qZ network were calculated according to the guidelines provided in [22], which are based on different criteria. The methodology proposed in [23] for dimensioning the LCL output filter was also used.

All the parameters and used values in the simulation study are summarized in Table I.

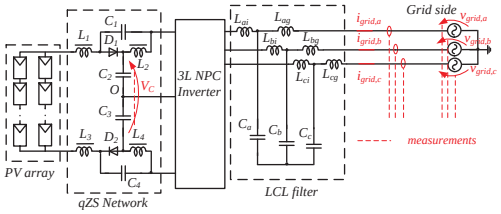

Fig. 6. Schematic circuit of a grid-connected multilevel qZ source inverter in a PV application.

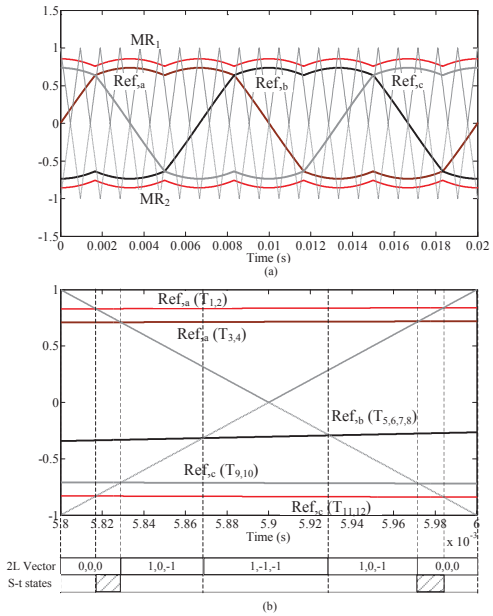

Fig. 7. APOD modulation scheme. a) General arrangement of references and carriers. b) Details in a certain switching period.

To tune the three PI controllers, an empirical method by observing the stability of the system responses was used. The two power closed control loops were adjusted to obtain fast responses of the manipulated variables ($V^*_{d,ref}$ and $V^*_{q,ref}$) without errors in the steady state regarding to the references powers.

Different treatment had the PI controller dedicated to the Dc-link voltage control by acting on the D_s (manipulated variable as well). If D_s varies, the peak dc-link voltage also changes and would become uncontrollable [13]. In addition, these effects are transferred into the output ac side, which distorts the output voltage and increases the voltage stress across the semiconductors. Finally, changes in D_s also have influence on the output power. Hence, power controllers are also affected. If the response times of power controllers and the dc-link voltage controller are similar, the interaction

between them is really significant and the system responses become unstable, as shown in Fig. 8. Due to the aforementioned reasons, the tuning procedure of PI controllers is exhibited as a critical task.

TABLE I
VALUES USED FOR SIMULATION STUDY

Parameter	Unit			Value		
Inductors $L_1,\ldots, L_4$	(mH)			0.9		
Capacitors $C_1,\ldots, C_4$	(μF)			200		
LCL output filter	(mH)	(μF)	(mH)	1.2	0.11	0.5
Grid RMS voltage	(V)			230		
Input voltage	(V)			600-771		
K_P of controllers (for I_d, I_q and D_s)				$1\cdot10^{-4}$	$1\cdot10^{-4}$	$1\cdot10^{-5}$
t_I of controllers (for I_d, I_q and D_s)	(s)			$5\cdot10^{-4}$	$5\cdot10^{-4}$	0.5
Switching frequency	(kHz)			100		
Simulation step	(μs)			0.2		

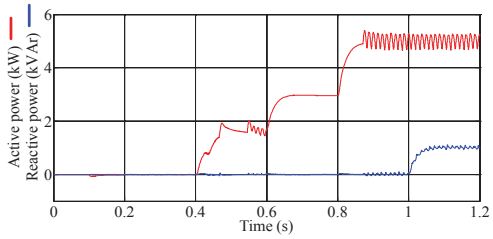

Fig. 8. *P* and *Q* responses when the dc-link control loop has fast parameters in its controllers.

A. No Shoot-Through Simulation Results

Fig. 9 represents the different main waveforms when the input voltage is 771 V. Therefore, no D_s regulation is necessary (inverter works in the buck mode). The test consists of different power reference steps. Grid connection is produced in 0.1 s (no transient or overcurrent is produced due to the $V_{d,grid}$ feedforward loop), with zero active and reactive power references. Active power reference is changed from 1.5 to 3 and to 5 kW in seconds 0.4, 0.6 and 0.8 s respectively, and the reactive power reference to 1 kVAr in second 1. As can be observed in Fig. 9*a*, the system tracks those references fast and with accuracy. An important aspect is that the influence between *P* and *Q* is practically negligible despite the fact that the decoupling method was not used. It is due to the low values of the passive elements of LCL output filter caused by the high switching frequency and the approach described in [23].

Fig. 9*b* shows the steady state waveforms of v_{grid} *(a,b,c)* and i_{grid} *(a,b,c)*. Distortion of v_{grid} *(a,b,c)* is related to the low short-circuit power grid with high impedance.

Fig. 9*c* depicts the waveforms of the input side and it is shown that the input current (I_{in}) is in continuous mode and V_{in} and V_c have the same value. Finally, in Fig. 9*d* the inverter voltages (v_{inv} *(a,b,c)*) are shown where shoot-through states are absent.

B. Simulation Results With Shoot-Through

Fig. 10 shows the main waveforms when the input voltage is lower and the shoot-through control loop is acting. The test is the same as in the previous case.

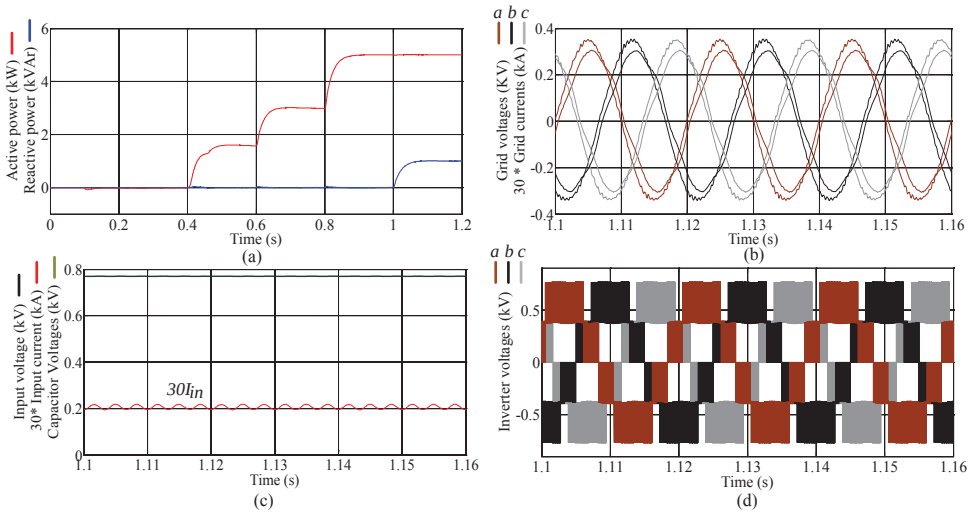

Fig. 9. Main waveforms without shoot-through operation. a) *P* and *Q* responses under different reference values. b) Steady waveforms of v_{grid} and i_{grid}. c) Steady waveforms of I_{in}, V_{in} and V_C (no boost is seen). d) Steady waveforms of v_{inv} (without shoot-through switching states).

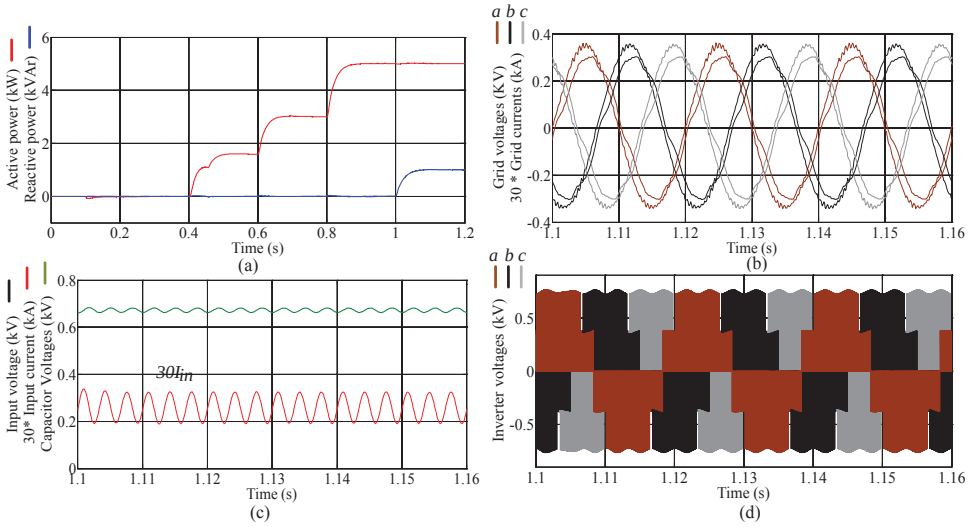

Fig. 10. Main waveforms with shoot-through operation. a) P and Q responses under different reference values. b) Steady waveforms of v_{grid} and i_{grid}. c) Steady waveforms of I_{in}, V_{in} and V_C (boost is seen). d) Steady waveforms of v_{inv} (with shoot-through switching states).

Fig. 10*a* shows that the references of P and Q are properly tracked and no influence exists between the control loops. The distortion of v_{grid} *(a,b,c)* manifested in Fig. 10*b* is higher as we anticipated in the first section due to the shoot-through changes. By controlling V_c (indirect control), the effect of dc-link voltage is transferred into the output ac side (Fig. 10*d*).

Fig. 10*c* depicts the waveforms of the input side, where the input current (I_{in}) is in continuous mode again and V_c is boosted in comparison with V_{in}. Finally, in Fig. 10*d* the inverter voltages (v_{inv} *(a,b,c)*) are shown in the presence of shoot-through states.

Fig. 11 represents the evolution of D_s during the whole simulation time. As mentioned above, this control loop was tuned looking for a slower response and in this way, small fluctuations were obtained in the steady state.

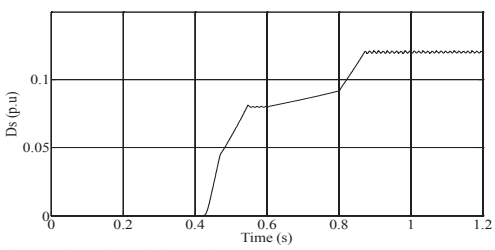

Fig. 11. Shoot-through duty cycle.

C. *Transient Responses When V_{in} Changes*

One of the most significant advantages of the inverter based impedance-source networks is the wide input operation range. Fast changes in the input voltage are common in the PV applications due to the fast changes in the irradiance conditions.

Here P and Q responses during a V_{in} step are analyzed. This voltage changes from 770 V to 500 V in the 1.2 s moment of time and the power responses are depicted in Fig. 12. It is possible to verify that in less than five fundamental periods the system tracks the references thanks to the regulation of shoot-through states (inverter changes suddenly from buck to boost mode).

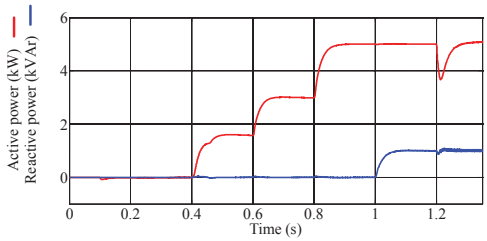

Fig. 12. System responses during a V_{in} step.

IV. CONCLUSIONS

This paper has presented a new operation strategy based on the *d-q* theory with an indirect dc-link voltage control for grid-connected three-phase inverter based on the impedance source network.

Due to the recently proposed topologies, the control system has many key aspects to be analyzed carefully. On the one hand, these include the effects of the indirect control method of the dc-link voltage in the grid-connected ac side (quality, stability, dynamic responses, etc.) and their influences on the other variables of the system, such as P and Q and its control parameters. The tuning of PI controllers is a critical task. Small changes in D_s produce considerable voltage changes in the dc-link, so those must be enclosed. In this study, large time constants for a PI controller devoted to D_s regulation were chosen to solve this problem.

Other key aspects to be dealt with are the proper operation of experimental set-ups at high switching frequency applications. Hardware limitations, PV dynamic response and the MPPT algorithm increase the complexity of the control system design. The latter aspects will be analyzed in the future studies.

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Three-Phase Three-Level Neutral-Point-Clamped qZ Source Inverter with Active Filtering Capabilities

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***Abstract*—In our effort to take advantage of a distributed location of a grid-connected photovoltaic inverter, focus is on active filtering capabilities for a grid-connected three-phase three-branch three-level neutral-point-clamped quasi impedance source inverter. An operation strategy derived from the classical *p-q* theory and a tracking technique for such topology are detailed. Different scenarios are considered with non-linear loads, to validate the proposed ideas and control systems. Our results from the PSCAD/EMTDC simulation tool show that the whole system performs well.**

Keywords—pulse width modulation inverters; photovoltaic systems; PSCAD; power system control; distributed power generation; power conditioning

I. INTRODUCTION

Low voltage electrical distribution systems worldwide have increased their number of grid-connected power electronic converters. For instance, by the end of 2013, the installed capacity of solar photovoltaic (PV) power generation reached 139 GW. For a long time, the main design objective of a PV inverter has been to extract the maximum power from the PV array and inject it into the main grid with a unitary power factor as the control reference [1]. New trends and policies for PV plants have proposed or obliged [2] to accomplish other functionalities. In this way, PV inverters would be able to contribute to the local voltage support, improve the power quality and give rise to flexibility and security of supply. Some of those demands cover power flow control [3], voltage level restoration at the point of common coupling (PCC) [4]-[5], active filtering capabilities [6], integration with energy storage systems [7], and communication compatibilities. Thus, smartgrid and microgrid [8] configurations can be a reality.

Concurrently, innovative ideas in terms of inverter circuitries have emerged. Some of them seem quite suitable for PV applications because they can step up the DC input voltage in a single power conversion stage by means of the shoot-through switching states, known as a Z-Source inverter and its derivations [9]-[11]. Furthermore, ZSI family has been integrated with multilevel bridges to acquire their intrinsic advantages [12].

Finally, it is well known that power electronic devices are widely used in industrial, commercial and domestic applications. All of them demand non-sinusoidal current and reactive power from the source, which causes voltage distortion at the PCC and affects users connected to the same one (Fig. 1 represents that cause-effect relationship). Shunt active power filters (APFs) [13] are a possible technical solution to deal with such problems. By using proper closed loop control strategies to generate the reference currents, they can supply the reactive power and harmonic contents demanded by the load.

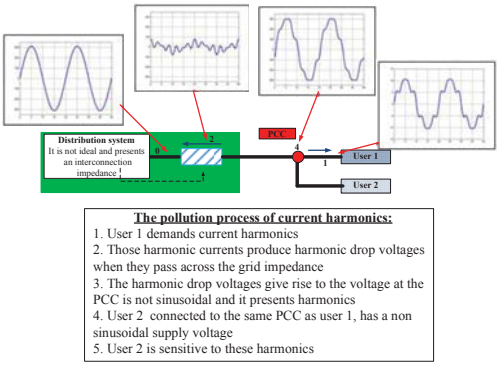


Fig. 1. Voltage distortion process caused by harmonic loads.

As mentioned above, the current low voltage electrical systems include many distributed PV inverters, which can take advantage of this distributed location to supply the non-linear loads connected to the PCC, improving the grid voltage quality in a certain way. Thus, this study explores the abilities of a 3-phase 3-level neutral-point-clamped quasi impedance source inverter (3L NPC qZSI) when it is working as an APF and a non-linear load is connected at the same PCC (schematic of the studied case is depicted in Fig. 2). The topology is mainly characterized by single stage energy conversion with boost function, by the inclusion of shoot-through states.

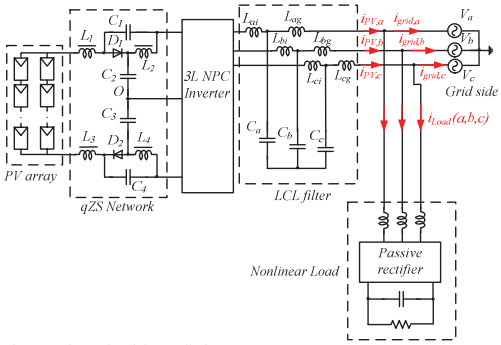


Fig. 2. Schematic of the studied case.

Hence, this control loop must be taken into account. Section 2 explains the control strategy and tracking technique for the 3L NPC qZSI, dealing with harmonic cancellation and reactive power compensation. Section 3 shows the simulation results under different test conditions in order to validate the proposed solution.

II. Operation Strategy and Tracking Technique for 3L NPC QZSI Acting as APF

Traditional control strategies for shunt APFs generate the reference current that must be provided to compensate reactive power and harmonic currents demanded by the load. This involves a set of currents in the phase domain, which will be tracked, generating the proper switching signals for the electronic converter, by means of the appropriate closed loop switching control technique such as hysteresis or dead-beat control. Four control strategies that stand out in the literature are: *p-q* method [14], i_d-i_q method [15], unitary power factor, and perfect harmonic cancellation [16].

For our case of study and as the main goal is to analyze the ability of this PV converter to develop reactive power compensation and harmonic cancellation tasks, just are necessaries to use three branches of the inverter. The strategy is derived from the *p-q* theory approach, combined with the DC-Link voltage control loop. The operation is explained below in the scheme in Fig. 3.

Reference current of the 3L NPC qZSI ($i_{PV,ref}$ *(a,b,c)*) is composed by the active power from the PV maximum power point tracker algorithm (MPPT), reactive power (*q(t)*) and non-active power ($p(t)$- $\bar{p}(t)$) demanded by the load. Those last two terms are obtained as follows: once v_{grid} *(a,b,c)* and i_{Load} *(a,b,c)* have been sensed, they are transformed into *α-β* quantities (Clarke transformation) in order to calculate the instantaneous real power (*p(t)*) and the instantaneous reactive power (*q(t)*) as:

$$p(t) = v_{grid,\alpha} \cdot i_{Load,\alpha} + v_{grid,\beta} \cdot i_{Load,\beta} \tag{1}$$

$$q(t) = v_{grid,\alpha} \cdot i_{Load,\beta} - v_{grid,\beta} \cdot i_{Load,\alpha} . \tag{2}$$

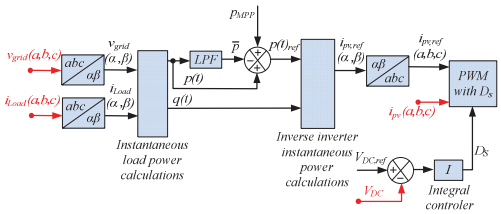


Fig. 3. Block diagram of the proposed control strategy.

After filtering *p(t)*, just AC component (non-active power) of *p(t)* is left. Subsequently, it is easy to obtain *α-β* quantities of $i_{pv,ref}$ *(a,b,c)* to finally turn them into phase domain currents with inverse Clarke transformation. Operating in this way, sinusoidal current in phase with the grid voltage will be required from the distribution grid.

DC-Link voltage control loop is built with one integral controller, which adjusts the shoot-through duty cycle (D_s) depending on the error between a predefined value for the DC-link voltage ($V_{DC,\ ref}$) and the sensed DC-Link voltage (V_{DC}) (known as indirect DC-Link control method [17]). If an error is positive, boost mode is presented in the converter.

In order to track $i_{pv,ref}$ *(a,b,c)*, a proportional controller was performed to limit the maximum current ripple. The error between the reference and the sensed currents is scaled with the assumed ripple. After that, it is needed to limit such value in order to take into account the possibility of including D_s due to the next constraint (implementation sketch is depicted in Fig. 4):

$$M \leq 1 - D_s . \tag{3}$$

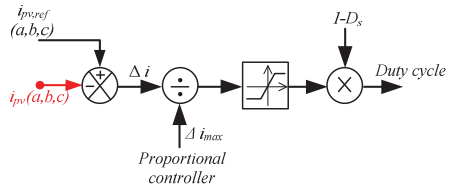


Fig. 4. Block diagram of duty cycles generation.

The values obtained after that procedure are considered as duty cycles to be applied by the 3L NPC qZSI. To generate the switching signal pattern (active states, zero states and shoot-through states), an Alternative Phase Opposition Disposition (APOD) Pulse Width Modulation (PWM) scheme was used in our simulations. Three modulating waves ($Duty_{,a}$, $Duty_{,b}$ and $Duty_{,c}$, obtained from the block diagram of Fig. 4) and two modified references (MR_1 and MR_2) are compared with two vertically disposed 180º phase-shifted carriers in order to obtain the different states of each switch (T) in each branch (a, b and c) by direct comparisons between signals or their complementary states. Details of this modulation approach are provided in [18]. Fig. 7 a) depicts the sketch of this modulation technique using a frequency modulation index (m_f) equal to 21 and Fig. 7 b) shows the details in a certain switching period.

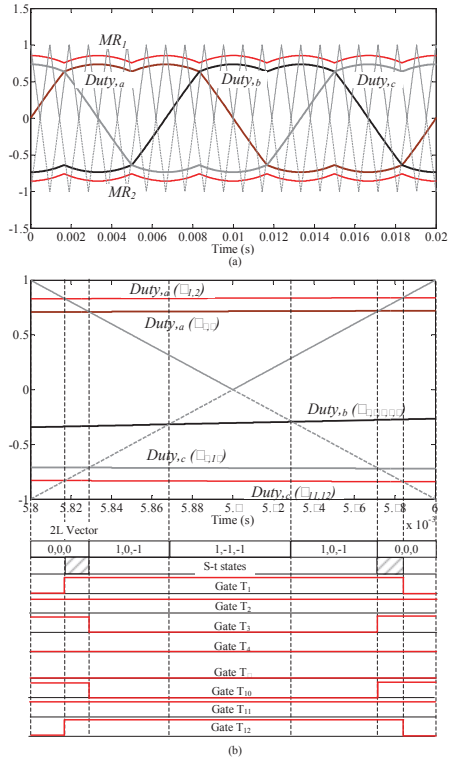


Fig. 5. Switching signal generations (normal states and shoot-through states).

III. Simulation Results

To validate the proposed strategy and demonstrate the ability of the 3L NPC qZSI to deal with active filtering functions, a simulation study in PSCAD□EMTDC is explained in this section. The main scenario is depicted in Fig. 2 and different conditions were selected to analyze the system performance. They can be summarized as follows:

- No compensations.
- Reactive power and harmonic content (demanded by the load) compensation. It is assumed that P_{MPP} is equal to zero.
- Reactive power, harmonic content compensation and P_{MPP} is equal to the fundamental active power demanded by the load.
- Reactive power, harmonic content compensation and P_{MPP} is larger than the fundamental active power demanded from the load.

The parameters used in the simulation study are presented in Table I. Values of the passive elements of the qZ network and the output filter were calculated according to guidelines in [1□]-[20].

□□ □o Compe□satio□s

In this case the inverter is disabled and the current that flows to the nonlinear load (i_{Load} *(a,b,c)*) is supplied by the electrical grid. As a result, the voltage at the PCC would be distorted, depending on the grid impedance. Main waveforms of that situation are shown in Fig. 6 a) and b).

□□ *Reactive Po□er a□d □armo□ic Co□te□t Compe□satio□□ MPP □qua□to □ero*

In this situation the converter will compensate the reactive power and the non-active power demanded by the load. The fundamental active power ($\bar{p}(t)$) will be provided by the electrical grid. Current waveforms of the inverter (i_{PV} *(a,b,c)*) and grid currents (i_{grid} *(a,b,c)*) are depicted in Fig. 7 a) and b). Obviously, the demanded current from the load (i_{Load} *(a,b,c)*) is equal as in Fig. 6 a).

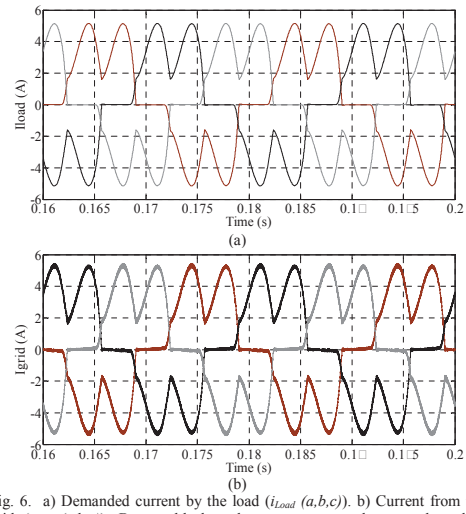


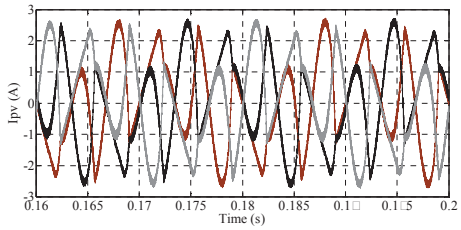
Fig. 6. a) Demanded current by the load (i_{Load} *(a,b,c)*). b) Current from the grid (i_{grid} *(a,b,c)*). Brown, black and grey represent phases a, b and c, respectively.

TABLE I
Values used for our Simulation Study

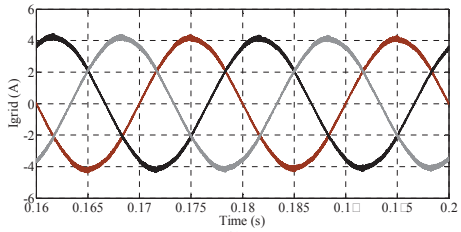
Parameter	Unit			Value		
Inductors L_1,□, L□	(mH)			0.□		
Capacitors C_1,□, C□	(μF)			200		
LCL output filter	(mH)	(μF)	(mH)	1.2	0.11	0.5
Grid RMS voltage	(V)			230		
Input voltage	(V)			525		
Maximum power point	(kW)			5		
L-C-R (values of passive rectifier)	(mH)	(μF)	(Ω)	0.75	560	145.8
Maximum i_{pv} ripple (Δi_{max})	□			5		
Switching frequency	(kHz)			100		
Simulation step	(□s)			0.2		

C□ Reactive Po□er a□d □armo□ic Co□te□t Compe□satio□□ PMPP □qua□to □u□dame□ta□□ctive Po□er Dema□ded by t□e Load

Now, the power at the *MPP* in the PV side has been adjusted to the same value as the fundamental active power demanded by the load. Thus, the result is that i_{grid} *(a,b,c)* would be equal to zero. Waveform of i_{PV} *(a,b,c)* is depicted in Fig. 8, which matches the shape and the value of i_{Load} *(a,b,c)* (Fig. 4. a). The quality of the voltage at the PCC is not affected because of the non-linear load connection, as in the previous case.



(a)



(b)

Fig. 7. a) Injected current by the inverter (i_{PV} *(a,b,c)*) current with non-active and reactive power compensation. b) Current provided by the grid (i_{grid} *(a,b,c)*) equal to the fundamental load active power.

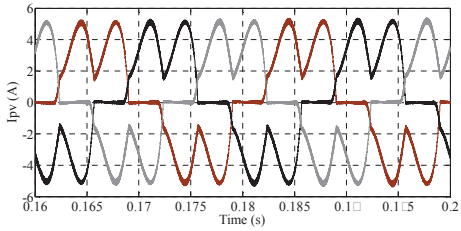
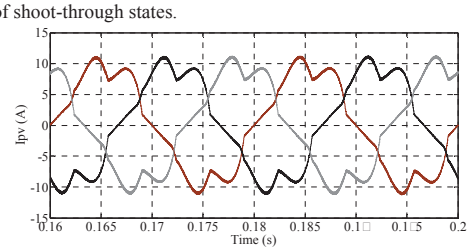


Fig. 8. Injected current by the inverter (i_{PV} *(a,b,c)*) with non-active, reactive power compensation and fundamental active power equal to the load power.

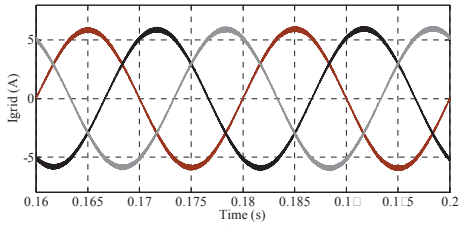
D□ Reactive Po□er a□d □armo□ic Co□te□t Compe□satio□□ P_{MPP} Larger t□a□ □u□dame□ta□□ctive Po□er Dema□ded by t□e Load

In this last situation, the power of the PV array at the *MPP* is larger than the fundamental active power, the power that the load is demanding. The excess of this active power is injected into the grid□hence, a sinusoidal current in phase with the voltage at the PCC is flowing into this. Waveforms of i_{PV} *(a,b,c)* and i_{grid} *(a,b,c)* are depicted in Fig. □ a) and b), respectively.

Fig. 10 a), b) and c) show other relevant waveforms in this situation: input current into the qZ network, DC-link voltage and voltage between the middle point of branch A and the ground. Fig. 10 a) shows that the input current is in continuous mode. Fig. 10 b) and c) reveal that the converter is working in boost mode, because both voltages drop uniformly to zero during the whole fundamental period because of the insertion of shoot-through states.

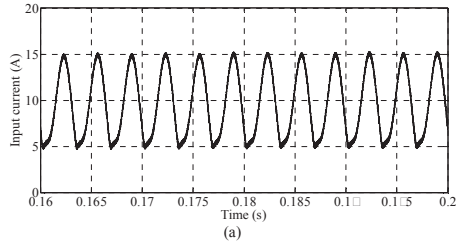


(a)

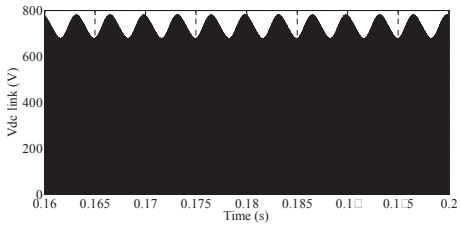


(b)

Fig. □ a) i_{PV} *(a,b,c)* with non-active, reactive power compensation and *MPP* power larger than power demanded by the load. b) i_{grid} *(a,b,c)* that flows to the grid.



(a)



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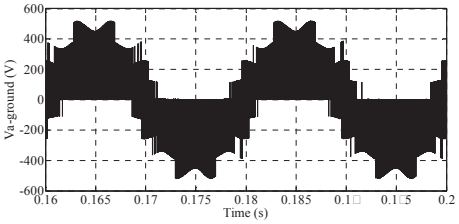

(c)

Fig. 10. a) Input current□b) DC-Link voltage□c) voltage between the middle point of branch A and the ground.

IV. CONCLUSIONS

An operation strategy with its tracking technique for a three-phase 3L NPC qZS inverter has been proposed and validated by means of simulation. The core idea is to take advantage of the distributed location of a PV inverter to compensate harmonic currents and reactive power demands locally. Obtained results have demonstrated good performance in different test conditions. Those tests were conducted simultaneously with the converter boosting the input voltage. Further research will focus on the experimental validation of the ideas and conclusions derived from this work.

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Short Curriculum Vitae

1. Personal data
   Name: Carlos Roncero Clemente
   Date and place of birth: 02.04.1984 in Badajoz, Spain
   Email: croncero@peandes.net
2. Education
   Bachelor Science in Electrical Engineering by University of Extremadura (2002-2006)
   Master Science in Industrial Management Engineering by University of Extremadura (2007-2008)
   Master Science in Architecture and Engineering Research by University of Extremadura (2011)
3. Professional employment
   Assistant research in PE&ES Research Group at the Electrical, Electronic and Control Engineering Department from University of Extremadura (2007-2010)
   Junior researcher and PhD student in PE&ES Research Group at the Electrical, Electronic and Control Engineering Department from University of Extremadura (2011-2015)
4. Honours and awards
   Best student in Bachelor Science in Electrical Engineering (2006)
   Best student in Master Science in Industrial Management Engineering (2008)
   First position in the call for young researcher scholarships from University of Extremadura (2010)
   First position in the call for PhD student scholarships from University of Extremadura (2015)
5. Research project participation
   Current conditioner for low voltage distribution networks (2008-2010)
   SIDER: Smart Inverter for Distributed Energy Resources (2011-2015)
6. Field of research
   Power electronic interfaces, modulation techniques, renewable energy sources and smart grids

The results obtained during the PhD research have been reported at 2 book chapters and published in 14 journal papers, in 15 international conferences and in 8 national conferences. 11 of the journal papers are published in journals included in the JCR list. In addition, one co-authored patent application was submitted to the European patent office.

Book chapters (2):

1. Carlos Roncero-Clemente, Serhii Stepenko, Oleksandr Husev, Víctor Miñambres-Marcos, Enrique Romero-Cadaval and Dmitri Vinnikov, *"Three-Level Neutral-Point-Clamped Quasi-Z-Source Inverter with Maximum Power Point Tracking for Photovoltaic Systems"*. Book chapter in: Technological Innovation for the Internet of Things. Editorial: Springer Berlin Heidelberg, pp. 334-342. 2013.
2. S. Polo-Gallego, C. Roncero-Clemente, E. Romero-Cadaval, V. Miñambres-Marcos, and M.A. Guerrero-Martínez, *"Development of a Photovoltaic Array Emulator in a Real Time Control Environment Using xPC Target*". Book chapter in: Technological Innovation for the Internet of Things. Editorial: Springer Berlin Heidelberg, pp. 325-333. 2013.

Journal publications listed in JCR (11):

1. Eugenio Roanes-Lozano, Luis M. Laita, Eugenio Roanes-Macías, Michael J. Wester, José Luis Ruiz-Lozano and Carlos Roncero, "*Evolution of railway network flexibility: The Spanish broad gauge case"*. Mathematics and Computer in Simulations, vol. 79, pp. 2317-2332. 2009. (Journal listed in second third (80/204).
2. Carlos Roncero-Clemente, M.I. Milanés-Montero, E. Romero-Cadaval, E. González-Romera and F. Barrero-González, *"Medida de energía en condiciones de distorsión y desequilibrio"*. Dyna Ingeniería e Industria, vol. 86, pp. 567-574. 2011. (Journal listed in last third (84/90)).
3. Carlos Roncero, María I. Milanés, Miguel A. Guerrero and E. Romero, *"Controllable electronic load with energy recycling capability"*. PRZEGLĄD ELEKTROTECHNICZNY (Electrical Review), vol. 87, pp. 154-159. 2011. (Journal listed in last third (221/245)).
4. Carlos Roncero-Clemente, E. Romero Cadaval, V. M. Miñambres Marcos, M. A. Guerrero Martínez and J. Gallardo Lozano, *"PV Array Emulator for Testing Commercial PV Inverters"*. ELEKTRONIKA IR ELEKTROTECHNIKA, (Electronics and Electrical Engineering), vol. 19, pp. 71-75. 2012. (Journal listed in last third (204/248)).
5. Carlos Roncero-Clemente, O. Husev, V. Miñambres-Marcos, E. Romero-Cadaval, S.Stepenko and D. Vinnikov, *"Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications"*. Informacije MIDEM. Journal of Microelectronics, Electronics Components and Materials, vol. 43, pp. 212-221. 2013. (Journal listed in last third (217/248)).

6. C. Roncero-Clemente, O. Husev, T. Jalakas, E. Romero-Cadaval, J. Zakis and V. Minambres-Marcos, *"PWM for Single Phase 3L Z/qZ-Source Inverter with Balanced Power Losses"*. ELEKTRONIKA IR ELEKTROTECHNIKA, (Electronics and Electrical Engineering), vol. 20, pp. 71-76. 2014. (Journal listed in last third (204/248)).
7. Oleksandr Husev, Andrii Chub, Enrique Romero-Cadaval, Carlos Roncero-Clemente and D. Vinnikov, *"Voltage Distortion Approach for Output Filter Design for Off-Grid and Grid-Connected PWM Inverters"*. Journal of Power Electronics, vol. 15, pp. 278-287. 2014. (Journal listed in last third (173/248)).
8. Oleksandr Husev, Carlos Roncero-Clemente, Enrique Romero-Cadaval, Dmitri Vinnikov and Serhii Stepenko, *"Single phase three-level neutral-point-clamped quasi-Z-source inverter"*. IET Power Electronics, vol. 8, pp. 1-10. 2015. (Journal listed in second third (113/248)).
9. F. Barrero-González, M.I. Milanés-Montero, E. González-Romera, C. Roncero-Clemente and P. González-Castrillo, *"El Control de Potencia y Frecuencia en los Sistemas Eléctricos Multiárea. Revisión y Nuevos Retos"*. Revista Iberoamericana de Automática e Informática Industrial (RIAI). Accepted for publication. 2015. (Journal listed in last third (58/59)).
10. Oleksandr Husev, A. Chub, E. Romero-Cadaval, C. Roncero-Clemente and D. Vinnikov, *"Hysteresis Current Control with Distributed Shoot-Through States for Impedance Source Inverters"*. International Journal of Circuit Theory and Applications. Online published on 2015. (Journal listed in second third (126/248)).
11. Oleksandr Husev, Carlos Roncero-Clemente, Enrique Romero-Cadaval, Dmitri Vinnikov and Tanel Jalakas, *"Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application"*. Electric Power Systems Research. Accepted for publication in 2015. (Journal listed in second third (126/248)).

Journal publications not listed in JCR (3):

1. Carlos Roncero Clemente, Enrique Romero Cadaval, Oleksandr Husev and Dmitri Vinnikov, *"Simulation Study of Different Modulation Techniques for Three-Level Quasi-Z-Source Inverter"*. Electrical, Control and Communication Engineering, vol. 1, pp. 11-17. 2012.
2. Carlos Roncero Clemente, Enrique Romero Cadaval, Oleksandr Husev; Dmitri Vinnikov and Serhii Stepenko, "Simulation of Grid Connected Three-Level Neutral-Point-Clamped qZS Inverter using PSCAD". Electrical, Control and Communication Engineering, vol. 2, pp. 14-19. 2013.
3. Carlos Roncero Clemente, Oleksandr Husev, Serhii Stepenko, Enrique Romero Cadaval and Dmitri Vinnikov, *"Output voltage control system for a three-level neutral-point clamped quasi-Z-source inverter"*. PRZEGLĄD ELEKTROTECHNICZNY (Electrical Review), vol. 5, pp. 76-80. 2013.

Contribution to international conferences (15):

1. Carlos Roncero Clemente, María Isabel Milanés Montero, V. M. Miñambres Marcos and E. Romero Cadaval, *"Three-Phase Regenerative Electronic Load to Test Shunt Power Conditioners"*. IEEE 7th International Conference on Compatibility and Power Electronics (CPE2011). Tallinn (Estonia). 2011.
2. Carlos Roncero Clemente, Enrique Romero Cadaval, Oleksandr Husev and Dmitri Vinnikov, *"New Modulation Technique for Three-Level Quasi-Z-Source Inverter"*. 12th International Symposium, Topical Problems in the Field of Electrical and Power Engineering. Doctoral School of Energy and Geotechnology II. Kuressare (Estonia). 2011.
3. Oleksandr Husev, Carlos Roncero Clemente, Sergey Stepenko, Dmitri Vinnikov and Enrique Romero Cadaval, *"CCM Operation Analysis of the Single-Phase Three-Level Quasi-Z-Source Inverter"*. 15th IEEE International Power Electronics and Motion Control Conference, EPE-PEMC 2012 ECCE Europe. Novi Sad (Serbia). 2012.
4. Carlos Roncero Clemente, Enrique Romero Cadaval, Oleksandr Husev and Dmitri Vinnikov, *"Simulation Study of Different Modulation Techniques for Three-Level Quasi-Z-Source Inverter"*. Riga Technical University 53rd International Scientific Conference, Power and Electrical Engineering. Riga (Latvia). 2012.
5. Oleksandr Husev, Sergey Stepenko, Carlos Roncero Clemente, Enrique Romero Cadaval and Dmitri Vinnikov, *"Single Phase Three-Level Quasi-Z-Source Inverter With a New Boost Modulation Technique"*. IEEE 38th Annual Conference of the IEEE Industrial Electronics Society, IECON 2012. Montreal (Canada). 2012.
6. Carlos Roncero Clemente, Enrique Romero Cadaval, Pedro Roncero Sánchez and Eva González Romera, *"Comparison of Two Power Flow Control Strategies for Photovoltaic Inverters"*. IEEE 38th Annual Conference of the IEEE Industrial Electronics Society, IECON 2012. Montreal (Canada). 2012.
7. Oleksandr Husev, Serhii Stepenko, Carlos Roncero Clemente, Dmitri Vinnikov and Enrique Romero Cadaval, *"Output Filter Design for Grid Connected Single Phase Three-Level Quasi-Z-Source Inverter"*. 8th International Conference on Compatibility and Power Electronics (CPE2013). Ljubljana (Eslovenia). 2013.
8. C. Roncero Clemente, E. González- Romera, E. Romero-Cadaval, M. I. Milanés Montero and V. Miñambres, *"PSCAD/EMTDC Model for Photovoltaic Modules with MPPT based on Manufacturer Specifications"*. 8th International Conference on Compatibility and Power Electronics (CPE2013). Ljubljana (Eslovenia). 2013.

9. Oleksandr Husev, Serhii Stepenko, Carlos Roncero-Clemente, E. Romero-Cadaval and R. Strzelecki, *"Experimental Investigation of High Frequency 3L-NPC qZS Inverter for Photovoltaic Application"*. IEEE 39th Annual Conference of the IEEE Industrial Electronics Society, IECON 2013. Vienna (Austria). 2013.
7. Carlos Roncero-Clemente, Enrique Romero-Cadaval, Oleksandr Husev, Dmitri Vinnikov and Serhii Stepenko, *"Grid-Connected PV System Based on a Single-Phase Three-Level qZS Inverter"*. IEEE 39th Annual Conference of the IEEE Industrial Electronics Society, IECON 2013. Vienna (Austria). 2013.
8. Carlos Roncero-Clemente, Oleksandr Husev, Enrique Romero-Cadaval and Dmitri Vinnikov, *"P and Q Control Strategy for Single Phase Z/qZ Source Inverter Based on d-q Frame"*. 23rd IEEE International Symposium on Industrial Electronics, ISIE 2014. Estambul (Turkey). 2014.
9. Carlos Roncero-Clemente, Oleksandr Husev, Enrique Romero-Cadaval J. Zakis, Dmitri Vinnikov and M.I. Milanés-Montero, *"Simulation Study of the Grid-Connected Single-phase Impedance Source NPC Inverter with Different Control Methods"*. IEEE International Conference on Industrial Technology (ICIT) 2015. Sevilla (Spain). 2015.
10. Carlos Roncero-Clemente, O. Husev, E. Romero-Cadaval, J. Zakis, D. Vinnikov and M.I. Milanés-Montero, *"Operation Strategy and Shoot-Through Indirect Control Method for Three-Phase Z-Source Inverters"*. IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG) 2015. Riga (Latvia). 2015.
11. C. Roncero-Clemente, O. Husev, E. Romero-Cadaval, J. Martins, D. Vinnikov and M.I. Milanés-Montero, *"Three-Phase Three-Level Neutral-Point-Clamped qZ Source Inverter with Active Filtering Capabilities"*. 9th International Conference on Compatibility and Power Electronics (CPE2015). Lisboa (Portugal). 2015.
15. Tatiana Shults, O. Husev, Carlos Roncero-Clemente, Frede Blaabjerg, and Ryszard Strzelecki, *"Design of Three-Phase Three-Level CIC T-Source Inverter with Maximum Boost Control"*. Accepted for oral session presentation in IEEE 41th Annual Conference of the IEEE Industrial Electronics Society, IECON 2015.

This work was partly carried out in different foreign research centres. The date and duration of each research stage are included below.

Research stages abroad

Research Center: Department of Electrical Engineering at Tallinn University of Technology

City: Tallinn Country: Estonia Año: 2012

Duration (months): 3

Research Center: Department of Electrical Engineering at Tallinn University of Technology

City: Tallinn Country: Estonia Año: 2013

Duration (months): 1

Research Center: Department of Energy Technology at Aalborg University

City: Aalborg Country: Danmark Año: 2014

Duration (months): 5